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VKD233HM Datasheet

1ch Touch/One-to-one output

Rev.1.2

1 General Description

VKD233HM is a single-channel touch detection chip. Its low power consumption, wide operating voltage range and stable touch detection effect can widely meet the needs of different applications. This touch detection chip is specially designed to replace traditional keys. It is equipped with a built-in voltage stabilizing circuit to provide a stable voltage for the touch detection circuit to use. The size of the touch detection PAD can be designed within a reasonable range according to different sensitivities.

2 Key Features

- Operating voltage: 2.4V to 5.5V
- Operating current 4.0uA@VDD=3.0V
- Low-voltage reset function (LVR)
- Built-in dedicated voltage stabilizing circuit for touch detection
- The response time is approximately 46ms @VDD=3V
- The sensitivity can be adjusted by an external capacitor (1 to 60pF)
- Built-in key debouncing, no need for external software to debouncing
- Press and hold the button (touch without leaving) for 16 seconds to reset
- Pin Q is an open-drain output
  The output mode is selected by the MDT pin as either direct output or latch output
- There is approximately 0.3 seconds of stabilization time after power-on. During this period, all functions are disabled. Do not touch the detection point during this time
- Self-calibrate parameters according to environmental changes
- The static electricity of HBM is greater than 4KV
- Available Packages:
  SOT23-6L(3mm x 3mm PP=0.95mm)

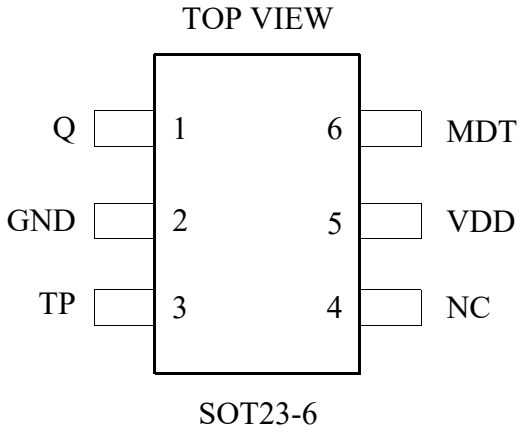
3 Product Selection

Part No.	Working voltage	Mode working/standby	Output (/ Optional)	Packaging
VKD223EB	2.0-5.5V	4.0uA/1.5uA(3V)	Directly/latch high/low levels	SOT23-6L
VKD233HB	2.4-5.5V	4.0uA/1.5uA(3V)	Directly/latch high/low levels	SOT23-6L
VKD233HH	2.4-5.5V	4.0uA/1.5uA(3V)	Directly/latch high/low levels and hold for 16 seconds to reset	SOT23-6L
VKD233HS	2.4-5.5V	4.0uA/no(3V)	Directly/latch high/low levels and hold for 16 seconds to reset	DFN6L
VKD233HR	2.4-5.5V	4.0uA/1.5uA(3V)	Directly/latch high/low levels and hold for 16 seconds to reset	DFN6L
VKD233HM	2.4-5.5V	5.0uA/no(3V)	Direct/latch open leakage low valid press and hold for 16 seconds to reset	SOT23-6L
VKD101HH	2.4-5.5V	4.0μA/1.5μA(3V)	Directly/latch high/low levels	SOT23-6L

4 Ordering Information

Part No.	Packaging	Tube Qty	Tray(reel) Qty	Box Qty	Total Qty	Notes
VKD223EB	SOT23-6L	—	3000/reel	30000/box	120000 PCS	
VKD233HB	SOT23-6L	—	3000/reel	30000/box	120000 PCS	
VKD233HH	SOT23-6L	—	3000/reel	30000/box	120000 PCS	
VKD233HS	DFN6L	—	3000/reel	30000/box	120000 PCS	
VKD233HR	DFN6L	—	3000/reel	30000/box	120000 PCS	
VKD233HM	SOT23-6L	—	3000/reel	30000/box	120000 PCS	
VKD101HH	SOT23-6L	—	3000/reel	30000/box	120000 PCS	

5 Package Pinout Information(SOT23-6)



For more information: Page 10

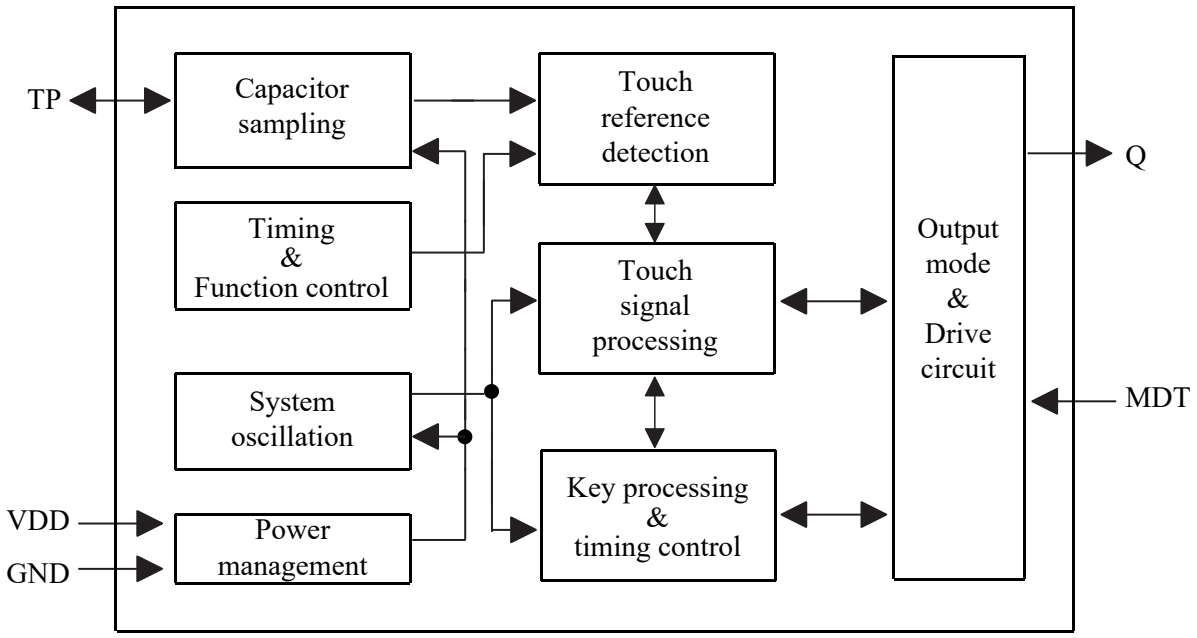
5.1 VKD233HM/SOT23-6L Pin Description

Pin No.	Pin name	I/O	Function Description
1	Q	O	CMOS Output
2	GND	P	Negative power supply
3	TP	I/O	Touch detection
4	NC	—	—
5	VDD	P	Positive power supply
6	MDT	I—RL	Select the output mode 0(default)➔Direct output；1➔Latch output

- **I** CMOS In
- O CMOS Output
- I/O CMOS Input/Output
- **P** Power supply/Groundin
- I-RH CMOS input has a built-in pull-up resistor
- I-RL CMOS input has a built-in pull-down resistor
- OD Open-drain output, no diode protection circuit

6 Functional Description

6.1 Block Diagram



6.2 Output Mode (selected using pins MDT)

MDT：Choose direct output or latch output.

Q Pin output parameters：

MDT	Output parameters
0	Direct CMOS output, low level effective
1	Latched CMOS output, power-on state = 1

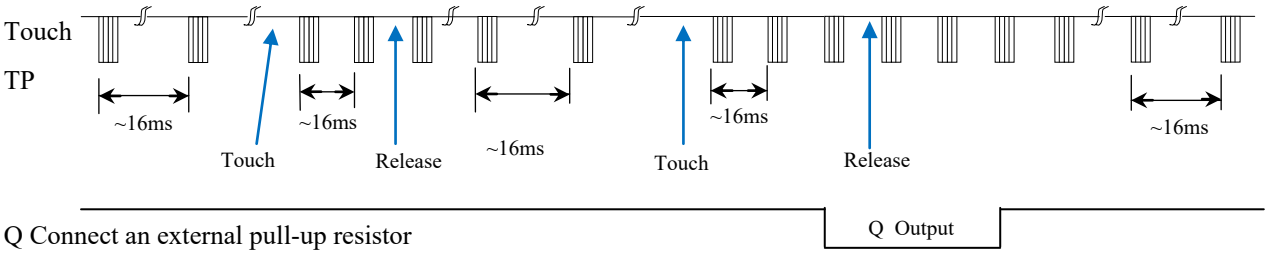
Note:
Considering energy conservation and packaging, the MDT pin is designed as a latch type, and its initial state upon power-on is either 0 or 1. If the MDT pin is connected to VDD or GND, the status will change to 1 or 0, and there will be no current leakage.

Output option pin	The initial state after power-on
MDT	0

Press and hold the button (touch without leaving) for 16 seconds to reset:
To minimize the detection of unintentional keys such as accidentally touching the sensor PAD, the chip is equipped with a maximum key duration function internally. When a touch key is pressed, the internal timer starts to count. Once the key is pressed for too long, exceeding approximately 16 seconds, the touch chip will ignore the status of the touched key, recaliculate it, obtain a new reference value, and simultaneously reset the output status to the initial power-on state.

6.3 Operating Modes

The VKD233HM chip operates in fast mode and has a relatively fast response speed. The fastest response time is approximately 46mS@3V

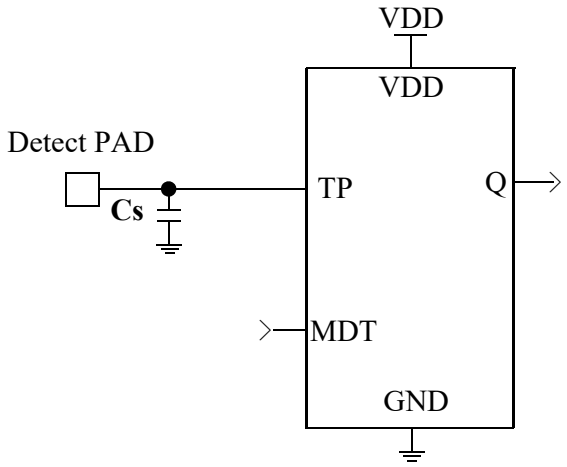


6.4 Sensitivity Adjustment

The size of the detection PAD connected on the PCB and the total load of the capacitors (parasitic capacitance and Cs capacitance) will affect the sensitivity The degree and sensitivity adjustment need to be adjusted according to the actual application.

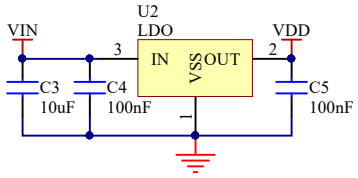
The following provides some methods for externally adjusting the sensitivity:

1. Adjust the size of the detection PAD
   Under the condition that other factors remain unchanged, using a larger detection PAD size can increase the sensitivity, and vice versa It will reduce the sensitivity, but the detection of PAD size must be used within the effective range.
2. Adjust the thickness of the medium (shell)
   Under the condition that other factors remain unchanged, using a thinner medium can increase sensitivity; conversely, it will reduce sensitivity Sensitivity, but the thickness of the medium must be below the maximum limit value.
3. Adjust the Cs capacitance value (please refer to the following figure)
   Under the condition that other factors remain unchanged, it is sensitive if the Cs capacitor is not connected to GND on the touch PAD The degree is the most sensitive. The Cs capacitance is within the usable range ($1 \leq Cs \leq 60pF$), and the larger the Cs capacitance value, the more sensitive it is The lower the sensitivity.



7 Application Circuits

It is recommended to use an LDO for power supply



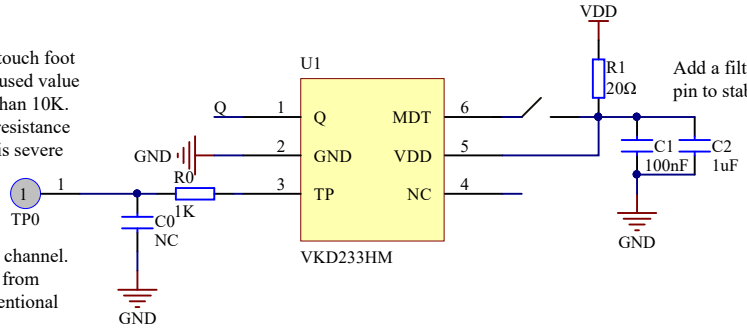
The output mode is determined by the state of the MDT pin

MDT

NC	Direct CMOS output, low level effective
VDD	CMOS latch output, power-on output 1

A 1K resistor is connected in series with the touch foot to enhance anti-interference. The commonly used value is 470R to 1K, with a maximum of no more than 10K. Depending on the interference situation, the resistance value should be increased if the interference is severe

C0 is used to fine-tune the sensitivity of each channel. Generally, the larger the capacitance ranging from 1pF to 60pF, the less sensitive it is. For conventional applications, it can be left unconnected



Add a filter capacitor to the power supply pin to stabilize the power supply

Notes:

1.On the PCB, the length of the line from the touch PAD to the touch pin should be as short as possible, and the touch traces must not be parallel or cross with other lines.

2.The power supply must be stable. Fluctuations, rapid drift or interference in the supply voltage may cause abnormal sensitivity or false detection.

3.The board covering the PCB must not contain any metal or conductive materials, and the same applies to the surface coating.

4.A C1 capacitor must be used between VDD and GND, and the distance from the VDD and GND pins of the chip should be the shortest. It is recommended to add the resistor R2 and capacitor C2 on the power supply.

5.Adjust the sensitivity of capacitor C0(0~60pF). The smaller the capacitance value, the more sensitive it is. The highest sensitivity is achieved without connecting a capacitor. The sensitivity adjustment must be made based on the actual PCB application. For conventional applications, it can be left unconnected. For C0, a capacitor with a smaller temperature coefficient and greater stability, such as X7R or NPO, must be selected.

6.Resistor R0 is mainly used to effectively prevent radio frequency interference and enhance anti-static capability. Its common value ranges from 470R to 1K, with a maximum not exceeding 10K. It can be omitted in conventional applications.

8 Electrical Characteristics

Absolute Maximum Ratings

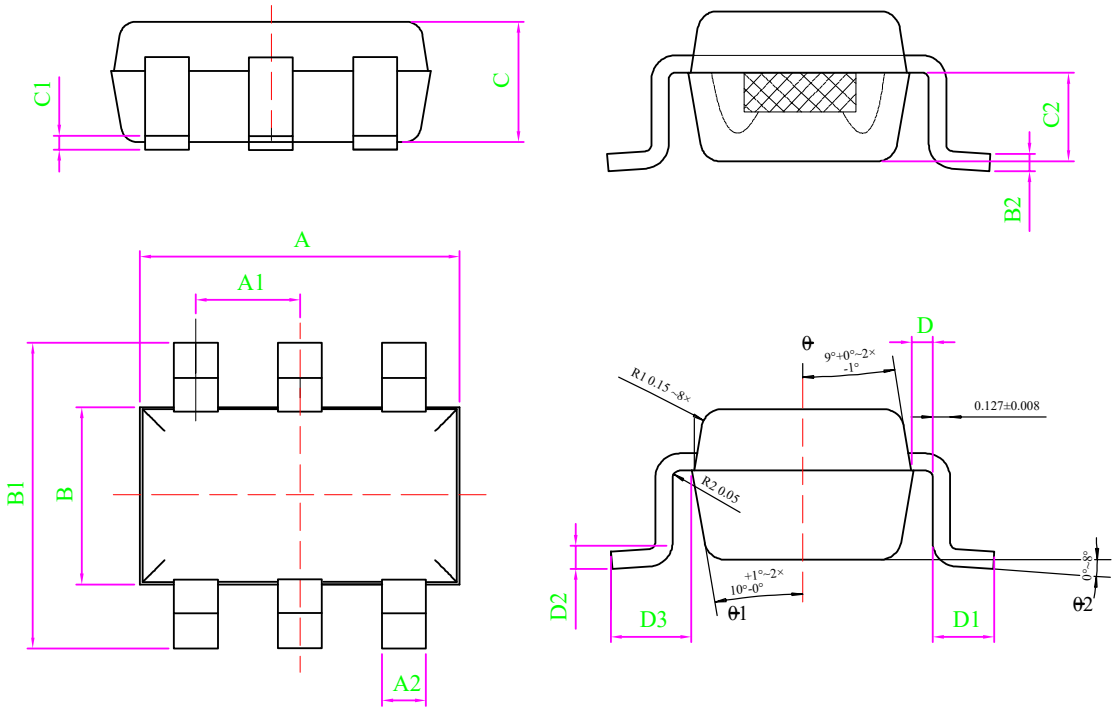
Parameter	Symbol	Ratings	Unit
Power voltage	VDD	-0.3～6.0	V
Input Voltage	V_{IN}	GND-0.3～VDD+0.3	V
Storage Temperature	T_{STG}	-50～+125	℃
Operating Temperature	T_{OTG}	-40～+85	℃
Human Body Mode	ESD	≧4	KV

DC/AC: (Test condition: Room temperature 25 ℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions (25 ℃)	
						VDD	Conditions
Operating voltage	VDD	2.4	3.0	5.5	V	—	—
Internal voltage regulator	VREG	2.2	2.3	2.4	V	—	—
Operating current	I_{OP}	—	4.0	8.0	μA	3.0V	—
Output Sink Current	I_{IL}	—	8	—	mA	3.0V	V_{OL}=0.6V
		—	16	—		5.0V	
Output Source Current	I_{OL}	—	-4	—	mA	3.0V	V_{OH}=2.4V
		—	-8	—		5.0V	V_{OH}=4.4V
Input Low Voltage	V_{IL}	—	—	0.2	VDD	VDD	Input Low Voltage
Input High Voltage	V_{IH}	0.8	—	1	VDD	VDD	Input High Voltage
Input pull-low resistor	R_L	—	25k	—	ohm	3.0V	VDD=3V
Output Response Time	T_R	—	46	—	mS	3.0V	—
		—	46	—		5.0V	—

9 Package Information

9.1 SOT23-6L(3mm x 3mm PP=0.95mm)



MILLIMETER			
SYMBOL	MIN	NOM	MAX
A	2.72	2.92	3.12
A1	0.90	0.95	1.00
A2	0.30	0.35	0.40
B	1.40	1.60	1.80
B1	2.60	2.80	3.00
B2	0.12	0.128	0.135
C	1.00	1.10	1.20
C1	0.04	-	0.10
C2	0.60	0.65	0.70
D	0.03	0.08	0.13
D1	0.30	-	0.60
D2	0.25TYP		
D3	0.60	0.65	0.70

10 Disclaimer

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11 Revision History

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Original version	YES
2	1.1	2020-02-11	Add reference circuit	YES
3	1.2	2025-11-13	Update version	YES

[1] Consult the recently published documents before starting or finishing the design.

[2] Since the release of this document , the device product status described in this document may have changed and may differ in several cases. The latest product status information can be found on the Internet at https://www.szvinka.com/