# 永嘉微电
## Vinka Microelectronics

# VK1Q60 Datasheet

8×4 LED DRIVER

Rev.1.3

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# 1  General Description

VK1Q60 is a dedicated chip for LED driver control with a keyboard scanning circuit interface. It integrates circuits such as a data latch, LED driver, and keyboard scanning internally. The SEG pin is connected to the anode of the LED, and the GRID pin is connected to the cathode of the LED, which can support 8SEG×4GRID dot matrix LED display. Supports up to 7×4 keys at most. This chip features stable performance, reliable quality and strong anti-interference ability. It is suitable for applications that require continuous operation for 24 hours. It adopts the QFN16L packaging form.

# 2  Key Features

- Operating voltage：3.0-5.5V
- Built-in RC oscillator
- 8 SEG pins, 4 GRID pins
- The SEG pin can only be connected to the anode of the LED, and the GRID pin can only be connected to the cathode of the LED
- 7×4 matrix keys do not support combination keys
  (Key display multiplexing requires hardware circuit coordination)
- 2-wire serial interface
- The overall brightness is adjustable at 8 levels
- The built-in display RAM is 8×4 bits
- Built-in power-on reset circuit
- Available Packages:
  QFN16L(3.0mm×3.0mm PP=0.5mm)

# 3  Application Field

- Small household appliances
- Induction cooker/microwave oven
- Pressure gauge

## 4   Product Selection

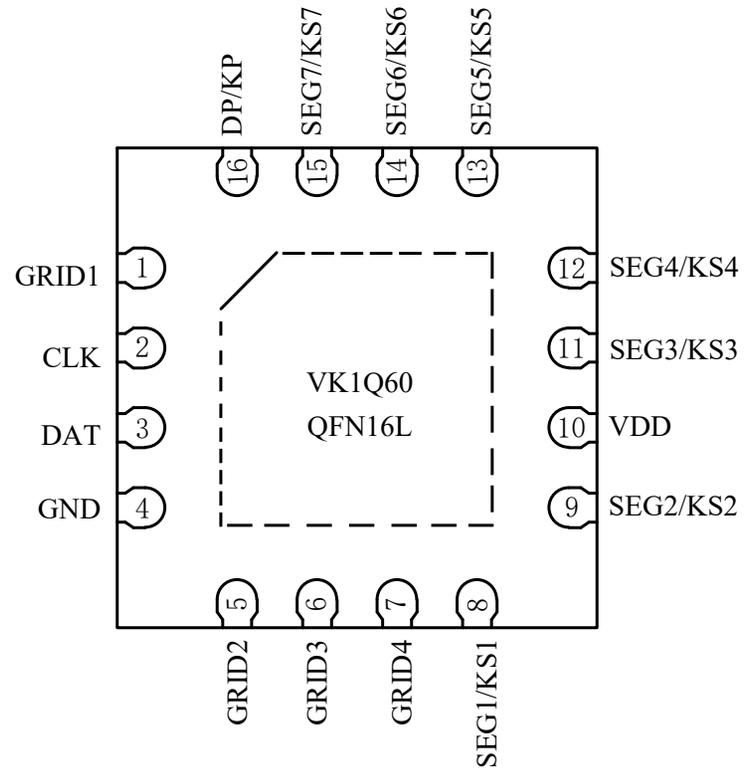| Part No. | Communication interface | Drive lattice | Common Cathode Drive | Common Anode Drive | Key press | Packaging |
|---|---|---|---|---|---|---|
| VK1640 | CLK/DIN | 128 | 8 / 16 | 16 / 8 | --- | SOP28 |
| VK1640A | CLK/DIN | 128 | 8 / 16 | 16 / 8 | --- | SSOP28 |
| VK1640B | CLK/DIN | 96 | 8 / 12 | 12 / 8 | --- | SSOP24 |
| VK1Q60 | CLK/DIN | 32 | 8 / 4 | 4 / 8 | 7×4 | QFN16L (3×3mm) |
| VK1650 | CLK/DAT | 32 | 8 / 4 | 4 / 8 | 7×4 | SOP16 |
| VK1651 | CLK/DIO | 28 | 4 / 7 | 7 / 4 | 7×1 | SOP16 |

Note: Except for VK1651, for all other common cathode/common anode digital tubes, SEG is connected to the anode and GRID to the cathode.

The SEG of VK1651 is connected to the cathode and the GRID to the anode.

## 5   Ordering Information

| Part No. | Packaging | Tube Qty | Tray(reel) Qty | Box Qty | Total Qty | Notes |
|---|---|---|---|---|---|---|
| VK1640 | SOP28 | 26/tube | | 2080/box | 20800 PCS | |
| VK1640A | SSOP28 | 50/tube | | 5000/box | 50000 PCS | |
| VK1640B | SSOP24 | 50/tube | | 10000/box | 100000 PCS | |
| VK1Q60 | QFN16L (3×3mm) | | 3000/reel | 30000/box | 120000 PCS | |
| VK1650 | SOP16 | | 4000/reel | 16000/box | 96000 PCS | |
| VK1651 | SOP16 | 50/tube | | 10000/box | | |

## 6 Package Pinout Information(QFN16L)

DP/KP (16)
SEG7/KS7 (15)
SEG6/KS6 (14)
SEG5/KS5 (13)

GRID1 (1)
CLK (2)
DAT (3)
GND (4)

VK1Q60
QFN16L

(12) SEG4/KS4
(11) SEG3/KS3
(10) VDD
(9) SEG2/KS2

GRID2 (5)
GRID3 (6)
GRID4 (7)
SEG1/KS1 (8)

For more information:

## 6.1 VK1Q60/QFN16L Pin Description

| No. | Name | I/O | Function |
|---|---|---|---|
| 1,5-7 | GRID1-GRID4 | O | LED GRID output (N-tube leakage open); Key scan output |
| 2 | CLK | I | The data clock input of the serial interface is equipped with an internal pull-up resistor |
| 3 | DAT | I/O | The data input and output of the serial interface are equipped with built-in pull-up |
| 4 | GND | GND | Negative power supply |
| 8,9, 11-15 | SEG1/KS1-SEG7/KS7 | I/O | LED SEG driver output, high level effective, also used as key scan input, high level effective, built-in pull-down |
| 10 | VDD | VDD | Positive power supply |
| 16 | DP/KP | O | LED SEG output, also used as keyboard icon output |

# 7    Functional Description

## 7.1  Block Diagram
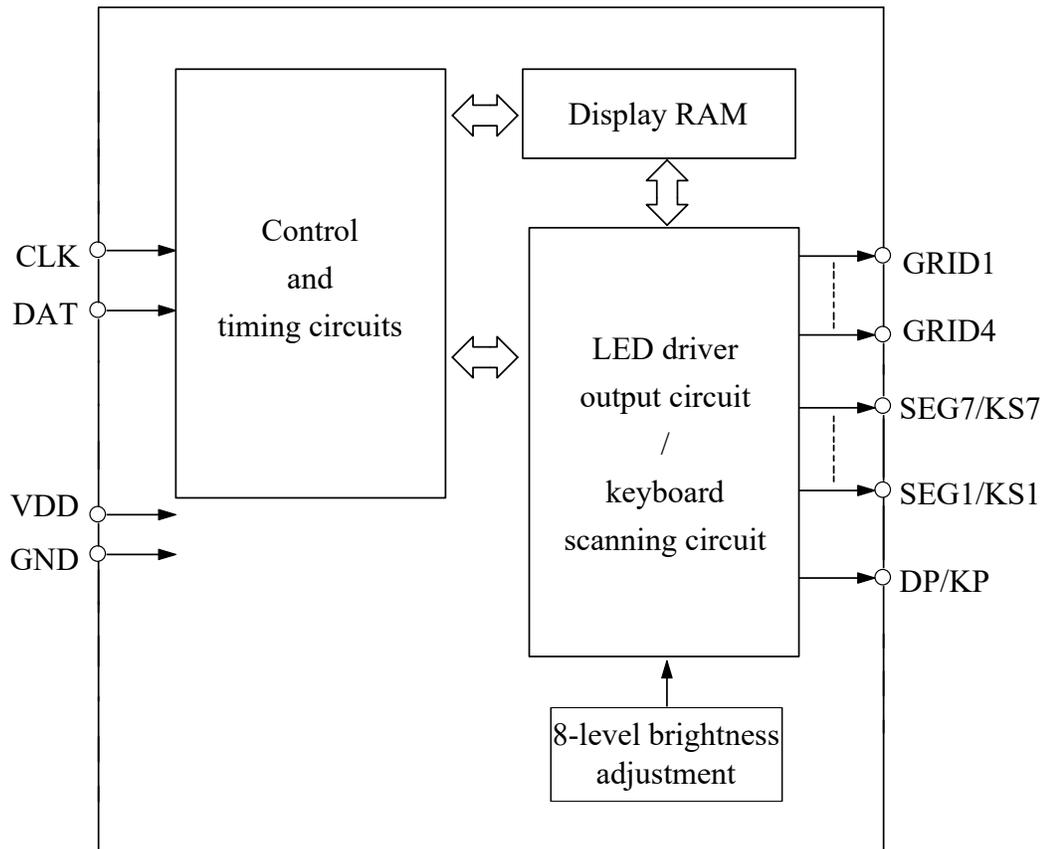
## 7.2 Display RAM- Storage Structure

The static display memory (RAM) has an 8× 4-bit structure and stores the displayed data. The content of RAM is directly mapped to the display content of the LED driver, with display addresses of 0x68,0x6A,0x6C, and 0x6E, totaling four display units. If you want to turn on or off a certain LED, simply set the corresponding display RAM position 1 or clear 0. For example, to control the on/off of LED1 driven by pins SEG1 and GRID1, simply set the corresponding display RAM (address 0x68) Bit0 position 1 or clear 0. Clear the RAM bits corresponding to the unused SEG pins in the application to 0.

The process of mapping the contents in RAM to leds is shown in the following table:

| SEG / GRID | DP | SEG7 | SEG6 | SEG5 | SEG4 | SEG3 | SEG2 | SEG1 | Addr |
|---|---|---|---|---|---|---|---|---|---|
| GRID1 | | | | | | | | LED1 | 0x68 |
| GRID2 | | | | | | | | | 0x6A |
| GRID3 | | | | | | | | | 0x6C |
| GRID4 | | | | | | | | | 0x6E |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |

Note:

1. The value stored inside the chip display RAM at the moment of power-on may be random. It is recommended that the customer perform a power-on reset of the display RAM, that is, write all the data 0x00 to the 4-byte display RAM(address 0x68,0x6A,0x6C,0x6E) after power-on.

2. The SEG pin can only be connected to the anode of the LED, and the GRID pin can only be connected to the cathode of the LED. They must not be reversed.

## 7.3 Keyboard Scanning

The keyboard scan codes corresponding to VK1Q60 are shown in the following table:

| Addressee | GRID4 | GRID3 | GRID2 | GRID1 |
|---|---|---|---|---|
| SEG1/KS1 | 47H | 46H | 45H | 44H |
| SEG2/KS2 | 4FH | 4EH | 4DH | 4CH |
| SEG3/KS3 | 57H | 56H | 55H | 54H |
| SEG4/KS4 | 5FH | 5EH | 5DH | 5CH |
| SEG5/KS5 | 67H | 66H | 65H | 64H |
| SEG6/KS6 | 6FH | 6EH | 6DH | 6CH |
| SEG7/KS7 | 77H | 76H | 75H | 74H |

Note: When using the key function, a 2KΩ resistor needs to be connected in series at the GRID pin. Combination keys are not supported.

# 8 Serial Communication Commands

## 8.1 Communication Interface

The VK1Q60 has two communication pins. Two-wire serial communication is adopted.

The CLK pin is the clock input pin. Data is written to the display RAM at the rising edge, and DIO pin data is read out at the rising edge.

The DAT pin is a serial data input pin, which is used for data input and output of the serial interface and has an inbuilt upper open leakage mode.

The starting condition for data input is that when CLK is at a high level, DAT decreases from high to low. The termination condition is that when CLK is high, DAT changes from a low level to a high level.
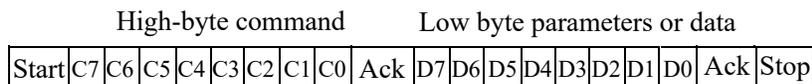
ACK signal: If the communication is normal, at the 8th clock falling edge of the serial communication, the VK1Q60 pulls down the DAT. DAT is released as input until the 9th rising edge of the clock is detected.

## 8.2 Command Description

The command is a 2-byte command, with the high byte being the command and the low byte being the set parameter, the written display data or the returned key value.

There are three types of high-byte commands:

I. System Settings Command -- used to configure parameters
II. Write Display Data Command - used for writing display data.
III. Read Key Commands - Used to read key values.

| | High-byte command | | | | | | | | | Low byte parameters or data | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Start | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 | Ack | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Ack | Stop |

## 8.3  System Settings Commands

This command is used to turn the display on and off, set the display mode, display brightness and sleep.

MSB — LSB

| Function | Byte | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | Note | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Command | 1st | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | System Settings Command | |
| Command | 2nd | 0 | 0 | 0 | 0 | | 0 | 0 | | Brightness setting | 8 levels of brightness |
| | | | 0 | 0 | 1 | | 0 | | | | 1 levels of brightness |
| | | | 0 | 1 | 0 | | 0 | | | | 2 levels of brightness |
| | | | 0 | 1 | 1 | | 0 | | | | 3 levels of brightness |
| | | | 1 | 0 | 0 | | 0 | | | | 4 levels of brightness |
| | | | 1 | 0 | 1 | | 0 | | | | 5 levels of brightness |
| | | | 1 | 1 | 0 | | 0 | | | | 6 levels of brightness |
| | | | 1 | 1 | 1 | | 0 | | | | 7 levels of brightness |
| | | | | | | 0 | 0 | | | 7/8 display control bits | 8SEG display mode |
| | | | | | | 1 | 0 | | | | 7SEG display mode |
| | | | 0 | 0 | 0 | 0 | 0 | | 0 | Turn on/off the display bit | Off display |
| | | | | | | | 0 | | 1 | | On display |
| | | | 0 | 0 | 0 | 0 | 1 | | 0 | | Activate sleep mode |

## 8.4 Write Display Data Commands

The display data write commands 0x68-0x6E respectively write data to the corresponding digital tube positions GRID1-GRID4, with each 1Bit of display data corresponding to 1 SEG.

| Function | Byte | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Note |
|----------|------|----|----|----|----|----|----|----|----|------|
| | | MSB | | | | | | | LSB | |
| Write the command to display data | 1st | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0x68 Write the display data to the digital tube position GRID1 |
| | | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0x6A Write the display data to the digital tube position GRID2 |
| | | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0x6C Write the display data to the digital tube position GRID3 |
| | | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0x6E Write the display data to the digital tube position GRID4 |
| Display data | 2nd | X | X | X | X | X | X | X | X | Display data: bit7-DP, bit6-SEG7,... bit0-SEG1 |

## 8.5 Read Key Commands

This command is used to read the key values. The keys only support single keys and do not support multiple keys being pressed simultaneously.

| Function | Byte | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | Note |
|----------|------|----|----|----|----|----|----|----|----|------|
| | | MSB | | | | | | | LSB | |
| Command | 1st | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | Read the key command |
| Key value | 2nd | X | X | X | X | X | X | X | X | Press the button to scan the code value |

# 9 Command Timing

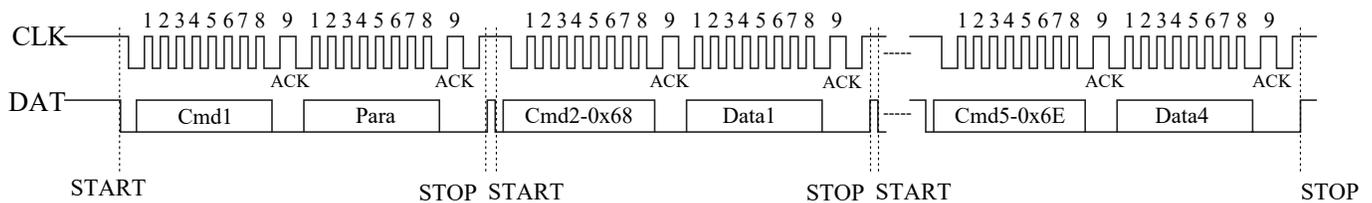## 9.1 Write Display The Data Timing Sequence

First, write the display data command (0x68-0x6E). After the command is sent, transfer 1 byte of display data.
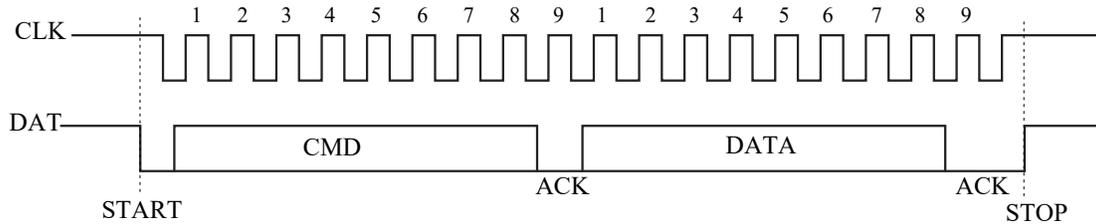


CMD: Write the display data command ->0x68-GRID1,0x6A-GRID2,0x6C-GRID3, 0x6E-GRID4

DATA: Write display data ->bit7-DP,bit6-SEG7,... bit0-SEG1

## 9.2 System Settings + Write Display Data Timing



Cmd1: System Settings Command.

Para: Display Parameters -> Open Display, set the number of LED display segments, set the display brightness level.

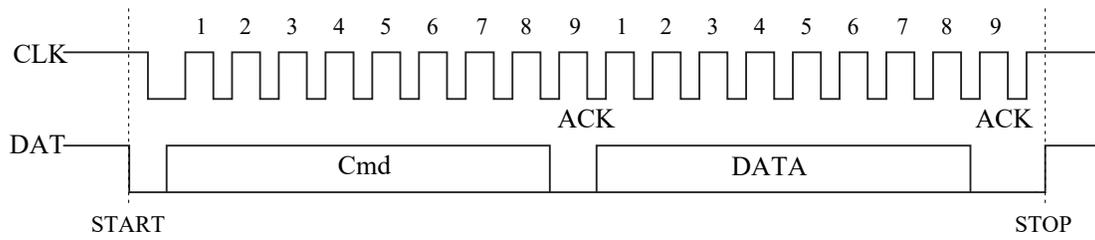Cmd2: Write the display data command 0x68.

Data1: Send display data to GRID1.

...

Cmd5: Write the display data command 0x6E.

Data4: Send display data to GRID4.

## 9.3  Read Key Timing Sequence



Cmd: Send the read key scan command (0x4F).

DATA: The key scan data read.

# 10   Application Circuits

When the surrounding interference is relatively large, a 10R to 1k resistor and a PF-level small capacitor to ground can be connected in series on the communication pin. When the power supply of the single-chip microcomputer (3.3V) and the driver chip (5V) is inconsistent, it is recommended to add a level conversion circuit on the communication pin
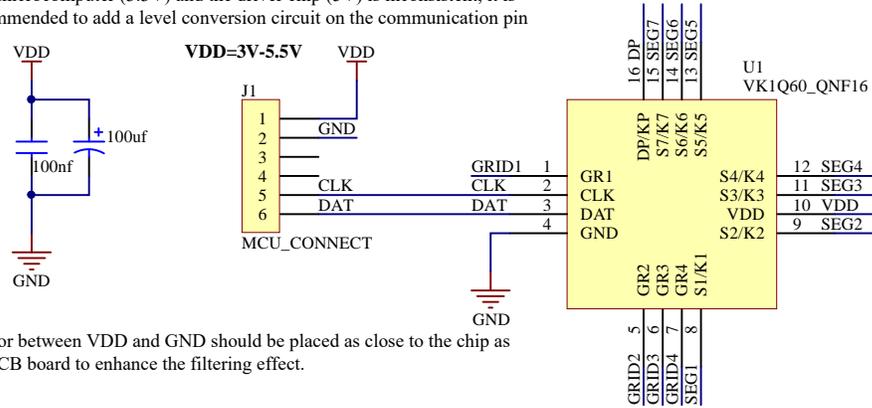
The filter capacitor between VDD and GND should be placed as close to the chip as possible on the PCB board to enhance the filtering effect.
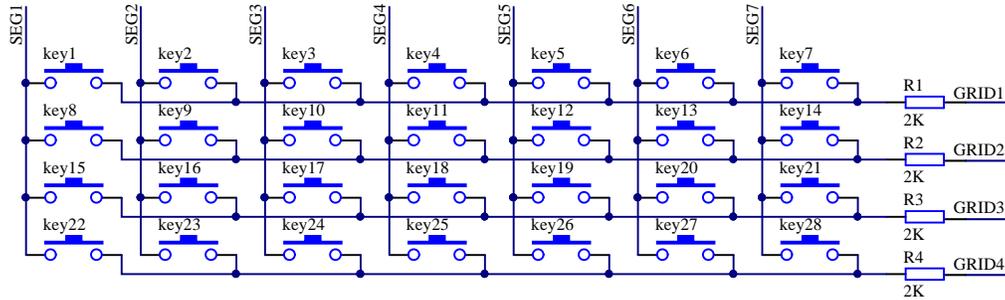
When using the key function, a 2KΩ resistor needs to be connected in series with the GRID pins.

Combination keys are not supported.
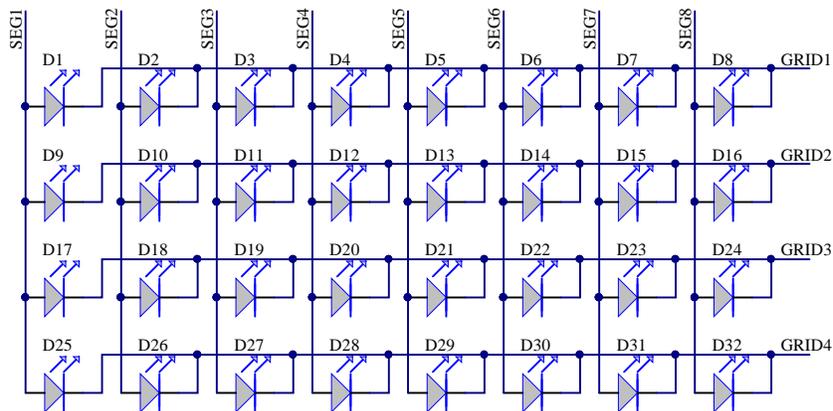
The SEG pin can only be connected to the anode of the LED, and the GRID pin can only be connected to the cathode of the LED

# 11 Electrical Characteristics

## 11.1 Absolute Maximum Ratings

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | VDD | -0.5～+6.5 | V |
| Input Voltage | VIN | $V_{SS}$-0.5～$V_{DD}$+0.5 | V |
| Storage Temperature | $T_{STG}$ | -55～+125 | ℃ |
| Operating Temperature | $T_{OTG}$ | -40～+85 | ℃ |

## 11.2 DC Electrical Characteristics

Test conditions：Ta = 25℃，VDD =5V

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Operating voltage | VDD | 3 | 5 | 5.5 | V | — |
| Static current | $I_{DD}$ | — | 80 | 150 | mA | — |
| Static current | $IC_s$ | — | 0.3 | 0.6 | mA | CLK、DAT、KP High level |
| Sleep current | $IC_{slp}$ | — | 0.05 | 0.1 | mA | CLK、DAT、KP High level |
| High-level output current | $I_{OHSEG}$ | — | -25 | — | mA | VO=VDD-2V SEG1-SEG7,DP |
| Low-level output current | $I_{OLGRID}$ | — | 150 | — | mA | VO=0.3V GRID1-GRID4 |
| Low-level Input | VIL | -0.5 | — | 0.8 | V | CLK、DAT |
| High-level Input | VIH | 2.0 | — | VDD+0.5 | V | CLK、DAT |
| Input low voltage1 | $VIL_{ki}$ | -0.5 | — | 0.5 | V | KS |
| Input high voltage1 | $VIH_{ki}$ | 1.8 | — | VDD+0.5 | V | KS |
| Input low voltage1 | $VOL_{dig}$ | — | — | 1.2 | V | GR Pin current-200mA |
| Input low voltage2 | $VOL_{dig}$ | — | — | 0.8 | V | GR Pin current-100mA |
| Input high voltage2 | $VOH_{dig}$ | 4.5 | — | — | V | GR Pin current5mA |
| Input low voltage3 | $VOL_{ki}$ | — | — | 0.5 | V | KS Pin current-20mA |
| Input high voltage3 | $VOH_{ki}$ | 4.5 | — | — | V | KS Pin current20mA |
| Input pull-down current | $I_{DN1}$ | -30 | -50 | -90 | uA | KS |
| Input pull-up current | $I_{UP1}$ | 100 | 200 | 300 | uA | CLK |
| Input pull-up current | $I_{UP2}$ | 150 | 300 | 400 | uA | DAT |
| Input pull-up current | $I_{UP3}$ | 500 | 2000 | 5000 | uA | KP |
| Power-on reset voltage | $V_R$ | 2.3 | 2.6 | 2.9 | V | POR |

## 11.3 AC Electrical Characteristics

Internal timing parameters (test conditions: Ta = 25°C, VDD =5V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Power-on reset time | $T_{PR}$ | 10 | 25 | 60 | ms |
| Display the scanning cycle | $T_P$ | 4 | 8 | 20 | ms |
| Key response time | $T_{KS}$ | 20 | 40 | 80 | ms |

Serial communication parameters (test conditions: Ta = 25°C, VDD =5V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| The establishment time of the DAT falling edge start signal | $T_{SSTA}$ | 100 | | | ns |
| The holding time of the DAT falling edge start signal | $T_{HSTA}$ | 100 | | | nS |
| The establishment time of the DAT rising edge stop signal | $T_{SSTO}$ | 100 | | | ns |
| The holding time of the DAT rising edge stop signal | $T_{HSTO}$ | 100 | | | ns |
| The low-level width of the CLK clock signal | $T_{CLOW}$ | 100 | | | nS |
| High-level width of the CLK clock signal | $T_{CHIG}$ | 100 | | | nS |
| The DAT input data establishes the time for the rising edge of CLK | $T_{SDA}$ | 30 | | | nS |
| The DAT input data establishes the time for the rising edge of CLK | $T_{HDA}$ | 10 | | | nS |
| The DAT output data effectively delays the CLK falling edge | $T_{AA}$ | 2 | | 30 | nS |
| Invalid DAT output data delays the falling edge of CLK | $T_{DH}$ | 2 | | 40 | nS |
| Average data transmission rate | $R_{ate}$ | 0 | | M | bps |

## 12 Package Information

### 12.1 QFN16L(3.0mm × 3.0mm PP=0.5mm)



TOP VIEW

SIDE VIEW

BOTTOM VIEW

EXPOSED THERMAL
PAD ZONE
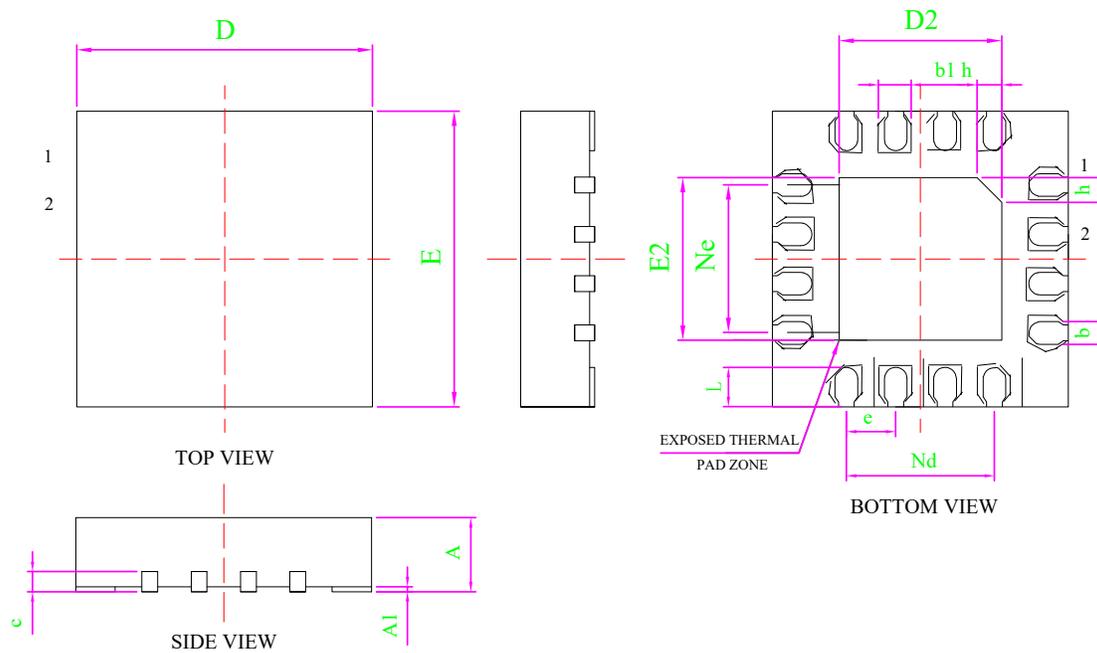
| Dimensions | | | |
|---|---|---|---|
| SYMBOL | MIN | NOMINAL | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 |
| b | 0.18 | 0.25 | 0.30 |
| b1 | 0.30 | 0.35 | 0.40 |
| c | 0.18 | 0.20 | 0.25 |
| D | 2.90 | 3.00 | 3.10 |
| D2 | 1.55 | 1.65 | 1.75 |
| e | 0.50BSC | | |
| Ne | 1.50BSC | | |
| Nd | 1.50BSC | | |
| E | 2.90 | 3.00 | 3.10 |
| E2 | 1.55 | 1.65 | 1.75 |
| L | 0.35 | 0.40 | 0.45 |
| h | 0.20 | 0.25 | 0.30 |
| L/F 载体尺寸（miL） | 75*75 | | |

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## 14 Revision History

| No. | Version | Date | Modify the content | Check |
|-----|---------|------|--------------------|-------|
| 1 | 1.0 | 2018-08-10 | Initial release | YES |
| 2 | 1.1 | 2018-10-11 | Add reference circuit | YES |
| 3 | 1.2 | 2019-03-21 | Alignment correction | YES |
| 4 | 1.3 | 2025-10-16 | Change Description | YES |

[1] Please refer to the latest version of this document before starting or finalizing any design.

[2] Since the release of this document, the status or availability of this product may have changed. For the most up-to-date information, please visit: https://www.szvinka.com/