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Vinka Microelectronics

VK16K33CQ Datasheet

8×8 LED Driver Display Chip

Rev.1.1

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1 General Description

The VK16K33C is a dedicated chip for digital tube or dot matrix LED driver control with a key scanning interface. It integrates circuits such as a data latch, keyboard scanning, and LED driver module internally. The data communicates with the MCU through the I2C communication interface. The SEG pin is connected to the anode of the LED, and the GRID pin is connected to the cathode of the LED, which can support 8SEG×8GRID dot matrix LED display panels. Supports a maximum of 8×3 keys. It is equipped with an internal power-on reset circuit. The overall flashing frequency can be set and it can enter standby mode through commands. It adopts the QFN20L package form.

2 Key Features

- Operating voltage:3.0-5.5V
- Integrated RC oscillator
- Up to 8 SEG pins and 8 GRID pins (the number of SEG pins varies depending on the encapsulation)
- The SEG pin can only be connected to the anode of the LED, and the GRID pin can only be connected to the cathode of the LED
- I2C communication interface allows the I2C slave address to be selected through the IO pin
- The overall brightness is adjustable at 16 levels
- Key scanning with a maximum of 8×3
  Key display multiplexing (requires hardware circuit coordination)
  Support combination keys (requires circuit coordination)
- Read/write display/key data addresses are automatically incremented by 1
- The built-in display RAM is 16×8 bits
- Built-in power-on reset circuit
- The overall flashing frequency can be set
- Enter standby mode through a command
- It has a large driving current and is suitable for high-brightness display scenarios
- Available Packages:
  QFN20L(3.0mm×3.0mm×0.75mm-0.40mm)

3 Product Selection

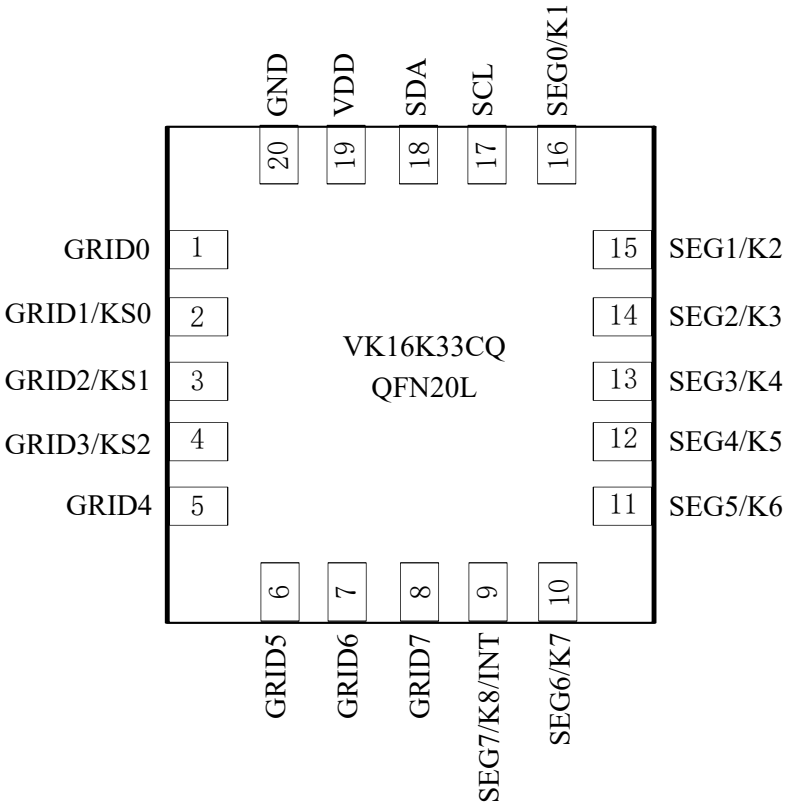
Part No.	Common Cathode Drive	Common Anode Drive	Key press	Packaging
VK16K33A	16 /8	8 /16	13×3	SOP28
VK16K33AA	16 /8	8 /16	13×3	SSOP28
VK16K33AQ	16 /8	8 /16	13×3	QFN28L(4mm×4mm)
VK16K33B	12 /8	8 /12	10×3	SOP24
VK16K33BA	12 /8	8 /12	10×3	SSOP24
VK16K33BQ	12 /8	8 /12	10×3	QFN24L(4mm×4mm)
VK16K33C	8 /8	8 /8	8×3	SOP20
VK16K33CQ	8 /8	8 /8	8×3	QFN20L(3mm×3mm)

Note: For both common cathode and common anode digital tubes, SEG is connected to the anode and GRID to the cathode.

4 Ordering Information

Part No.	Packaging	Tube Qty	Tray(reel)Qty	Box Qty	Total Qty	Notes
VK16K33A	SOP28	26/tube		2080/box	20800 PCS	
VK16K33AA	SSOP28	50/tube		10000/box	100000 PCS	
VK16K33AQ	QFN28L		490/reel	4900/box	29400 PCS	
VK16K33B	SOP24	30/tube		2400/box	24000 PCS	
VK16K33BA	SSOP24	50/tube		10000/box	100000 PCS	
	SSOP24		4000/reel	8000/box	64000 PCS	
VK16K33BQ	QFN24L		490/reel	4900/box	29400 PCS	
VK16K33C	SOP20	36/tube		2880/box	28800 PCS	
VK16K33CQ	QFN20L		490/reel	4900/box	29400 PCS	

5 Package Pinout Information(QFN20L)



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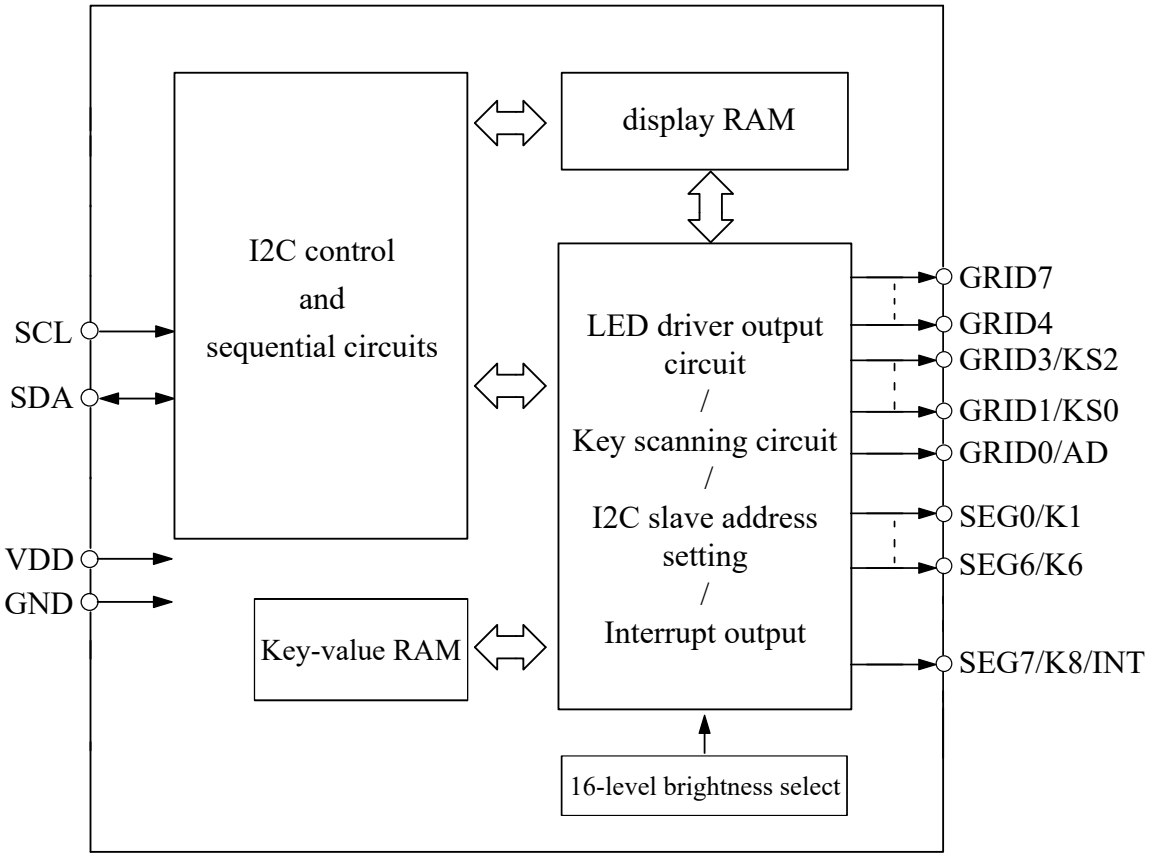
5.1 VK16K33CQ/QFN20L Pin Description

No.	Name	I/O	Function
20	VSS	VSS	Negative power supply
1	GRID0	O	LED GRID output (N-channel open-drain output)
2-4	GRID1/KS0- GRID3/KS2	O	LED GRID output (N-channel open-drain output); Key scan output.
5~8	GRID4 ~GRID7	O	LED GRID output (N-channel open-drain output)
10-16	SEG6/K7- SEG0/K1	I/O	LED SEG output (P-channel); Key scanning input, the key signal is latched after the display cycle ends.
17	SCL	I	The I2C serial clock pin requires an external pull-up resistor
18	SDA	I/O	The I2C serial data input/output pins need to be connected to an external pull-up resistor
19	VDD	VDD	Positive power supply
8	SEG7/K8/INT	I/O	I. When the Bit0 of the SEG/INT register is set to "0", this pin serves as the LED SEG output (P-channel driver) and the input for key scanning. The key signal is latched after the display cycle ends. II. When the Bit0 of the SEG/INT register is set to "1", this pin is an interrupt (INT) output. When the Bit1 of the SEG/INT register is set to "0", the INT output is valid at a low level. When the Bit1 of the SEG/INT register is set to "1", the INT output is valid at a high level III. The button function and the INT function for this pin are mutually exclusive and only one can be selected at a time.

6 Functional Description

6.1 Block Diagram



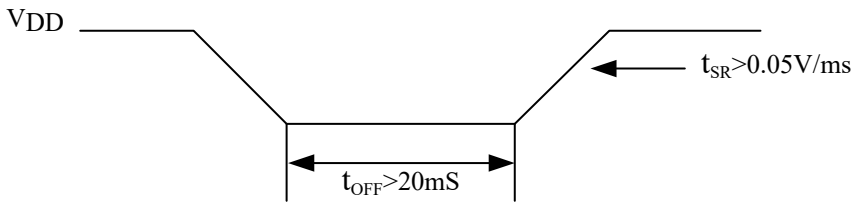
6.2 Power-On Reset

After power-on, the chip is initialized through the internal power-on reset circuit. Within 1ms after power-on reset, I2C data transmission is avoided. The state after initialization is as follows:

- The system oscillator is turned off
- GRID0 to GRID3 output VDD
- GRID4 to GRID7 output high impedance
- All SEG pins are input pins
- The LED display is turned off
- Button scanning stops
- Set the SEG/INT pin to SEG output
- The display brightness is 16/16 Duty.

For a power-on reset to be triggered during operation (e.g., if VDD drops below the specified minimum operating voltage), the following condition must be met: VDD must fall to 0V and remain there for at least 20ms before rising to the normal operating voltage.

Power-on reset sequence



6.3 Standby Mode And Wake-up

Standby mode

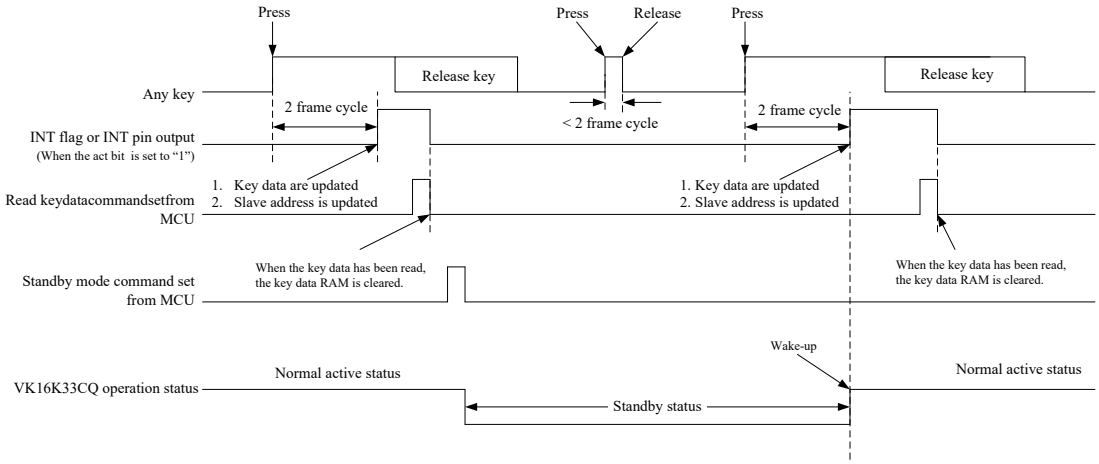
In standby mode, apart from system setting commands, the VK16K33CQ does not accept any input commands and cannot write data to the display RAM. If the system sets the Bit0 of the register to "0", it enters the standby mode.

The status in standby mode is as follows:

- The system oscillator is turned off.
- GRID0 to GRID3 output VDD.
- GRID4 to GRID7 output high impedance.
- The LED display is off.
- Button scanning stops.
- All key data and the INT flag bit are reset to zero until the standby mode is lifted.
- If any key is pressed or the system setting register Bit0 is set to 1, the standby mode is lifted and the chip is awakened.
- In standby mode, all SEG pins are set to input state, unless the SEG/INT pin is configured as an INT output.
- If the Bit0 in the SEG/INT register is set to 1, all SEG pins are set as inputs except for the SEG/INT pin which is set as an INT output.
- If the Bit1 in the SEG/INT setting register is set to 0, the INT pin maintains a high-level output.
- If the Bit1 bit in the SEG/INT setting register is set to 1, the INT pin maintains a low-level output.

Wake up

- The chip can be awakened by pressing a valid key or setting the system setting register Bit0 to 1, and then the key scan can be performed.
- The system oscillator has started to work normally.
- In standby mode, the VK16K33A can still be written with any command, and the last command will be executed after it is awakened. The relationship between pressing a key and the wake-up action is shown in the following figure.



6.4 Display RAM- Storage Structure

The static display memory (RAM) has a structure of 16×8 bits and stores the displayed data. The content of RAM is directly mapped to the display content of the LED driver, with the display address ranging from 0x00 to 0x0F, and there are a total of 16 display units.

If you want to turn on or off a certain LED, simply set the corresponding display RAM position to 1 or clear it to 0:

For instance, to control the on/off of LED1 driven by pin SEG0 and pin GRID0, simply set the Bit0 position of the corresponding display RAM (address 0x00) to 1 or clear to 0.

The process of mapping the contents in RAM to leds is shown in the following table:

SEG / GRID	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	Addr	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	Addr	SEG / GRID
GRID0									0x01								LED1	0x00	GRID0
GRID1									0x03									0x02	GRID1
GRID2									0x05									0x04	GRID2
GRID3									0x07									0x06	GRID3
⋮				⋮					⋮				⋮					⋮	⋮
GRID7									0x0F									0x0E	GRID7
	D7	D6	D5	D4	D3	D2	D1	D0		D7	D6	D5	D4	D3	D2	D1	D0		

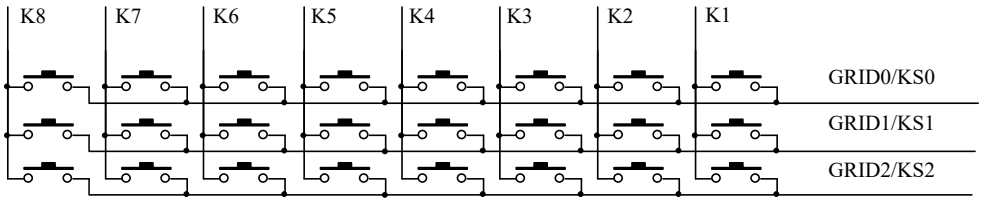
Note:

The content of the display RAM at power-on is undefined. It is recommended to initialize the display RAM by writing 0x00 to all 16 addresses (0x00-0x0F) after power-up.

The SEG pin can only be connected to the anode of the LED, and the GRID pin can only be connected to the cathode of the LED. They must not be reversed.

7 Key Scanning

7.1 Key Data Reading



Key scanning is automatically completed by the hardware, and users only need to read the key values through I2C. When a key is pressed, an INT interrupt is generated. This interrupt flag can be read via I2C or output through the INT pin (open-leak output). Within one key scanning cycle, the total debouncing time for 30 (10x3) key scans is at least 20ms. An INT interrupt will be generated when one or more keys that were not pressed in the previous scanning period are scanned within the sampling period. During each debouncing cycle, the key scanning circuit will detect the number of keys pressed simultaneously (supporting multiple keys pressed at the same time).

When all key data has been read, the key data RAM is cleared and the INT flag bit is reset to "0". If the SEG/INT pin is set to INT output, the INT pin returns to the level when no key was pressed.

INT flag bit register:

INT register address	INT								Function Description
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	There is a key press sign
0x60	INT flag bit	INT flag bit	INT flag bit	INT flag bit	INT flag bit	INT flag bit	INT flag bit	INT flag bit	The INT flag is set to '1' upon any key press. It is cleared to '0' after all key data is read.

Key value RAM address and corresponding key:

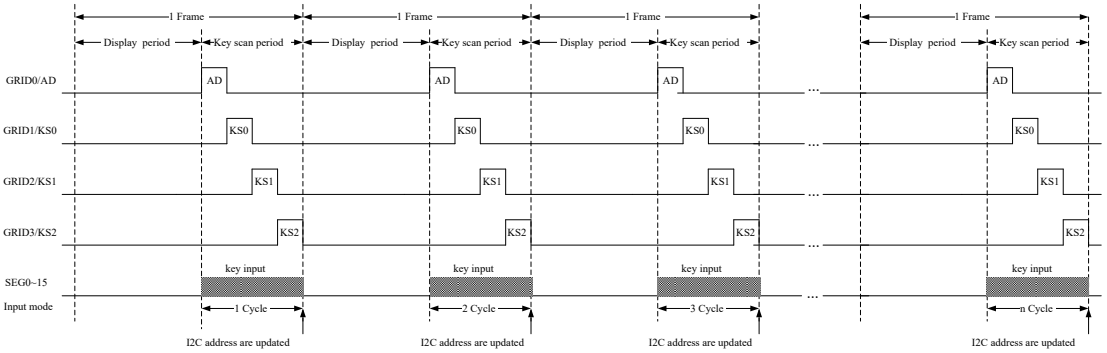
Key value RAM address	....							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x40	KS0/K8	KS0/K7	KS0/K6	KS0/K5	KS0/K4	KS0/K3	KS0/K2	KS0/K1
0x41	0	0	0	0	0	0	0	0
0x42	KS1/K8	KS1/K7	KS1/K6	KS1/K5	KS1/K4	KS1/K3	KS1/K2	KS1/K1
0x43	0	0	0	0	0	0	0	0
0x44	KS2/K8	KS2/K7	KS2/K6	KS2/K5	KS2/K4	KS2/K3	KS2/K2	KS2/K1
0x45	0	0	0	0	0	0	0	0

Note:

It is recommended to only perform read operations on the key-value RAM and read the data from address 0x40 to 0x45 in sequence starting from address 0x40.

7.2 Key Scan Timing

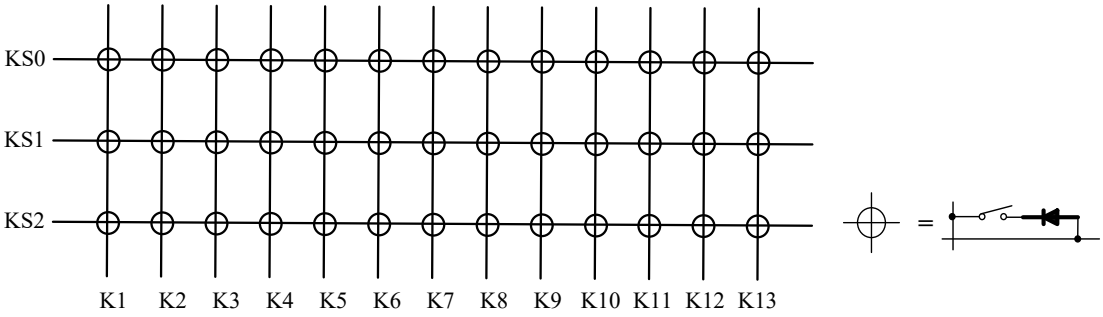
The key scanning sequence is shown in the figure:



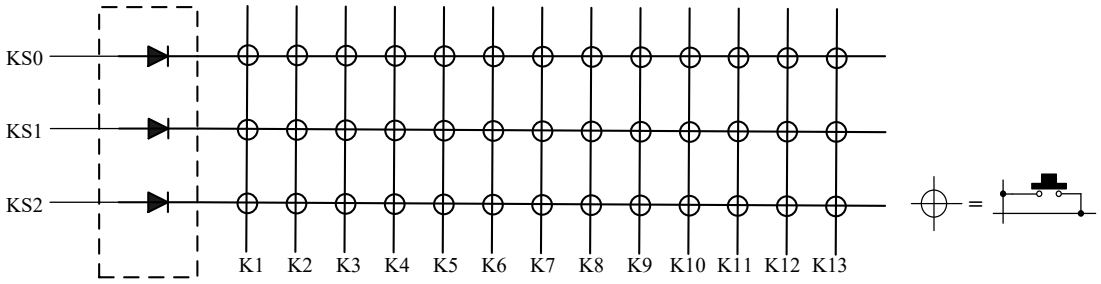
Note: The I2C slave address is updated during the key scan cycle.

7.3 Combined Key Circuit

When the number of keys pressed simultaneously is ≥3, a diode needs to be connected in series with each combination key, as shown in the following figure:



When the number of keys pressed simultaneously is ≤2, a diode needs to be connected in series with the KS0-KS2 keys, as shown in the following figure:



Note:

This circuit does not allow three or more keys to be pressed simultaneously; otherwise, the keys may not be correctly recognized.

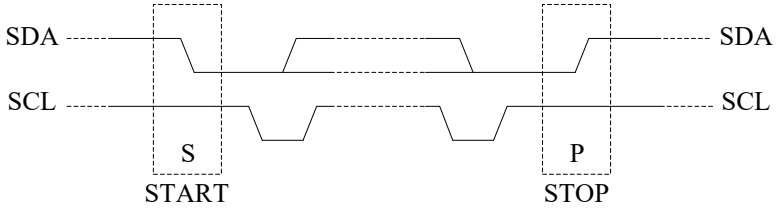
8 Communication Commands

8.1 I2C Communication Interface

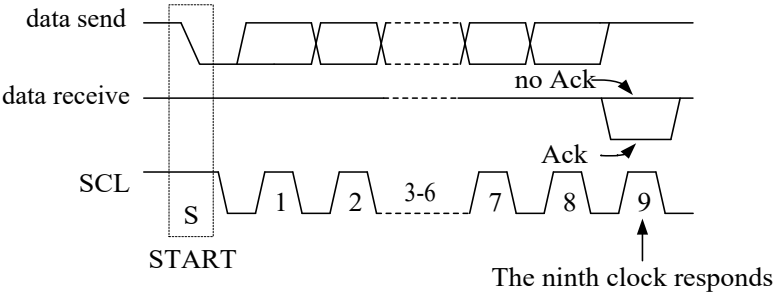
The VK16K33CQ has two communication pins and follows the I2C protocol.

The SCL pin is the clock input pin, and the SDA pin is the serial data input/output pin. When the I2C bus is idle, both of these pins are at a high level. The data on the SDA line must remain stable at high levels of the clock. The clock signal on the SCL line can only be changed when it is at a low level. When the SCL signal is at a high level and the SDA signal changes from a high level to a low level, the data cable starts to work or resumes work. When the SCL signal is at a high level and the SDA signal changes from a low level to a high level, it stops working.

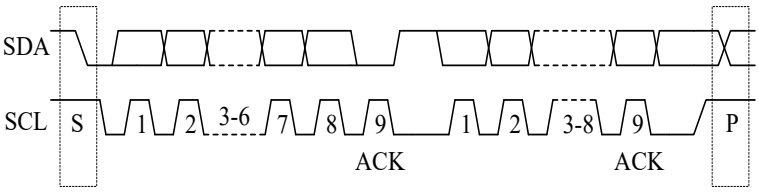
START and STOP



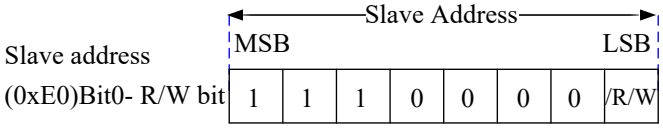
Acknowledge



Byte Format



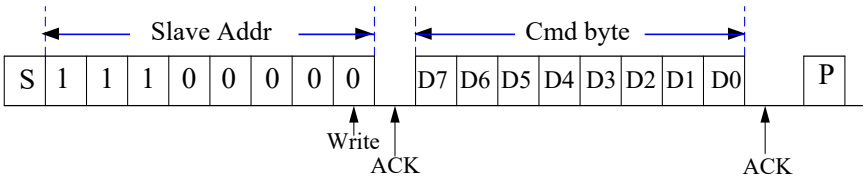
9 I2C Address



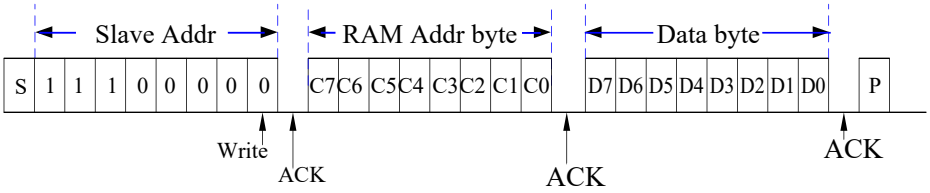
9.1 I2C Command Format

Write operation

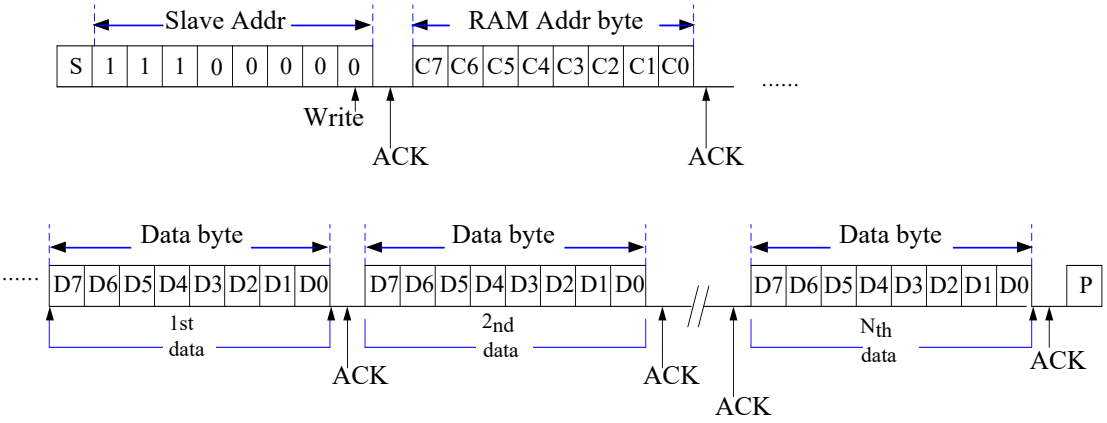
Write commands



Write a single byte of data to display RAM

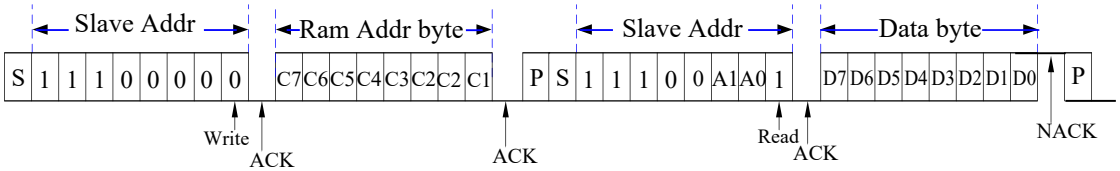


Write multiple bytes of data to the display RAM

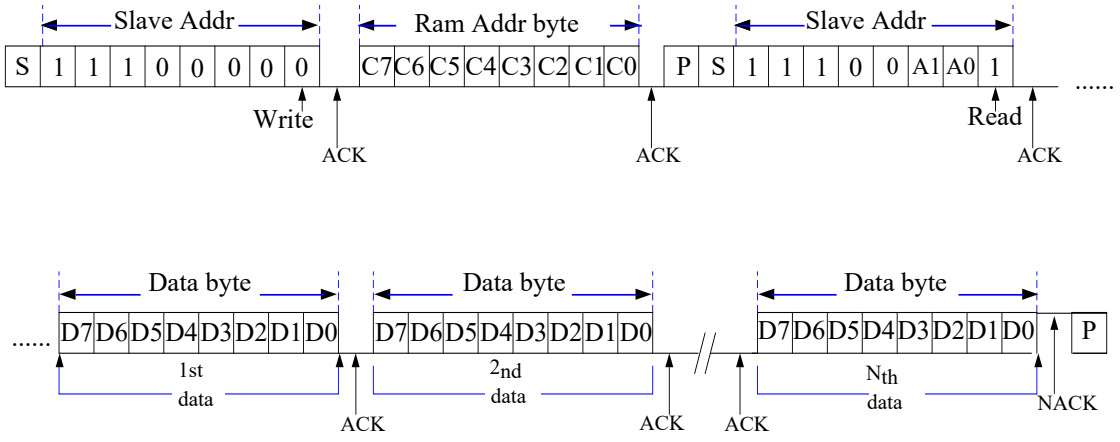


9.2 Read Operation

Reading a data byte does not apply to reading key values.



When reading N bytes, the address pointer automatically increments by 1 upon receiving the ACK from the host. When reading the key, the address starts from 0x40 and continuously reads 6 pieces of data.



10 Command Description

10.1 System Settings Commands

This command is used to set the working mode of the chip: normal mode or standby mode.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Function	Note	Default
0	0	1	0	X	X	X	0	System oscillator	Standby mode(oscillator off)	0x20
0	0	1	0				1	On/Off	Normal mode(with the oscillator on)	

10.2 Display Setting Commands

This command is used to set the on/off of the LED display and the overall flashing frequency of the LED.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Function	Note	Default
1	0	0	0	X			0	Show on/off	Show off	0x80
1	0	0	0				1		Display on	
1	0	0	0	X	0	0		Flickering frequency	Flashing off	0x80
1	0	0	0		0	1			2Hz	
1	0	0	0		1	0			1Hz	
1	0	0	0		1	1			0.5Hz	

10.3 SEG/INT Pin Function Setting Command

This command is used to set the output function of the INT/SEG pin.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Function	Note	Default
1	0	1	0	X	X	0	0	INT/SEG pin function selection and INT pin output level setting	Set to SEG output	0xA0
1	0	1	0			0	1		Set to INT output, active low	
1	0	1	0			1	1		Set to INT output, active high	

10.4 Display Address Setting Command

This command is used to set the address of the display RAM (0x00-0x0F). When powered on, the address is set to 0x00 by default.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Display RAM address
0	0	0	0	0	0	0	0	0x00
0	0	0	0	0	0	0	1	0x01
0	0	0	0	0	0	1	0	0x02
0	0	0	0	0	0	1	1	0x03
0	0	0	0	0	1	0	0	0x04
0	0	0	0	0	1	0	1	0x05
0	0	0	0	0	1	1	0	0x06
0	0	0	0	0	1	1	1	0x07
0	0	0	0	1	0	0	0	0x08
0	0	0	0	1	0	0	1	0x09
0	0	0	0	1	0	1	0	0x0A
0	0	0	0	1	0	1	1	0x0B
0	0	0	0	1	1	0	0	0x0C
0	0	0	0	1	1	0	1	0x0D
0	0	0	0	1	1	0	1	0x0E
0	0	0	0	1	1	1	1	0x0F

10.5 Display Brightness Setting Command

This command is used to set the display brightness (level 16).

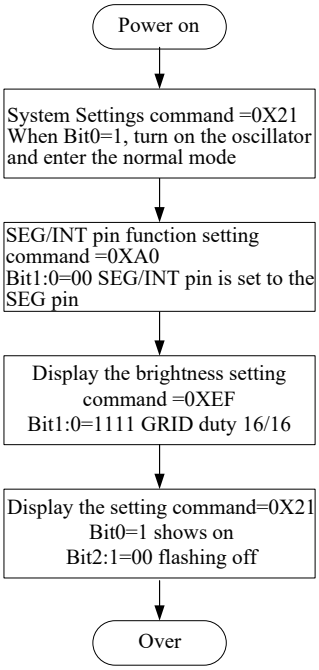
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Function	Note
1	1	1	0	0	0	0	0	Set the GRID pulse width	Set the pulse width to 1/16
1	1	1	0	0	0	0	1		Set the pulse width to 2/16
1	1	1	0	0	0	1	0		Set the pulse width to 3/16
1	1	1	0	0	0	1	1		Set the pulse width to 4/16
1	1	1	0	0	1	0	0		Set the pulse width to 5/16
1	1	1	0	0	1	0	1		Set the pulse width to 6/16
1	1	1	0	0	1	1	0		Set the pulse width to 7/16
1	1	1	0	0	1	1	1		Set the pulse width to 8/16
1	1	1	0	1	0	0	0		Set the pulse width to 9/16
1	1	1	0	1	0	0	1		Set the pulse width to 10/16
1	1	1	0	1	0	1	0		Set the pulse width to 11/16
1	1	1	0	1	0	1	1		Set the pulse width to 12/16
1	1	1	0	1	1	0	0		Set the pulse width to 13/16
1	1	1	0	1	1	0	1		Set the pulse width to 14/16
1	1	1	0	1	1	1	0		Set the pulse width to 15/16
1	1	1	0	1	1	1	1		Set the pulse width to 16/16

11 Command Application

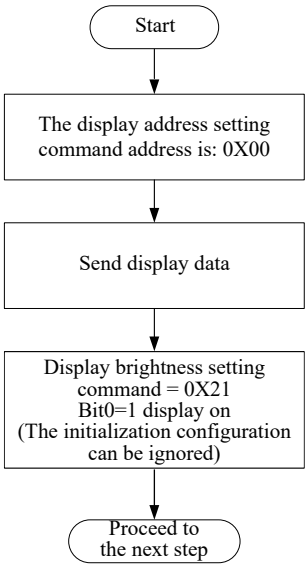
11.1 Initialize Configuration

When powering on, the power-on reset sequence must be met. After power-on, parameters need to be configured first.

The initial parameters are configured through a series of commands, and the command sequence is as shown in the following figure:

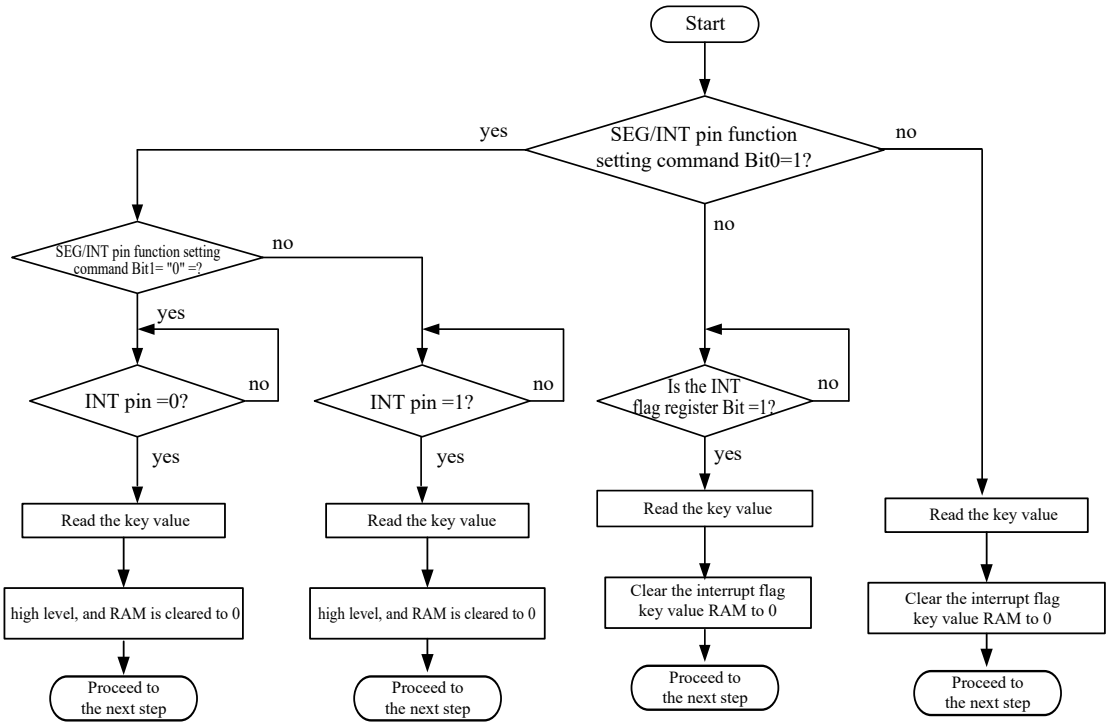


11.2 Display Data Write Command Sequence



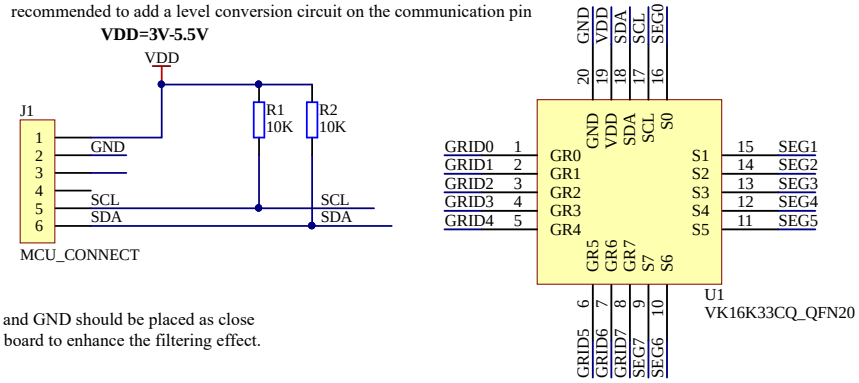
11.3 Key-value read Command sequence

It is recommended to only perform read operations on the key data RAM and start from address 0x40. Each read operation should sequentially read the data from address 0x40 to 0x45.

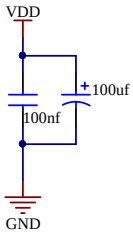


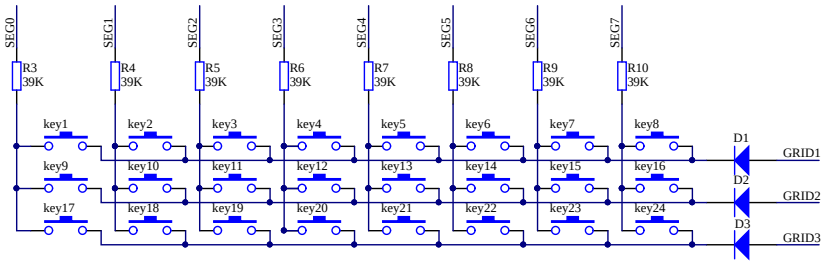
12 Application Circuits

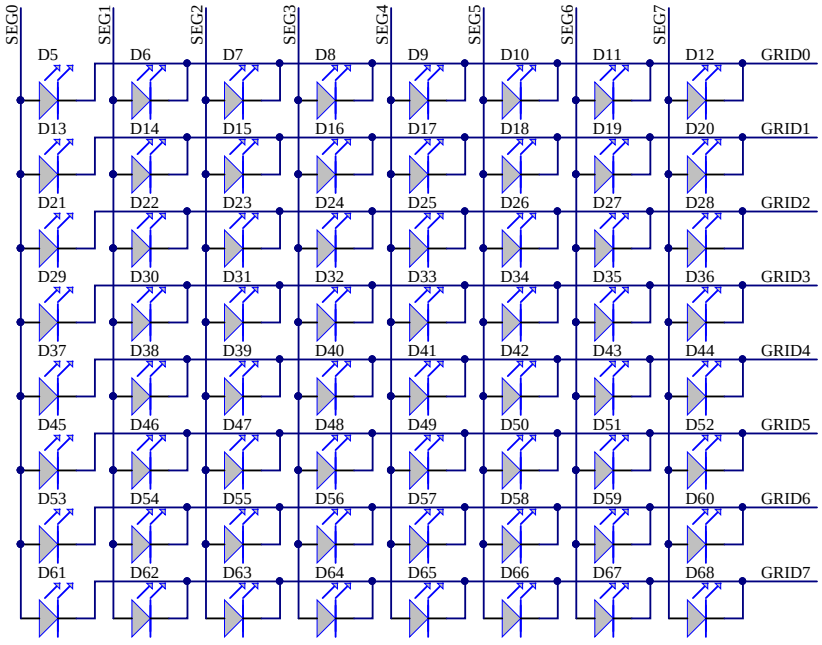
When the surrounding interference is relatively large, a 10R to 10k resistor and a PF-level small capacitor to ground can be connected in series on the communication pin. When the power supply of the single-chip microcomputer (3.3V) and the driver chip (5V) is inconsistent, it is recommended to add a level conversion circuit on the communication pin



The filter capacitor between VDD and GND should be placed as close to the chip as possible on the PCB board to enhance the filtering effect.







Connect the SEG pin to the anode of the LED and the GRID pin to the cathode of the LED

13 Electrical Characteristics

13.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	V_{SS}-0.3V to V_{SS}+6.5	V
Input Voltage	VIN	V_{SS}-0.3V to V_{DD}+0.3	V
Storage Temperature	T_{STG}	-50～+120	℃
Operating Temperature	T_{OTG}	-40～+85	℃

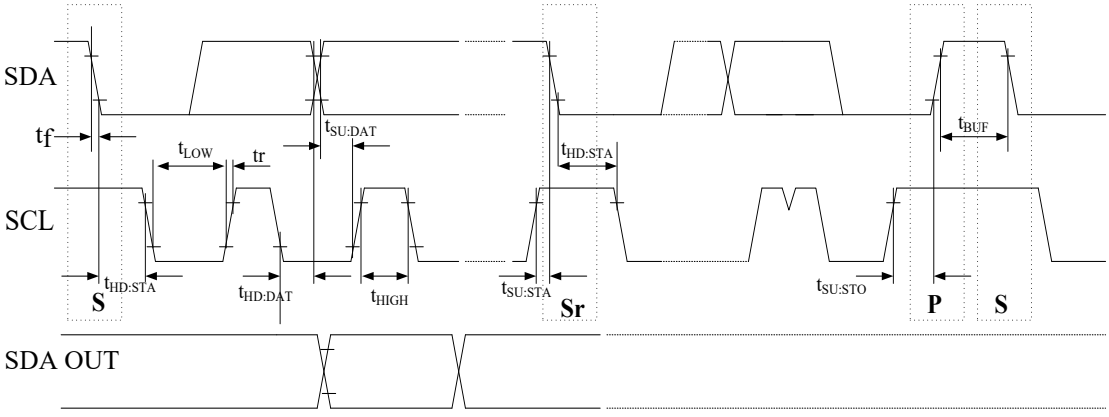
13.2 DC Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition	
						VDD	Condition
VDD	Supply voltage	3.0	5	5.5	V	-	-
IDD	Working current	-	1	2	mA	5	No-load, normal operation, with the SEG/INT terminal set to 0
I_{STB}	Standby current	-	1	10	μA	5	No-load, standby mode
V_{IH}	High-level Input	0.7_{VDD}	-	VDD	V	5	SDA,SCL
V_{IL}	Low-level Input	0	-	0.3_{VDD}	V	5	SDA,SCL
I_{IL}	Input leakage current	-1	-		μA	-	V_{IN} = V_{SS} or V_{DD}
R_{PL}	Input pull-down resistor	250		-	KΩ	5	SEG0/K1~SEG7/K8, During the key scan
I_{OL1}	Low-level output current	6	-	-	mA	5	V_{OL}=0.4V; SDA
I_{OL2}	SEG source current	6	-	-	mA	5	V_{OL}=0.4V,INT Pin
I_{OH1}	SEG source current	-20	-25	-40	mA	5	V_{OH}=V_{DD}-2V,(SEG0~SEG7)
		-25	-30	-50	mA		V_{OH}=V_{DD}-3V,(SEG0~SEG7)
I_{TOLSEG}	High-level output current tolerance	-	-	5	%	5	V_{OH}=V_{DD}-3V,(SEG0~SEG7)
I_{OL3}	GRID sink current	160	200	-	mA	5	V_{OL}=0.3V,(GRID0~GRID7pin)
I_{OH2}	GRID source current	-20	-25	-40	mA	5	V_{OH}= VDD-2V, (GRID0~GRID3 pin)

13.3 AC Electrical Characteristics

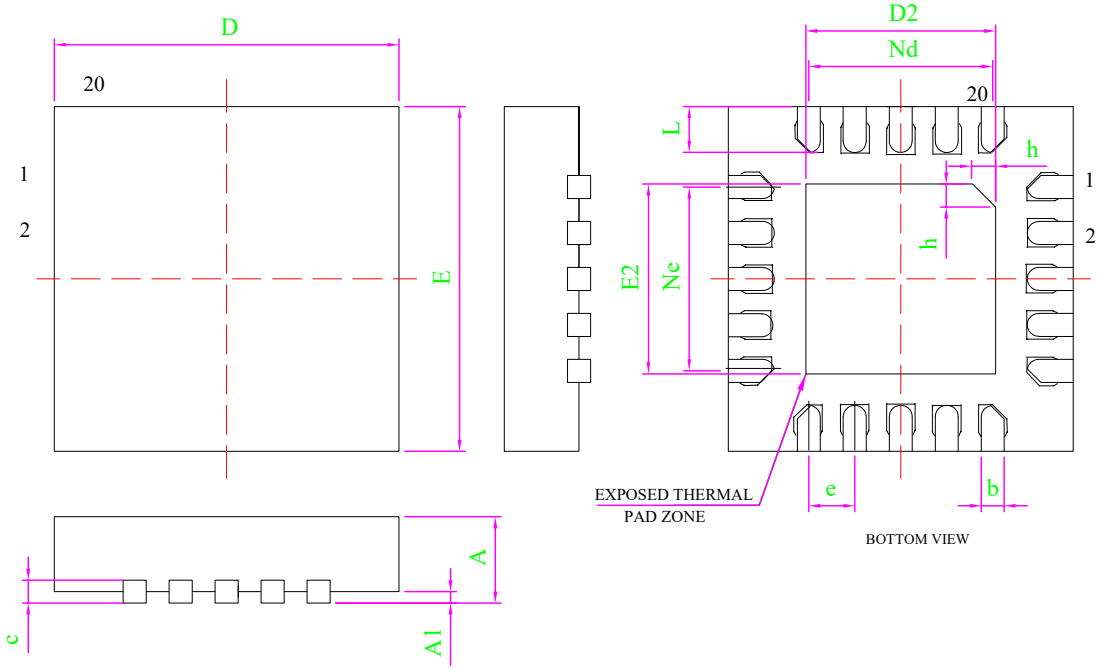
Symbol	Parameter	Min.	Max.	Unit	Test Condition Condition
f_{SCL}	Clock frequency	-	400	kHZ	—
t_{BUF}	Bus idle time	1.3	-	μs	During this period, the bus must remain idle until a new transmission begins
$t_{HD;\ STA}$	Start-up condition holding time	0.6	-	μs	After this period, the first clock pulse will be generated
t_{LOW}	SCL low-level time	1.3	-	μs	—
t_{HIGH}	SCL high-level time	0.6	-	μs	—
$t_{SU;\ STA}$	Set the time for the Star status	0.6	-	μs	It is only related to the repeated START signal
$t_{HD;\ DAT}$	Data retention time	0	-	μs	—
$t_{SU;\ DAT}$	Data setting time	100	-	ns	—
t_r	Rising time	-	0.3	μs	Periodic sampling
t_f	Decrease time	-	0.3	μs	Periodic sampling
$t_{SU;\ STO}$	Stop setting the time for the condition	0.6	-	μs	—
t_{AA}	The effective clock output time	-	0.9	μs	—
t_{SP}	Input filter time constant (SDA and SCL pins)	-	50	ns	Noise suppression time

I²C Timing



14 Package Information

14.1 QFN20L(3.0mm×3.0mm×0.75mm-0.40mm)



MILLIMETER			
SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e	0.40BSC		
Ne	1.60BSC		
Nd	1.60BSC		
E	2.90	3.00	3.10
E2	1.55	1.56	1.75
L	0.35	0.40	0.45
h	0.20	0.25	0.30
L/F carrier size（Mil）	75*75		

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16 Revision History

No.	Version	Date	Modify the content	Check
1	1.0	2022-08-09	Initial release	YES
2	1.1	2025-11-03	Change Description	YES

[1] Please refer to the latest version of this document before starting or finalizing any design.

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