永嘉微电
Vinka Microelectronics

VK16D33AQ Datasheet

8×16 Constant Current LED Driver

Rev.1.1

1 General Description

VK16D33AQ is a dedicated chip for constant current digital tube or dot matrix LED driver control, integrating circuits such as a data latch and an LED constant current driver module internally. The bit number of scanning can be adjusted through register configuration to obtain a larger single-point driving current. The data communicates with the MCU through the I2C communication interface. The SEG pin is connected to the anode of the LED, and the GRID pin is connected to the cathode of the LED, which can support dot matrix LED display panels ranging from 8SEG×1GRID to 8SEG×16GRID. It adopts the QFN28L packaging form and is suitable for driving small LED display screens.

Compared with the traditional LED display panel driver chips, when the number of lit LED changes or the input voltage varies, the current of a single LED will change, thereby affecting the display brightness. It adopts a constant current design. Once the display mode is configured, the current of each LED remains constant and will not fluctuate due to changes in the number of lit LED or input voltage.

2 Key Features

- Operating voltage:3.0-5.5V
- Integrated RC oscillator
- 8 SEG and 16 GRID（can be selected from 1 to16）
- SEG pins connect to LED Anode , GRID pins connect to LED Cathode
- I2C communication interface
- 16 levels of overall brightness adjustable (SEG constant current setting 16 levels)
- The built-in display RAM is 8×16 bits
- Built-in power-on reset circuit
- Output constant current
- It has a large driving current and is suitable for high-brightness display applications
- Available Packages:
  QFN28L(4.0mm × 4.0mm PP= 0.40mm)

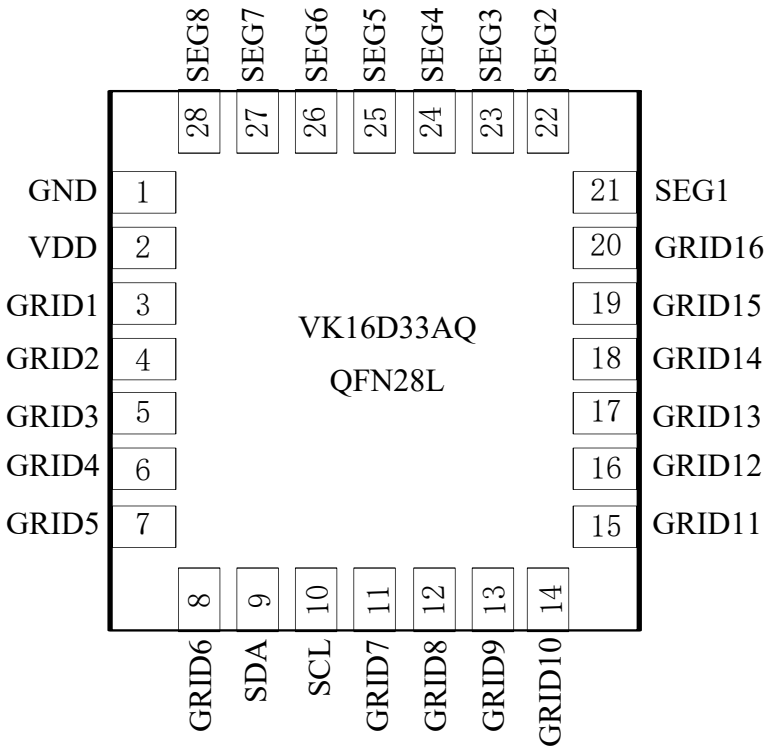
3 Product Selection

Part No.	VK16D32	VK16D32AQ	VK16D33	VK16D33AA	VK16D33AQ	VK16D33Q
Max. LED	96	96	128	128	128	128
SEG/GRID	8/12	8/12	8/16	8/16	8/16	8/16
Packaging	SSOP24	QFN24L	SOP28	SSOP28	QFN28L	QFN32L

4 Ordering Information

Part No.	Packaging	Tube Qty	Tray Qty	Box Qty	Total Qty	Notes
VK16D32	SSOP24	50/tube		10000/box	100000PCS	
VK16D32AQ	QFN24L		490/tray	4900/box	29400PCS	
VK16D33	SOP28	26/tube		2080/box	20800PCS	
VK16D33AA	SSOP28		4000/tray	8000/box	64000PCS	
VK16D33AQ	QFN28L		490/tray	4900/box	29400PCS	
VK16D33Q	QFN32L		490/tray	4900/box	29400PCS	

5 Package Pinout Information(QFN28L)



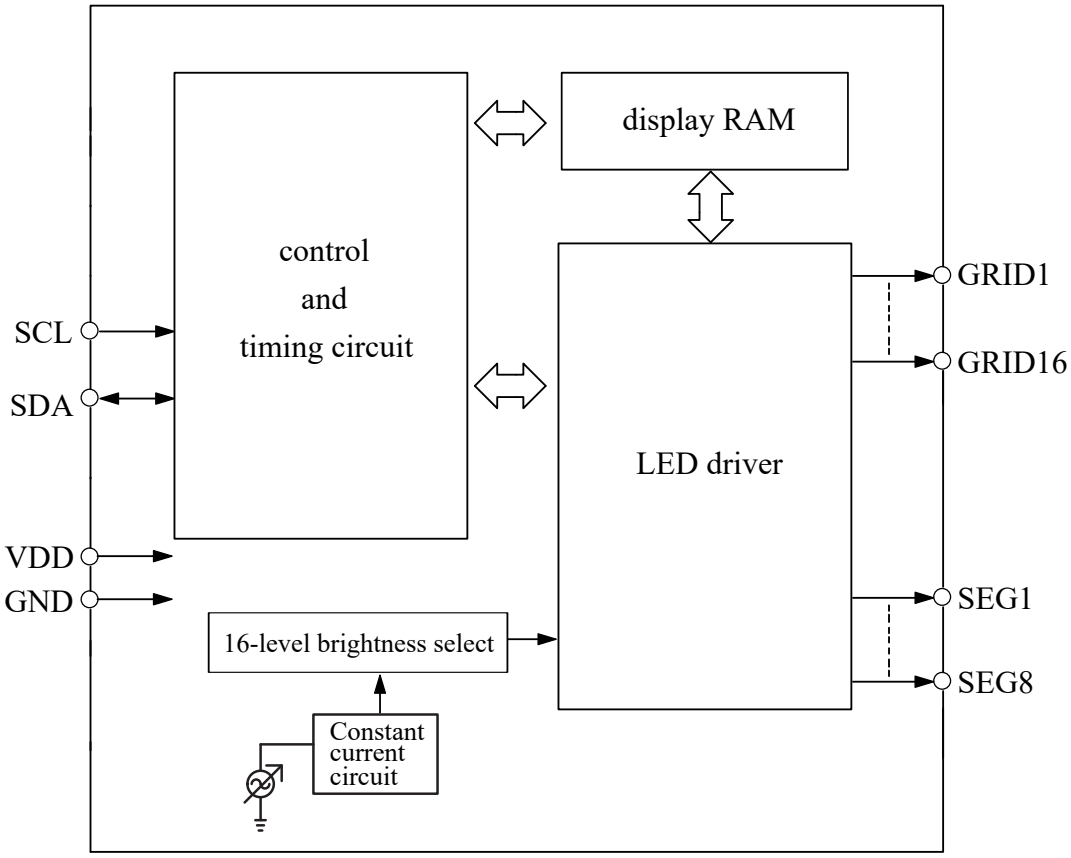
For more information: Page 16

5.1 VK16D33AQ/QFN28 Pin Description

No.	Name	I/O	Function
21~28	SEG1~SEG8	O	LED SEG drive outputs
1	GND	GND	Negative power supply
2	VDD	VDD	Positive power supply
3~8 11~20	GRID1 ~GRID6 GRID7~GRID16	O	LED GRID drive outputs
9	SDA	I/O	The I2C serial data input/output pins need to be connected to an external pull-up resistor
10	SCL	I	The I2C serial clock pin requires an external pull-up resistor

6 Functional Description

6.1 Block Diagram



6.2 Display RAM

The static display memory (RAM) has a structure of 8×16 bits and stores the displayed data. The content of RAM is directly mapped to the display content of the LED driver, with the display address ranging from 0x00 to 0x0F, and there are a total of 16 display units. If you want to turn on or off a certain LED, simply set the corresponding display RAM position to 1 or clear to 0. For example, to control the on/off of LED1 driven by pins SEG1 and GRID1, simply set the Bit0 position of the display RAM (address 0x00) to 1 or clear to 0.

The process of mapping the contents in RAM to LED is shown in the following table:

SEG / GRID	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	Address
GRID1								LED1	0x00
GRID2									0x01
GRID3									0x02
GRID4									0x03
GRID5									0x04
GRID6									0x05
⋮									⋮
GRID14									0x0D
GRID15									0x0E
GRID16									0x0F
	D7	D6	D5	D4	D3	D2	D1	D0	

Note:

1. The value stored inside the chip display RAM at the moment of power-on may be random. It is recommended that the customer perform a power-on reset of the display RAM, that is, write all the data 0x00 to the 16-bit memory address (0x00-0x0F) after power-on.
2. The SEG pin can only be connected to the anode of the LED, and the GRID pin can only be connected to the cathode of the LED. They must not be reversed.

7 I2C Communication Command

7.1 I2C Communication Interface

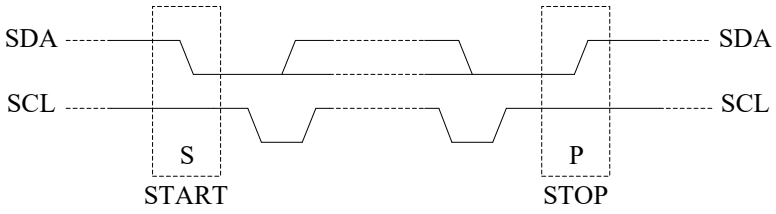
The VK16D33AQ has two communication pins and follows the I2C protocol, with a maximum communication speed of 400kbit/S.

The SCL pin is the clock input pin, and the SDA pin is the serial data input/output pin, which requires an external pull-up resistor.

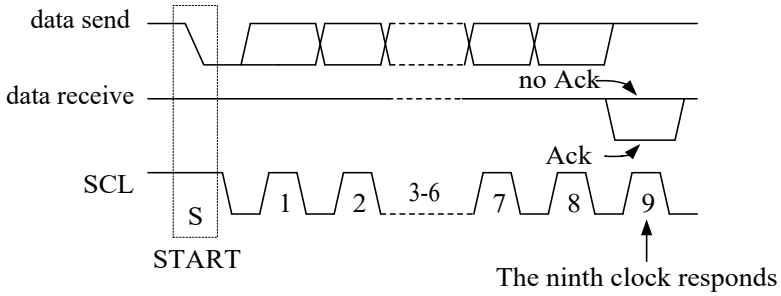
When the I2C bus is idle, both pins are at a high level. When the SCL signal is at a high level and the SDA signal changes from a high level to a low level, the operation starts or resumes. Conversely, when the SCL signal is at a high level and the SDA signal changes from a low level to a high level, the operation stops.

When the SCL signal is at a high level, the data on the SDA port is all valid and stable. Only when the SCL signal is at a low level can the level on the SDA port be changed.

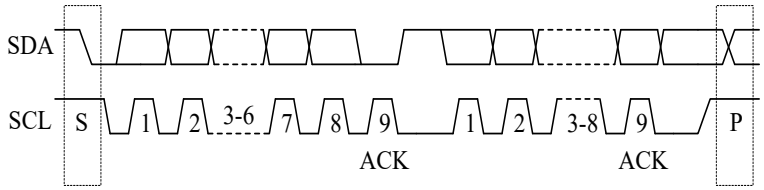
START and STOP



Acknowledge



Byte Format



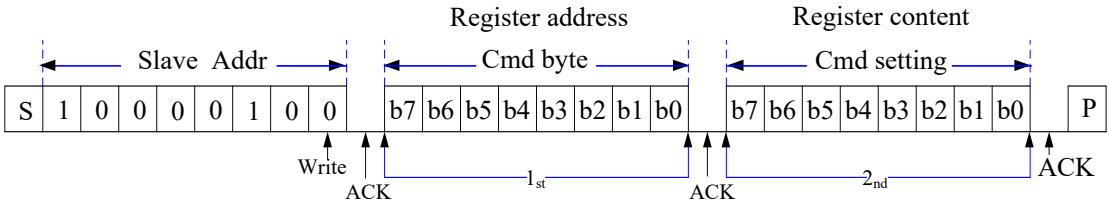
Slave Address (0x84) bit0-R/W

1	0	0	0	0	1	0	0

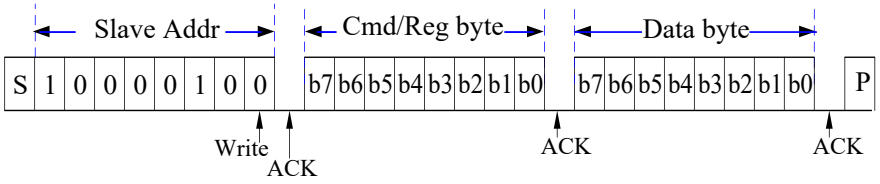
7.2 I2C Command Format

Write Operation

Write Command



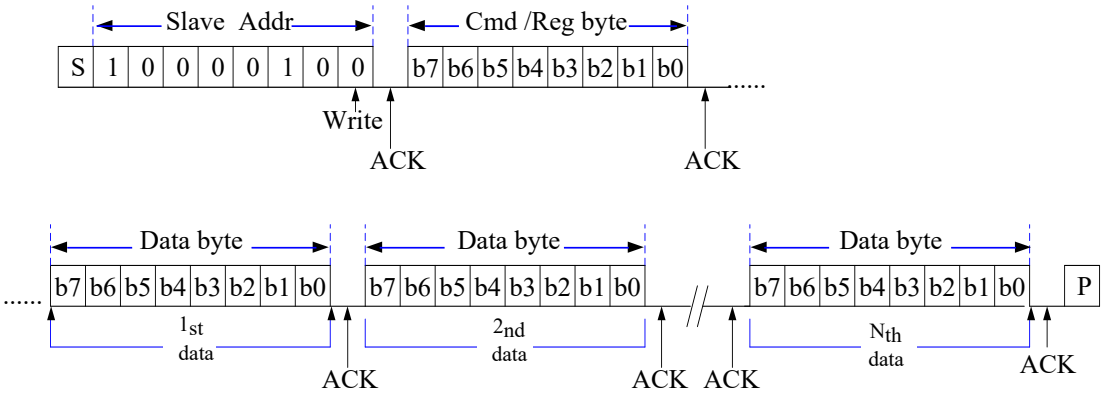
Write a single byte of data to display RAM



Note:

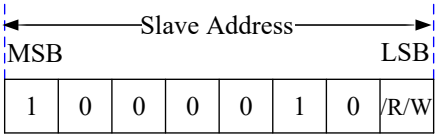
If the byte after the Slave address is a command code, the byte after the command code is ignored.

Write multiple bytes of data to the display RAM



7.3 Command Description

Slave Address
(0x84) Bit0-R/W



After power on, the status control command（register 0x12) needs to be configured to 0x01 (work state).

Command(Register) writing sequence:

State control command → Display data command → Display control command → status control command.

Note：Once bit0 of the State control register is configured as "0", when rewriting data, be sure to configure the State control register to 0x01 before performing other operations.

8 Display Control Command

Select display brightness (16 levels)

Register Address	Register content								Function
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Display brightness level (SEG continuous current)
0x10	--------- 0				1	1	1	1	70mA(default)
					1	1	1	0	65.6mA
					1	1	0	1	61.3mA
						-----			-----
					0	0	0	1	8.75mA
					0	0	0	0	4.37mA

Select number of scan GRID ,default 12GRID.

Register Address	Register content								Function
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	number of scan GRID
0x11	--------- 0				1	0	1	1	16GRID(default)
					1	0	1	0	15GRID
					1	0	0	1	14GRID
						-----			-----
					0	0	0	0	1GRID

8.1 Status Control Command

Register Address	Register content								Function
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	work state
0x12	--------- 0							0	Shutdown(default)
								1	Normal operation
							0		display off(default)
							1		display on

8.2 Display Data Command

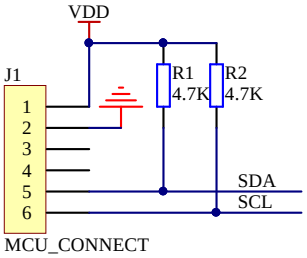
The displayed data addresses range from 0x00 to 0x0F, totaling 16 bytes, corresponding respectively to the LED lights of the matrices connected to the SEG and GRID pins.

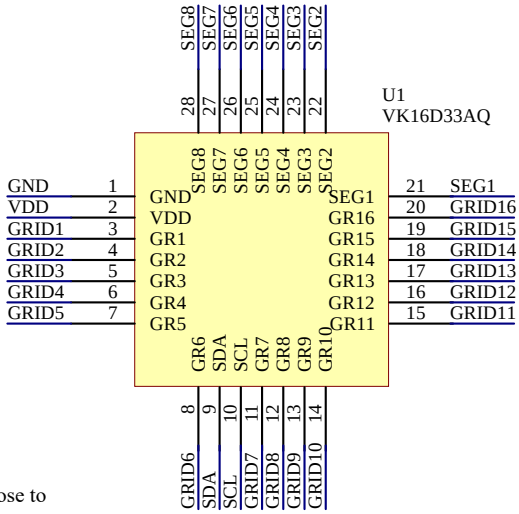
display data address	display content								Function
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	display data
0x00-0x0F	X	X	X	X	X	X	X	X	1 bit control 1 LED (by 1SEG and 1 GRID)

9 Application Circuits

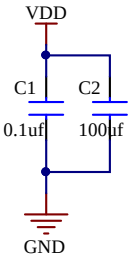
When the surrounding interference is relatively large, a 10R to 10k resistor and a PF-level small capacitor to ground can be connected in series on the communication pin. When the power supply of the single-chip microcomputer (3.3V) and the driver chip (5V) is inconsistent, it is recommended to add a level conversion circuit on the communication pin

VDD=3V-5.5V

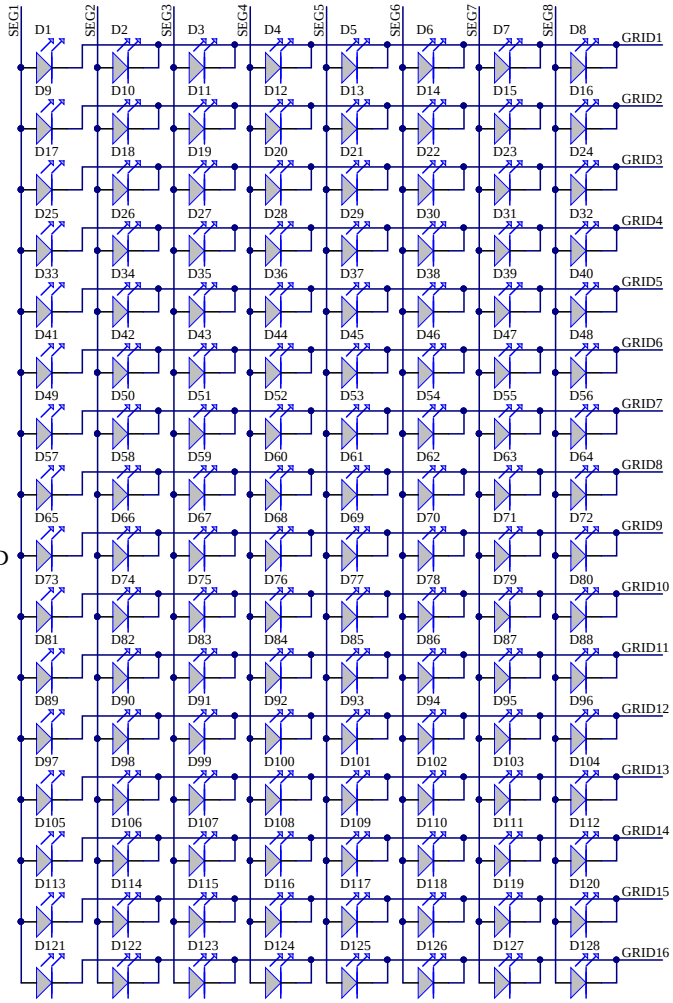




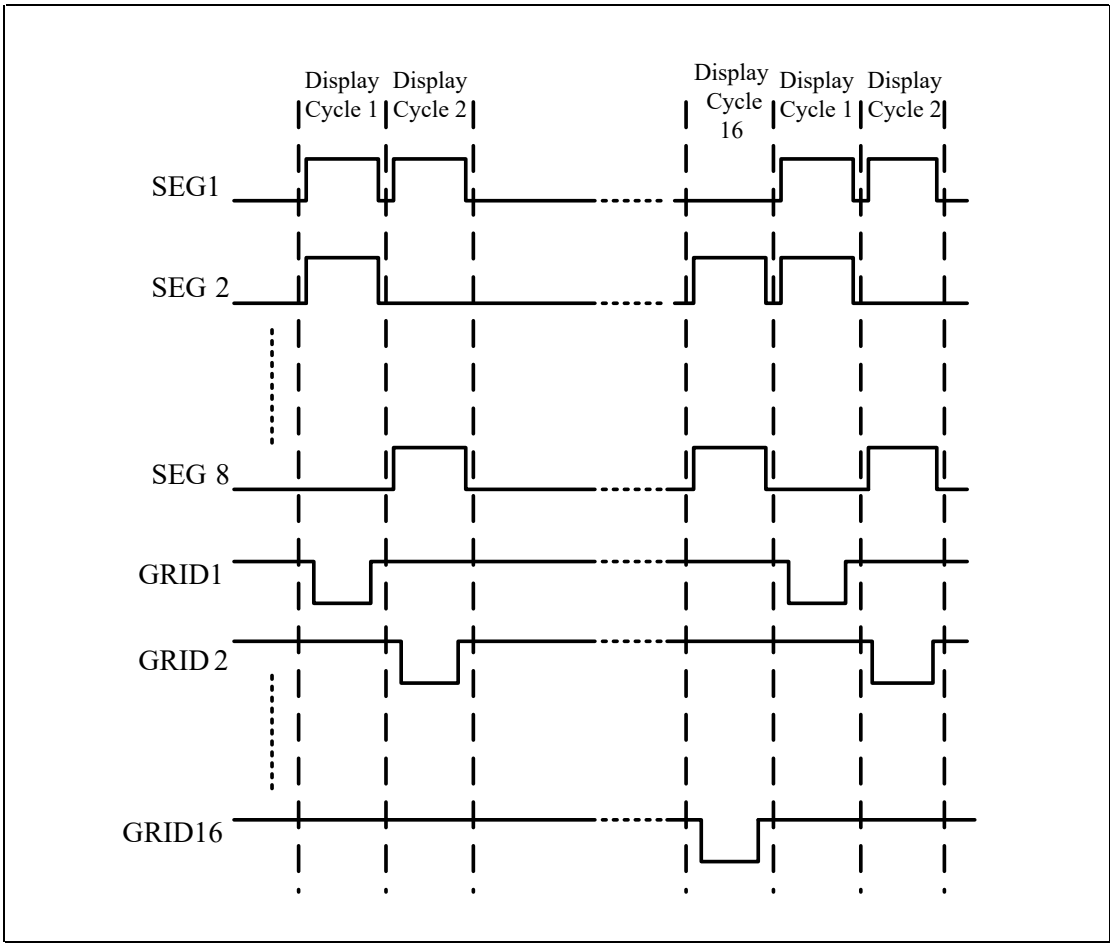
The filter capacitor between VDD and GND should be placed as close to the chip as possible on the PCB board to enhance the filtering effect.



Connect the SEG pin to the anode of the LED and the GRID pin to the cathode of the LED



10 Display Cycle



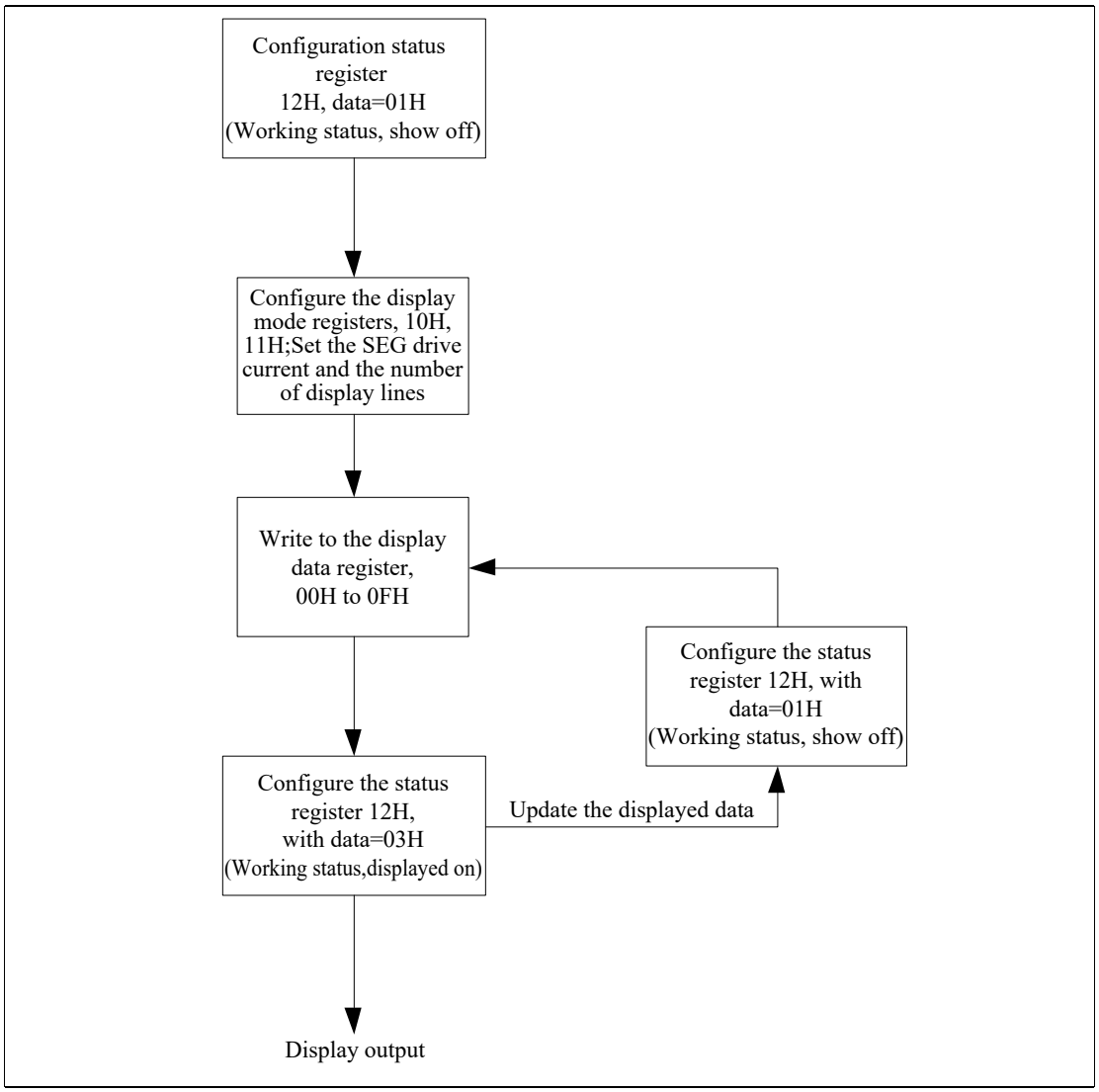
Instruction sequence:

1. For the first power-on, the status control register (i.e. 12H) needs to be configured to 01H (i.e., the circuit enters the working state).

2. Register write sequence: Status control register → Display data register → display mode register → status control register.

Note: Once the Bit0 of the status control register is configured to "0", when rewriting data, the status control register must be configured to 01H first before performing other operations

11 Software Flowchart



12 Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3～6.0	V
Input Voltage	VIN	VSS-0.5～VDD+0.5	V
Drive output current	$I_{OLGRID}\Sigma^{1}16$	+600	mA
	I_{OHSEG}	-77	mA
Power loss	P_D	1500	mW
Storage Temperature	T_{STG}	-65～+150	℃
Operating Temperature	T_{OTG}	-40～+85	℃

12.2 DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
High Level output Current	I_{OHSG}	Vo=VDD-1V SEG1～SEG8	-63	-70	-77	mA
Low Level output Current	I_{OLGOUT}	Vo=0.8V	—	560	—	mA
Input Current	I_{IN}	VI=VDD，SDA，SCL	—	—	±1	uA
High-level Input	V_{IH}	SDA,SCL	$0.7V_{DD}$	—	5	V
Low-level Input	V_{IL}	SDA,SCL	0	—	$0.3V_{DD}$	V
Hysteresis voltage	V_H	SDA,SCL	—	0.35	—	V
Dynamic current loss	I_{DD_DYN}	Noload/LED OFF	—	—	1	mA
shutdown Current	I_{SHUT}	Shutdown enable			10	uA

12.3 AC Electrical Characteristics

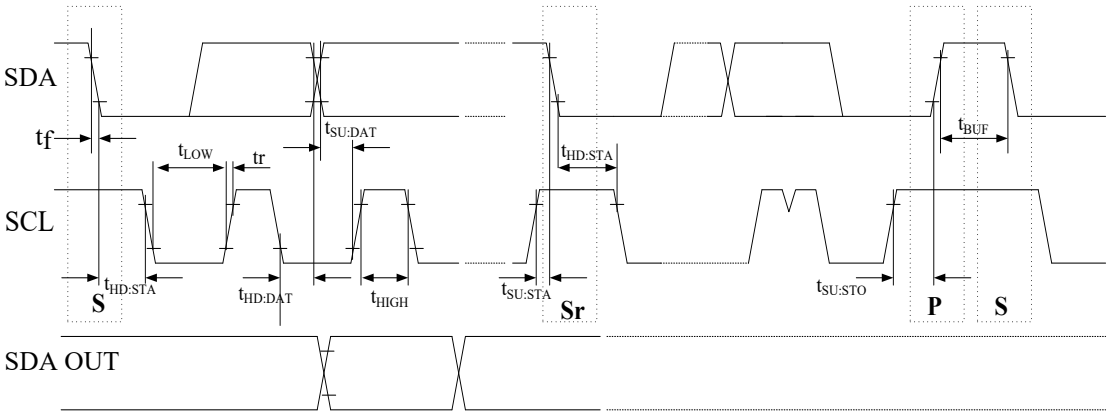
Switch Parameters

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Rising Time	TTZH1	SEG1~8,CL=300pF	—	—	2	us
	TTZH2	GRID1~16,CL=300pF	—	—	0.5	us
Falling Time	TTZH	CL=300pF, SEGn, GRIDn	—	—	120	us

Timing Parameters

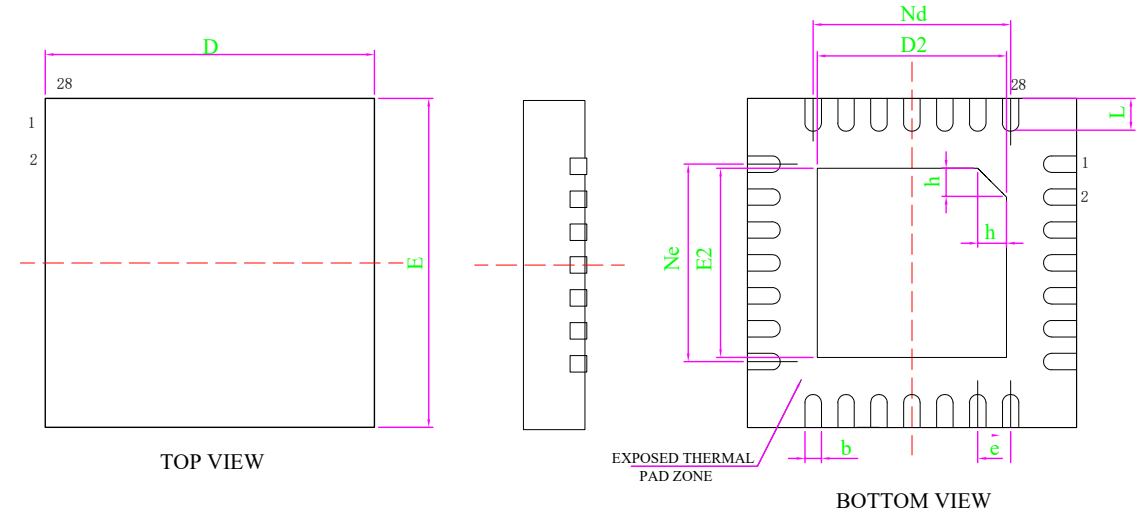
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
SCL clock frequency	F_{SCL}	-	-	400	KHz	
Bus Free Time	t_{BUF}	1.3	-	-	μS	Time in which the bus must be free before a new transmission can start
Start Condition Hold Time	$t_{HD:STA}$	0.6	-	-	μS	After this cycle, the first clock pulse is generated
SCL Low Time	t_{LOW}	1.3	-	-	μS	
SCL High Time	t_{HIGH}	0.6	-	-	μS	
Start Condition Setup Time	$t_{SU:STA}$	0.6	-	-	μS	Only relevant for repeated START condition
Data Hold Time	$t_{HD:DAT}$	-	-	0.9	nS	
Data Setup Time	$t_{HD:DAT}$	100	-	-	nS	
SDA , SCL Rising Time	t_R	20+0.1Cb1	-	-	nS	periodically sampled
SDA,SCL Falling Time	t_F	20+0.1Cb	-	-	nS	periodically sampled
Stop Condition Setup Time	$t_{SU:STO}$	-	-	-	μS	

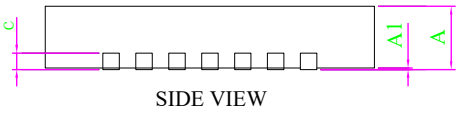
I²C Timing



13 Package Information

13.1 QFN28L(4.0mm × 4.0mm PP= 0.40mm)





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.20	2.30	2.40
e	0.40BSC		
Ne	2.40BSC		
Nd	2.40BSC		
E	3.90	4.00	4.10
E2	2.20	2.30	2.40
L	0.35	0.40	0.45
h	0.30	0.35	0.40

14 Disclaimer

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15 Revision History

No.	Version	Date	Modify the content	Check
1	1.0	2022-08-09	Initial release	YES
2	1.1	2025-10-23	Change Description	YES

[1] Please refer to the latest version of this document before starting or finalizing any design.

[2] Since the release of this document, the status or availability of this product may have changed. For the most up-to-date information, please visit: https://www.szvinka.com/