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VK1651 Datasheet

7×4 LED DRIVER

Rev.1.3

1 General Description

VK1651 is a dedicated LED driver control chip with a keyboard scanning circuit interface. It integrates a data latch, LED driver, keyboard scanning and other circuits internally. The SEG pin is connected to the cathode of the LED, and the GRID pin is connected to the anode of the LED, which can support a dot matrix LED display of 7SEG×4GRID. Supports up to 7×1 keys. This chip has excellent performance and is suitable for driving the display screens of induction cookers, microwave ovens and small household appliances. Adopt SOP16 and DIP16 packaging forms.

2 Key Features

- Operating voltage：3.0-5.5V
- Built-in RC oscillator
- 7SEG pins, 4 GRID pins
- The SEG pin can only be connected to the cathode of the LED, and the GRID pin can only be connected to the anode of the LED (common anode)
- 7×1 matrix keys (combination keys not supported)
- 2-wire serial interface
- The overall brightness is adjustable at 8 levels
- The built-in display RAM is 8×4 bits
- Built-in power-on reset circuit
- Available Packages:
  SOP16(150mil)(9.90m × 3.90mm PP=1.27mm)

3 Application Field

- Small household appliances
- Induction cooker/microwave oven
- Pressure gauge

4 Product Selection

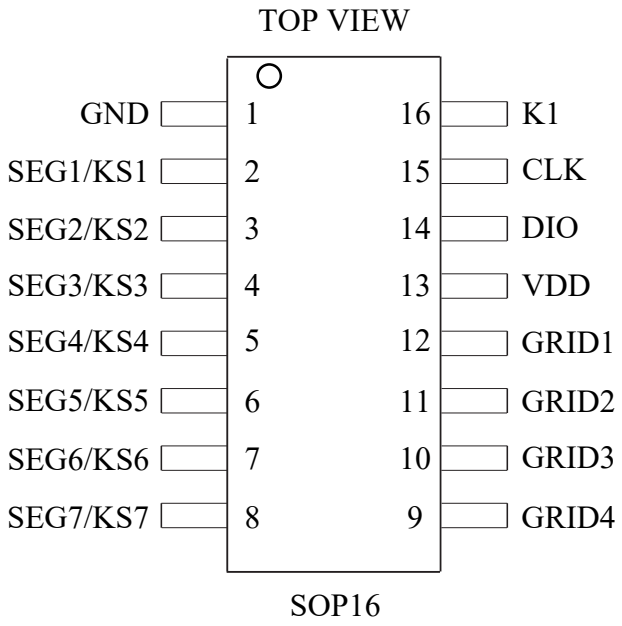
Part No.	Communication interface	Drive lattice	Common Cathode Drive	Common Anode Drive	Key press	Packaging
VK1640	CLK/DIN	128	8 / 16	16 / 8	---	SOP28
VK1640A	CLK/DIN	128	8 / 16	16 / 8	---	SSOP28
VK1640B	CLK/DIN	96	8 / 12	12 / 8	---	SSOP24
VK1Q60	CLK/DIN	32	8 / 4	4 / 8	7×4	QFN16L (3×3mm)
VK1650	CLK/DAT	32	8 / 4	4 / 8	7×4	SOP16
VK1651	CLK/DIO	28	4 / 7	7 / 4	7×1	SOP16

Note: Except for VK1651, for all other common cathode/common anode digital tubes, SEG is connected to the anode and GRID to the cathode.
The SEG of VK1651 is connected to the cathode and the GRID to the anode.

5 Ordering Information

Part No.	Packaging	Tube Qty	Tray(reel) Qty	Box Qty	Total Qty	Notes
VK1640	SOP28	26/tube		2080/box	20800 PCS	
VK1640A	SSOP28	50/tube		5000/box	50000 PCS	
VK1640B	SSOP24	50/tube		10000/box	100000 PCS	
VK1Q60	QFN16L (3×3mm)		3000/reel	30000/box	120000 PCS	
VK1650	SOP16		4000/reel	16000/box	96000 PCS	
VK1651	SOP16	50/tube		10000/box		

6 Package Pinout Information(SOP16)



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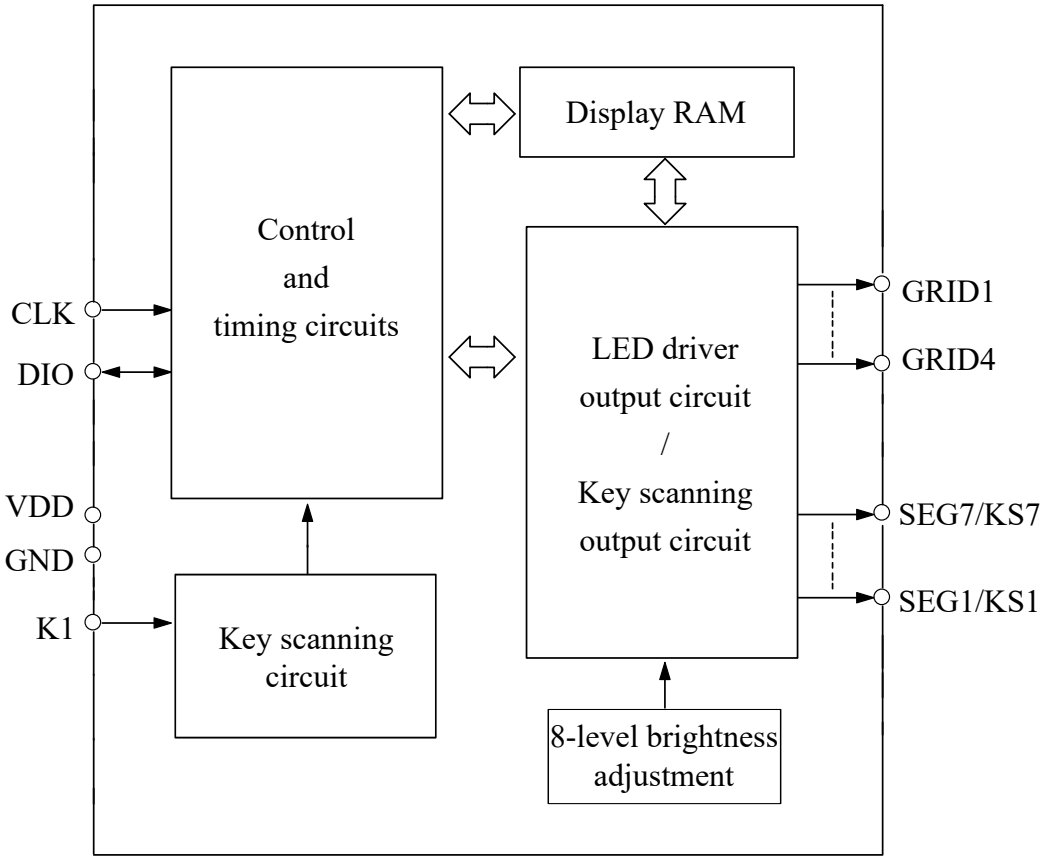
6.1 VK1651/SOP16 Pin Description

No.	Name	I/O	Function
1	GND	GND	Negative power supply
2-8	SEG1/KS1-SEG7/KS7	O	LED SEG driver output, high level effective, also used as key scan input, high level effective, built-in pull-down
9-12	GRID1-GRID4	O	LED GRID output (N-tube leakage open); Key scan output
13	VDD	VDD	Positive power supply
14	DIO	I/O	Serial data input/output
15	CLK	I	Input/output data at the rising edge
16	K1	O	The data input to this pin is latched after the display period ends, and K1 has a 10K pull-up resistor inside

7 Functional Description

7.1 Block Diagram



7.2 Display RAM- Storage Structure

The static display memory (RAM) has an 8× 4-bit structure and stores the displayed data. The content of RAM is directly mapped to the display content of the LED driver, with display addresses ranging from 0xC0 to 0xC3, and there are a total of 4 display units. If you want to turn on or off a certain LED, simply set the corresponding display RAM position 1 or clear 0. For example, to control the on/off of LED1 driven by pins SEG1 and GRID1, simply set the bit0 position of the corresponding display RAM (address 0xC0) to 1 or clear 0. When powered on, the default address is 0xC0.

The process of mapping the contents in RAM to leds is shown in the following table:

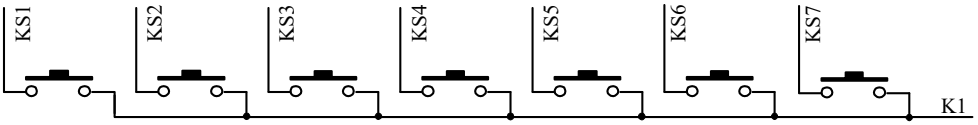
SEG / GRID	X	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	Addr
GRID1								LED1	0xC0
GRID2									0xC1
GRID3									0xC2
GRID4									0xC3
	D7	D6	D5	D4	D3	D2	D1	D0	

Note:

1. The value stored inside the chip display RAM at the moment of power-on may be random. It is recommended that the customer perform a power-on reset of the display RAM, that is, write all the data 0x00 to the 4-byte display RAM(address 0xC0-0xC3) after power-on
2. The SEG pin can only be connected to the anode of the LED, and the GRID pin can only be connected to the cathode of the LED. They must not be reversed.

7.3 Keyboard Scanning

The key scan matrix is 7×1 bits, as shown below:



After the key is pressed, the read key values of VK1651 are shown in the following table:

column / line	KS1	KS2	KS3	KS4	KS5	KS6	KS7
K1	0xEF	0x6F	0xAF	0x2F	0xCF	0x4F	0x8F
	Key value						

Note: Combination keys are not supported. When no key is pressed, the read key data is 0xFF(11111111).

8 Serial Communication Commands

8.1 Communication Interface

The VK1651 has two communication pins. Two-wire serial communication is adopted.

The CLK pin is the clock input pin. Data is written to the display RAM at the rising edge, and DIO pin data is read out at the rising edge.

The DIO pin is a serial data input pin. Input data changes at the low level of the CLK and is transmitted at the high level of the CLK.

The starting condition for data input is that when CLK is at a high level, DAT decreases from high to low. The termination condition is that when CLK is high, DAT changes from a low level to a high level.

ACK signal: If the communication is normal, at the 8th clock falling edge of the serial communication, the VK1651 pulls down the DAT. DAT is released as input until the 9th rising edge of the clock is detected.

8.2 Command Format

Commands are used to set the display mode, write display data and read key values.

The first byte input by DIO after the falling edge of CLK is taken as the command. After decoding, the highest two bits, 7 and 6, are selected to distinguish different commands, as shown in the following table:

Bit7	Bit6	Command function
0	1	Data read and write setting command
1	0	Display control command
1	1	Address setting command

9 Command Description

9.1 Data Read And Write Setting Commands

This instruction is used to set data writing and reading. Bits B1 and B0 are not allowed to be set to 01 or 11.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	Note
0	1	For irrelevant items, fill in 0				0	0	Data read and write mode Settings	Write the data to the display register
0	1					1	0		Read keys scan data
0	1				0			Address increase mode Settings	Automatic address increase
0	1				1				Fixed address
0	1			0				Test mode Settings (for internal use)	Normal mode
0	1			1					Test mode

9.2 Address Setting Command

Set the address of the displayed RAM (0xC0-0xC3). When powered on, the address is set to 0xC0 by default.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Display RAM address
1	1	For irrelevant items, fill in 0		0	0	0	0	0xC0
1	1			0	0	0	1	0xC1
1	1			0	0	1	0	0xC2
1	1			0	0	1	1	0xC3

9.3 Display Control Commands

Set the display switch and select the display brightness (8 levels).

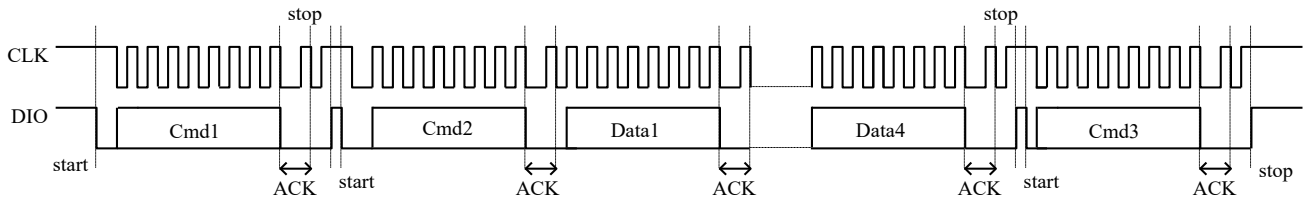
MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	Note
1	0	For irrelevant items, fill in 0			0	0	0	Grayscale setting	Set the pulse width to 1/16
1	0				0	0	1		Set the pulse width to 2/16
1	0				0	1	0		Set the pulse width to 4/16
1	0				0	1	1		Set the pulse width to 10/16
1	0				1	0	0		Set the pulse width to 11/16
1	0				1	0	1		Set the pulse width to 12/16
1	0				1	1	0		Set the pulse width to 13/16
1	0				1	1	1		Set the pulse width to 14/16
1	0			0				Display switch Settings	Display off
1	0			1					Display on

10 Command Timing

10.1 Send Display Data (address automatically adds 1)

To transfer display data using the address auto-increment mode, first set the starting address of the data to be transferred (corresponding to the display RAM address). After the starting address command word is sent, the display data is directly transmitted, with a maximum of 4 bytes. After the data is transmitted, the corresponding display control command is sent.



Cmd1: Data Read and Write Settings Command - Set Address Auto-increment Mode (0x40)

Cmd2: Address Setting Command - Set the display RAM address (0xC0-0xC3)

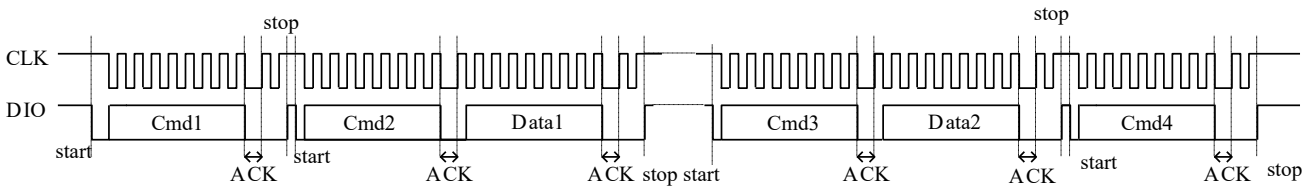
Data1: Send display data to the display RAM address set by Cmd2

Data1-Datan: Send the display data to the starting address set by Cmd2 and the subsequent display RAM (up to 4 bytes)

Cmd3: Display Control Command - Display on and set the display brightness level

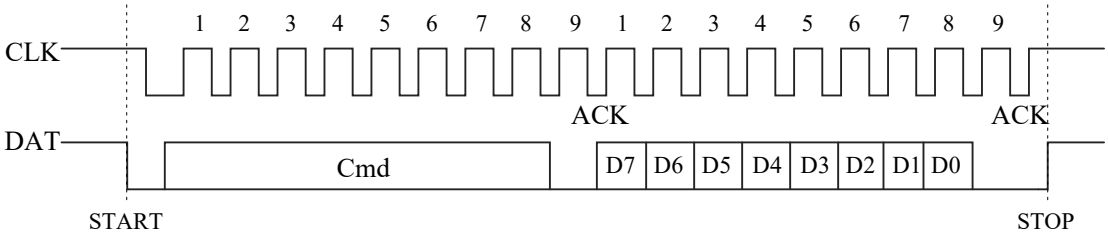
10.2 Send Display Data (fixed address)

To transmit display data using the fixed address mode, first set the address for the data to be transmitted (corresponding to the display RAM address). After the address is sent, directly transmit 1 byte of display data through an ACK signal. Once the data transmission is completed, send a stop signal. Then start transmitting the address of the next display data. Directly transmit 1 byte of display data through an ACK signal. After the data transmission is completed, send a stop signal. ... Display the data until the last byte is transmitted, with a maximum of 4 bytes.



Cmd1: Data Read and Write Settings Command - Set Fixed Address Mode (0x44)
Cmd2: Address Setting Command - Set the display RAM address (0xC0-0xC3)
Data1: Send display data to the display RAM address set by Cmd2
Cmd3: Address Setting Command - Set Display RAM Address (0xC0-0xC3)
Data2: Send display data to the display RAM address.... set by Cmd3 A maximum of 4 bytes of data can be transmitted
Cmd4: Display Control Commands - Display on and set the display brightness level

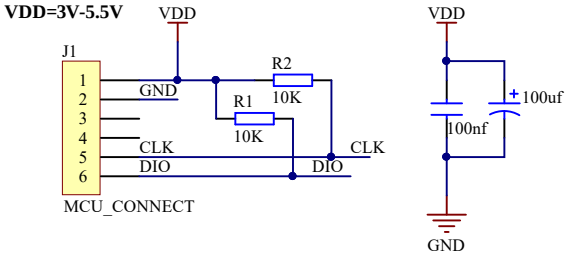
10.3 Read The Key Timing Sequence

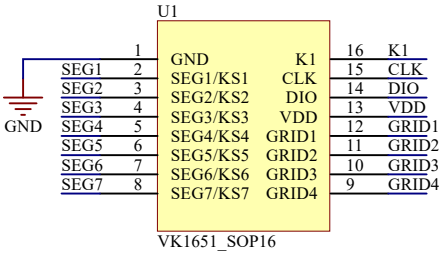


Cmd: Send read key scan command (0x42)
Data: Read key value, 1 byte represents one key code, only supports single keys, does not support multiple keys.

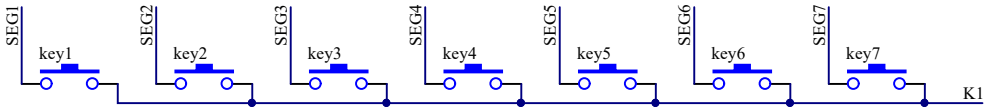
11 Application Circuits

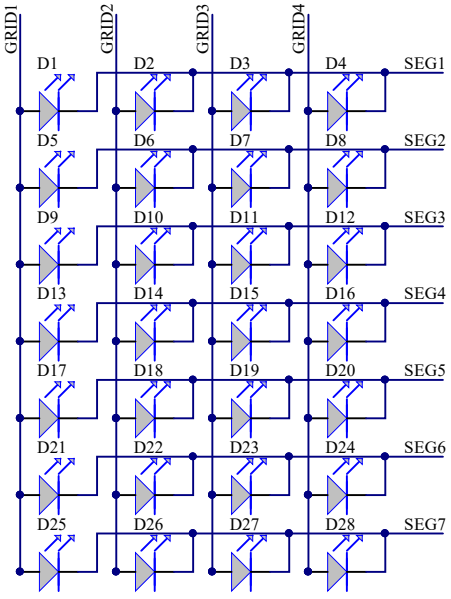
When the surrounding interference is relatively large, a 10R to 10k resistor and a PF-level small capacitor to ground can be connected in series on the communication pin. When the power supply of the single-chip microcomputer (3.3V) and the driver chip (5V) is inconsistent, it is recommended to add a level conversion circuit on the communication pin





The filter capacitor between VDD and GND should be placed as close to the chip as possible on the PCB board to enhance the filtering effect.





The SEG pin can only be connected to the cathode of the LED, and the GRID pin can only be connected to the anode of the LED

12 Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.5～7.0	V
Input Voltage	VIN	V_{SS}-0.5～V_{DD}+0.5	V
SEG output current	I_{O1}	-500	mA
GRID output current	I_{O1}	200	mA
Power loss	P_D	400	mW
Storage Temperature	T_{STG}	-65~+150	℃
Operating Temperature	T_{OTG}	-40~+85	℃

12.2 DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	3.0	5.0	5.5	V	—	—
Static current	I_{DD}	—	—	5.0	mA	5V	No load /LED off
Low-level input current	I_{OL1}	-20	-25	-40	mA	5V	VO=VDD-2V SEG1~SEG7
	I_{OL2}	-20	-30	-50			VO=VDD-3V SEG1~SEG7
High-level output current	I_{OH}	80	140	—	mA	5V	VO=VDD-0.3V GRID1- GRID4
High-level output current tolerance	I_{TOLSEG}	—	—	5	%	VDD	VO=VDD-3V SEG1- SEG7
Low-level Input	V_{IL}	0	—	0.3	VDD	VDD	CLK, DIO
High-level Input	V_{IH}	0.7	—	1.0		VDD	
Hysteresis voltage	V_H	—	0.35	—		VDD	
Pull-up resistor	R_L	—	10	—	kΩ	5V	K1

12.3 AC Electrical Characteristics

Internal timing parameters (test conditions: Ta = 25℃, VDD =5V)

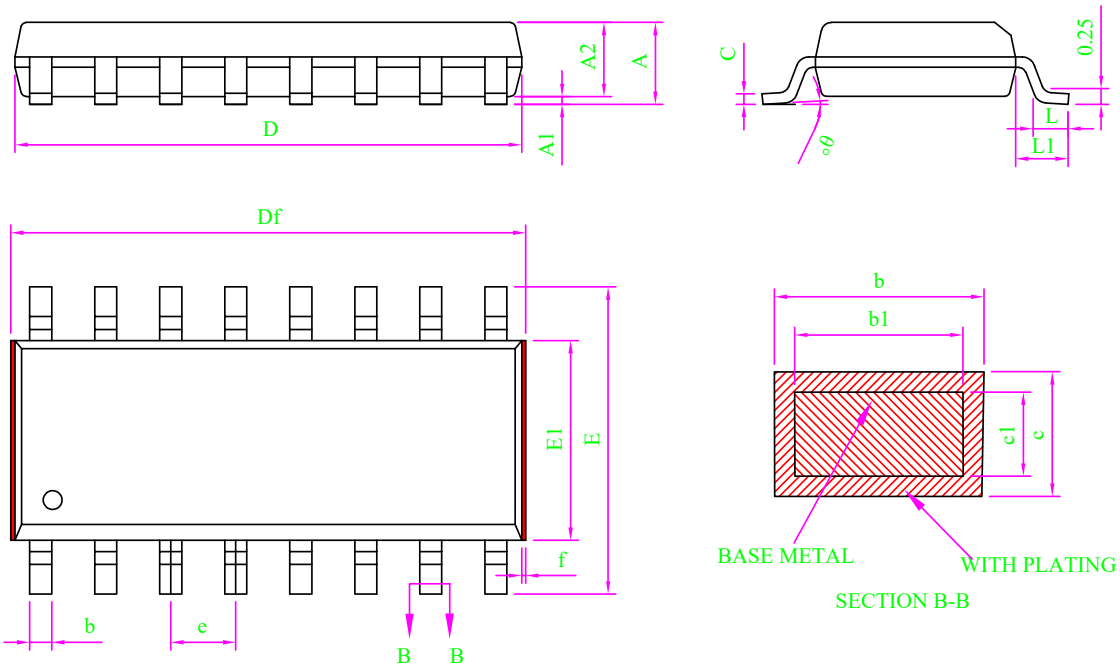
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Oscillation frequency	F_{OSC}	—	500	—	KHz	
Transmission delay time	t_{PLZ}	—	—	300	nS	CLK→DOUT CL=15pF,RL=10KΩ
	P_{ZL}	—	—	100	nS	
Rising time	t_{ZH1}	—	—	2	μS	CL=300pF SEG1-SEG7
	t_{TZH2}	—	—	0.5	μS	CL=300pF GRID1-GRID4
Decrease time	t_{THZ}	—	—	120	μS	CL = 300pF SEGn,GRIDn
Maximum input clock frequency	F_{MAX}	—	—	1	MHz	Duty cycle: 50%
Input capacitance	C_I	—	—	15	pF	—

Serial communication parameters (test conditions: Ta = 25℃, VDD =5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Clock pulse width	P_{WCLK}	400	—	—	nS	—
Data establishment time	t_{SETUP}	100	—	—	nS	—
Data retention time	t_{HOLD}	100	—	—	nS	—
Waiting time	T_{wait}	1	—	—	μS	CLK↑→CLK↓

13 Package Information

13.1 SOP16(9.9mm × 3.9mm PP=1.27mm)



Note:

1. All dimension are in mm.
   Dim D&El does not include plastic flash; Df includes plastic flash(f);
   Flash: Plastic residual around body edge after de junk/singulation.
2. Dim b does not include dambar protrusion/intrusion.
3. Plating thickness 0.007mm-0.020mm

MILLIMETER			
SYMBOL	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	0.15	0.20
A2	1.35	1.45	1.55
b	0.39	-	0.47
b1	0.38	0.41	0.43
c	0.20	-	0.25
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
Df	9.90	-	10.40
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
L	0.51	0.66	0.81
L1	0.95	1.05	1.15
θ	0	-	8°
f	0.05	-	0.20

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15 Revision History

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Initial release	YES
2	1.1	2018-10-11	Add reference circuit	YES
3	1.2	2019-03-21	Alignment correction	YES
4	1.3	2025-10-17	Change Description	YES

[1] Please refer to the latest version of this document before starting or finalizing any design.

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