Vinka Microelectronics

VK1640A Datasheet

8×16 LED DRIVER
Rev.1.3

1 General Description

VK1640A is a dedicated chip for digital tube or dot matrix LED driver control, integrating circuits such as data latches and LED drivers internally. The SEG pin is connected to the anode of the LED, and the GRID pin is connected to the cathode of the LED, which can support 8SEG×16GRID dot matrix LED display. It is suitable for driving small LED display screens. It adopts the SSOP28 packaging form.

2 Key Features

- Operating voltage：3.0-5.5V
- Built-in RC oscillator
- 8 SEG pins, 16 GRID pins
- The SEG pin can only be connected to the anode of the LED, and the GRID pin can only be connected to the cathode of the LED
- 2-wire serial interface
- The overall brightness is adjustable at 8 levels
- The built-in display RAM is 8×16 bits
- Built-in power-on reset circuit
- Available Packages:
  SSOP28(150mil)(9.9mm×3.9mm PP=0.635mm)

3 Application Field

- Small household appliances
- Induction cooker/microwave oven
- Pressure gauge

4 Product Selection

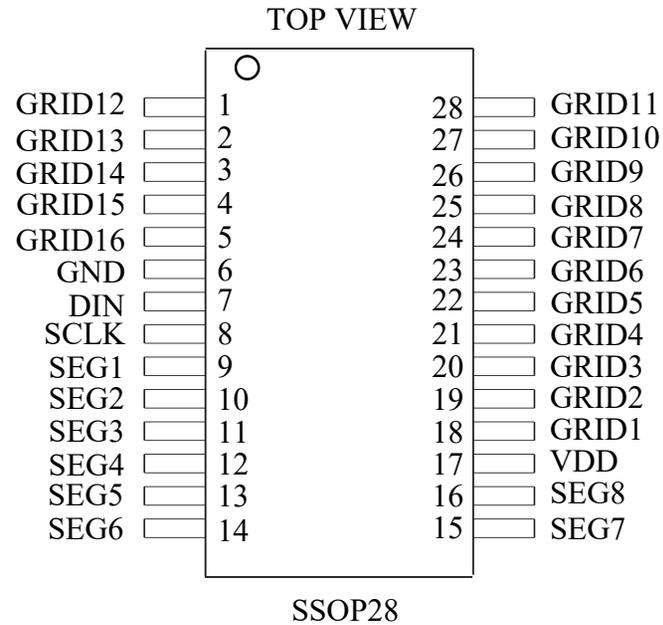| Part No.	Communication interface	Drive lattice	Common Cathode Drive	Common Anode Drive	Key press	Packaging
VK1640	CLK/DIN	128	8 / 16	16 / 8	---	SOP28
VK1640A	CLK/DIN	128	8 / 16	16 / 8	---	SSOP28
VK1640B	CLK/DIN	96	8 / 12	12 / 8	---	SSOP24
VK1Q60	CLK/DIN	32	8 / 4	4 / 8	7×4	QFN16L (3×3mm)
VK1650	CLK/DAT	32	8 / 4	4 / 8	7×4	SOP16
VK1651	CLK/DIO	28	4 / 7	7 / 4	7×1	SOP16

Note: Except for VK1651, for all other common cathode/common anode digital tubes, SEG is connected to the anode and GRID to the cathode.

The SEG of VK1651 is connected to the cathode and the GRID to the anode.

5 Ordering Information

Part No.	Packaging	Tube Qty	Tray(reel) Qty	Box Qty	Total Qty	Notes
VK1640	SOP28	26/tube		2080/box	20800 PCS	
VK1640A	SSOP28	50/tube		5000/box	50000 PCS	
VK1640B	SSOP24	50/tube		10000/box	100000 PCS	
VK1Q60	QFN16L (3×3mm)		3000/reel	30000/box	120000 PCS	
VK1650	SOP16		4000/reel	16000/box	96000 PCS	
VK1651	SOP16	50/tube		10000/box		

6 Package Pinout Information(SSOP28)

TOP VIEW

Pin		Pin	
GRID12	1	28	GRID11
GRID13	2	27	GRID10
GRID14	3	26	GRID9
GRID15	4	25	GRID8
GRID16	5	24	GRID7
GND	6	23	GRID6
DIN	7	22	GRID5
SCLK	8	21	GRID4
SEG1	9	20	GRID3
SEG2	10	19	GRID2
SEG3	11	18	GRID1
SEG4	12	17	VDD
SEG5	13	16	SEG8
SEG6	14	15	SEG7

SSOP28

For more information:

6.1 VK1640A/SSOP28 Pin Description

No.	Name	I/O	Function
18-28 1-5	GRID1-GRID16	O	LED GRID output (N-tube leakage open)
6	GND	GND	Negative power supply
7	DIN	I	Serial data input, data changes at the low level of SCLK and is transmitted at the high level of SCLK.
8	SCLK	I	The clock signal reads the input data to the display RAM at the rising edge.
9-16	SEG1-SEG8	O	LED SEG output (P tube leakage open)
17	VDD	VDD	Positive power supply

7 Functional Description

7.1 Block Diagram
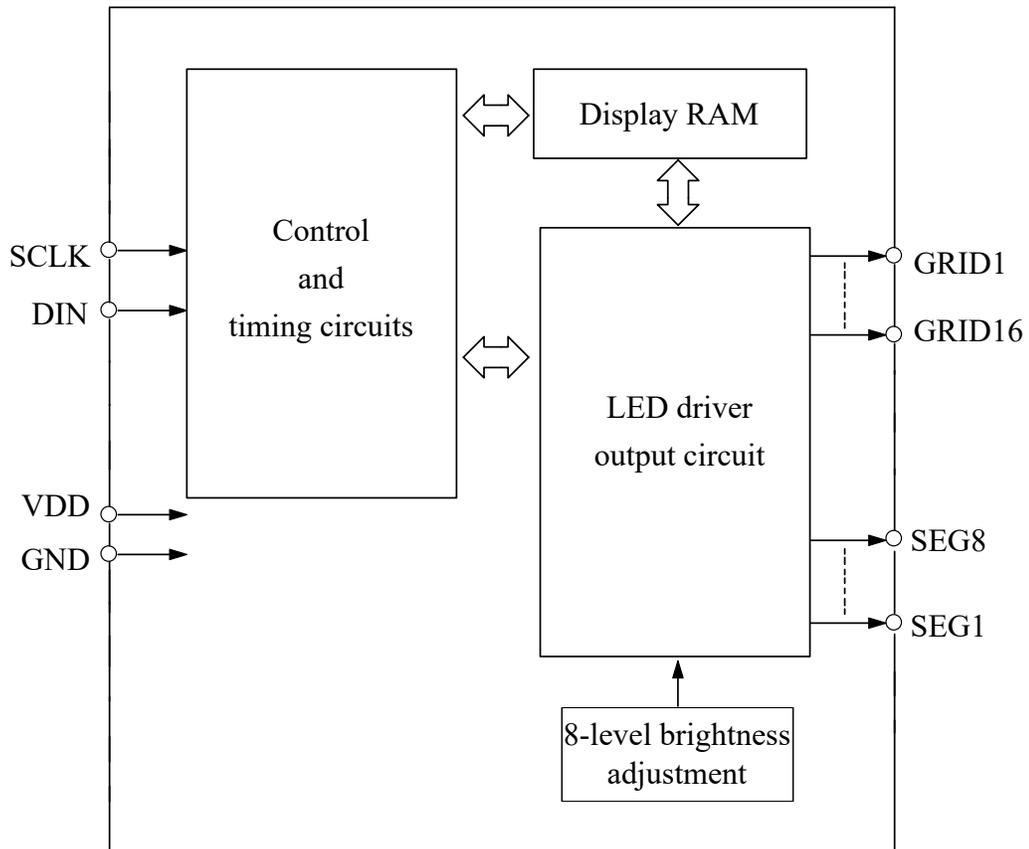
7.2 Display RAM- Storage Structure

The static display memory (RAM) has a structure of 8×16 bits and stores the displayed data. The content of RAM is directly mapped to the display content of the LED driver, with display addresses ranging from 0xC0 to 0xCF, and there are a total of 16 display units. If you want to turn on or off a certain LED, simply set the corresponding display RAM position 1 or clear 0. For example, to control the on/off of LED1 driven by pins SEG1 and GRID1, simply set the Bit0 position of the corresponding display RAM (address 0xC0) to 1 or clear 0. Clear the RAM bits corresponding to the unused SEG pins in the application to 0.

The process of mapping the contents in RAM to LED is shown in the following table:

SEG / GRID	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	Addr
GRID1								LED1	0xC0
GRID2									0xC1
GRID3									0xC2
GRID4									0xC3
GRID5									0xC4
GRID6									0xC5
GRID7									0xC3
GRID8									0xC4
GRID9									0xC5
GRID10									0xC2
GRID11									0xC3
GRID12									0xC4
GRID13									0xC5
GRID14									0xCD
GRID15									0xCE
GRID16									0xCF
	D7	D6	D5	D4	D3	D2	D1	D0	

Note:

1. The value stored inside the chip display RAM at the moment of power-on may be random. It is recommended that the customer perform a power-on reset of the display RAM, that is, write all the data 0x00 to the 16-byte display RAM(address 0xC0-0xCF) after power-on.

2. The SEG pin can only be connected to the anode of the LED, and the GRID pin can only be connected to the cathode of the LED. They must not be reversed.

8　Serial Communication Commands

8.1　Communication Interface

The VK1640A has two communication pins.

The SCLK pin is the clock input pin, which reads data from the rising edge to the display RAM.

The DIN pin is a serial data input pin. The input data changes at the low level of SCLK and is transmitted at the high level of SCLK.

The initial condition for data input is that when SCLK is at a high level, DIN decreases from high to low. The termination condition is that when SCLK is high, DIN changes from a low level to a high level.

8.2　Command Format

Commands are used to set the display mode and write display data.

After the "START" command becomes valid, the first byte input by DIN is taken as the command. After decoding, the highest two bits, Bit7 and Bit6, are selected to distinguish different commands, as shown in the following table:

bit7	bit6	Function
0	1	Data write setting command
1	0	Display control command
1	1	Address setting command

9   Command Description

9.1   Data Write Settings Command

This command is used for LED display data writing and key reading as well as related commands. Bit1 and Bit0 bits are not allowed to be set to 01 or 11.

When powered on, the Bit3-Bit0 data is 0.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Function	Note
0	1					0	0	Data writing	Write the data to the display register
0	1	---			0			Address increase mode Settings	Address increases automatically
0	1				1				Fixed address
0	1			0				Working mode Settings	Normal mode
0	1			1					Test mode

9.2   Address Setting Command

Set the address of the displayed RAM (0xC0-0xCF). When powered on, the address is set to 0xC0 by default.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Display RAM address
1	1			0	0	0	0	0xC0
1	1			0	0	0	1	0xC1
1	1			0	0	1	0	0xC2
1	1			0	0	1	1	0xC3
1	1			0	1	0	0	0xC4
1	1			0	1	0	1	0xC5
1	1	---		0	1	1	0	0xC6
1	1			0	1	1	1	0xC7
1	1			1	0	0	0	0xC8
1	1			1	0	0	1	0xC9
1	1			1	0	1	0	0xCA
1	1			1	0	1	1	0xCB
1	1			1	1	0	0	0xCC
1	1			1	1	0	1	0xCD
1	1			1	1	1	0	0xCE
1	1			1	1	1	1	0xCF

9.3 Display Control Command

Set the display switch and select the display brightness (8 levels).

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Function	Note
1	0				0	0	0		Set the pulse width to 1/16
1	0				0	0	1		Set the pulse width to 2/16
1	0				0	1	0		Set the pulse width to 4/16
1	0				0	1	1	Set the	Set the pulse width to 10/16
1	0	---			1	0	0	pulse width	Set the pulse width to 11/16
1	0				1	0	1		Set the pulse width to 12/16
1	0				1	1	0		Set the pulse width to 13/16
1	0				1	1	1		Set the pulse width to 14/16
1	0			0				Display switch	Display off
1	0			1					Display on

## 9.4 Command Timing

Write commands or display data
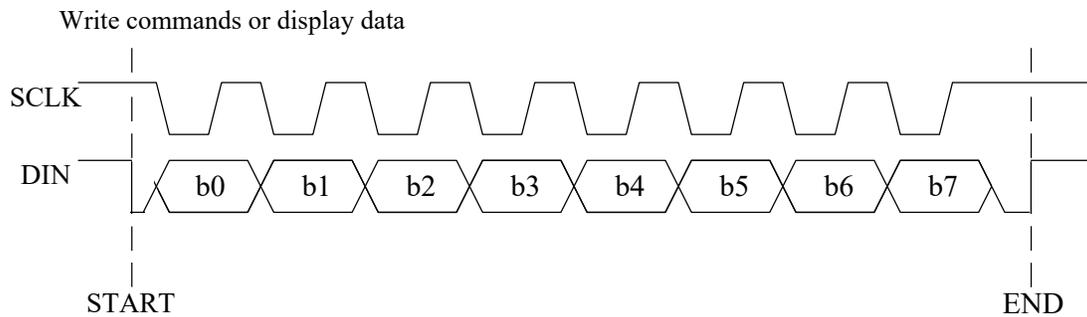
10 Command Application

10.1 Send Display Data (address automatically adds 1)

To transfer display data using the address auto-increment mode, first set the starting address of the data to be transferred (corresponding to the display RAM address). After the start address command word is sent, the display data is directly transmitted, with a maximum of 16 bytes.
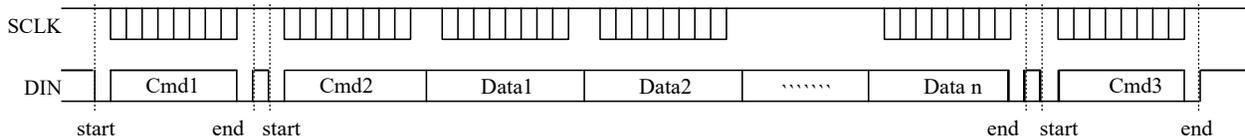
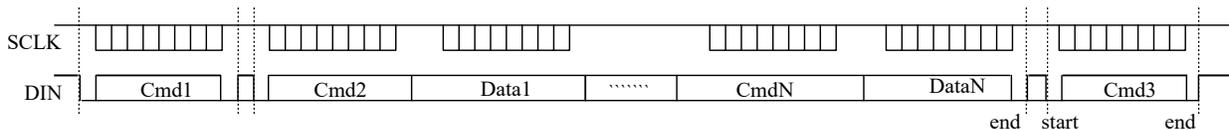Cmd1: Data Write Setting Command - Set Address to increase automatically (0×40)

Cmd2: Address Setting Command - Set the display RAM starting address
(0×C0-0×CF)

Data1-Datan: Send the display data to the starting address set by Cmd2 and the subsequent display RAM (up to 16 bytes)

Cmd3: Display Control Command - Display on and set the display brightness level

10.2 Send Display Data (fixed address)

To transfer display data using the fixed address mode, first set the address for the data to be transferred (corresponding to the display RAM address). After the address is sent, directly transfer 1 byte of display data. Then send the address of the next display data, directly sending 1 byte of display data. ... Display the data until the last byte is transmitted, with a maximum of 16 bytes.

Cmd1: Data Write Setting Command - Set Fixed Address Mode (0x44)

Cmd2: Address Setting Command - Set Display RAM Address (0xC0-0xCF)

Data1: Send display data to the display RAM address set by Cmd2

CmdN: Address Setting Command - Set display RAM Address (0xC0-0xCF)

DataN: Send display data to the display RAM address.... set by CmdN A maximum of
16 bytes of data can be transmitted

Cmd3: Display Control Command - Display on and set the display brightness level

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11 Application Circuits

When the surrounding interference is relatively large, a 10R to 10k resistor and a PF-level small capacitor to ground can be connected in series on the communication pin. When the power supply of the single-chip microcomputer (3.3V) and the driver chip (5V) is inconsistent, it is recommended to add a level conversion circuit on the communication pin
VDD=3V-5.5V
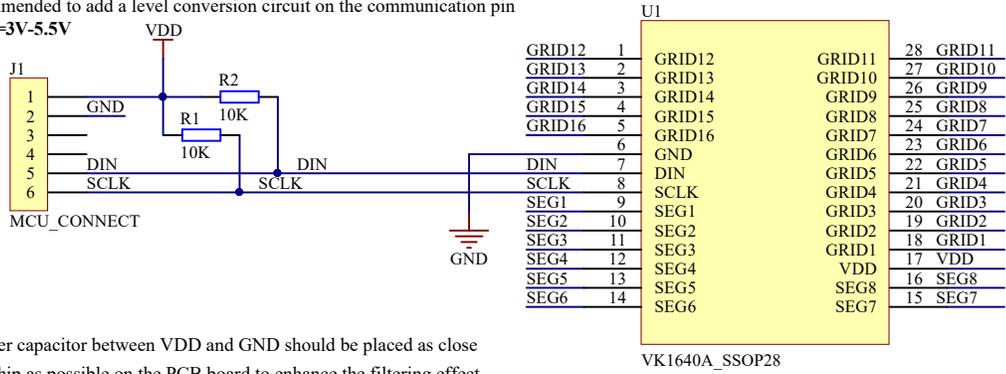
The filter capacitor between VDD and GND should be placed as close to the chip as possible on the PCB board to enhance the filtering effect.
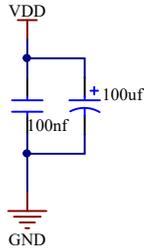
Connect the SEG pin to the anode of the LED
and the GRID pin to the cathode of the LED
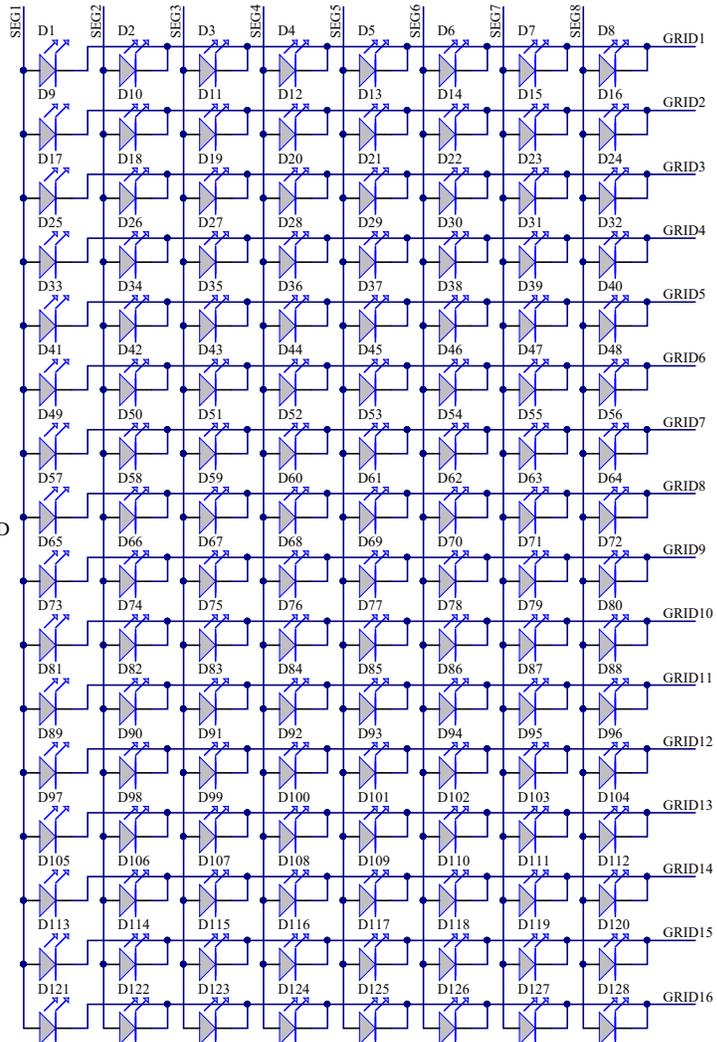
12　Electrical Characteristics

12.1　Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.5～+6.0	V
Input Voltage	V_{IN}	V_{SS}-0.5～V_{DD}+0.5	V
Power loss	P_D	400	mW
Drive output current	I_{OLGRID}	+200	mA
	I_{OHSEG}	-50	mA
Storage Temperature	T_{STG}	-65～+150	°C
Operating Temperature	T_{OTG}	-40～+85	°C

12.2　DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	3.0	—	5.5	V	—	—
Static current	I_{DD}	—	—	0.1	mA	5V	No load /LED off
High-level output current	I_{OH1}	-20	-25	-40	mA	5V	VO=VDD-2V SEG1- SEG8
	I_{OH2}	-20	-30	-50			VO=VDD-3V SEG1- SEG8
Low-level input current	I_{OLGRID}	80	140	—	mA	5V	VO=0.3V GRID1- GRID16
Low-level Input	V_{IL}	0	—	0.3	VDD	VDD	SCLK,DIN
High-level Input	V_{IH}	0.7	—	1.0		VDD	
Hysteresis voltage	V_H	—	0.35	—	V	5V	SCLK,DIN

12.3 AC Electrical Characteristics

Switch parameter

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Oscillation frequency	F_{osc}	—	500	—	KHz	
Transmission delay time	t_{PLZ}	—	—	300	nS	CLK→DOUT CL=15pF,RL=10KΩ
	P_{ZL}	—	—	100	nS	
Rising time	t_{ZH1}	—	—	2	μS	CL=300pF SEG1-SEG8 GRID1-GRID16
	t_{TZH2}	—	—	0.5	μS	CL=300pF GRID1-GRID16
Decrease time	t_{THZ}	—	—	120	μS	CL = 300pF SEGn,GRIDn
Maximum input clock frequency	F_{MAX}	—	—	1	MHz	Duty cycle: 50%
Input capacitance	C_I	—	—	15	pF	—

Timing parameter

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Clock pulse width	P_{WCLK}	400	—	—	nS	—
Data establishment time	t_{SETUP}	100	—	—	nS	—
Data retention time	t_{HOLD}	100	—	—	nS	—
Waiting time	T_{wait}	1	—	—	μS	CLK↑→CLK↓
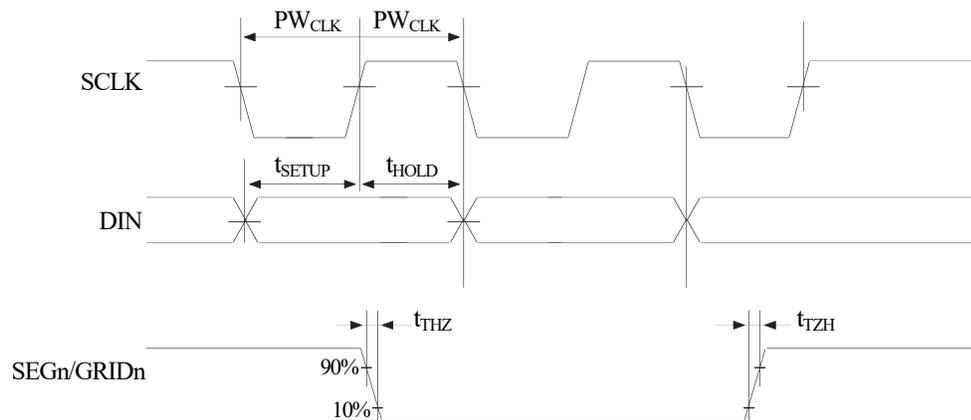
13   Package Information

13.1   SSOP28(150mil) (9.9mm × 3.9mm PP=0.635mm)
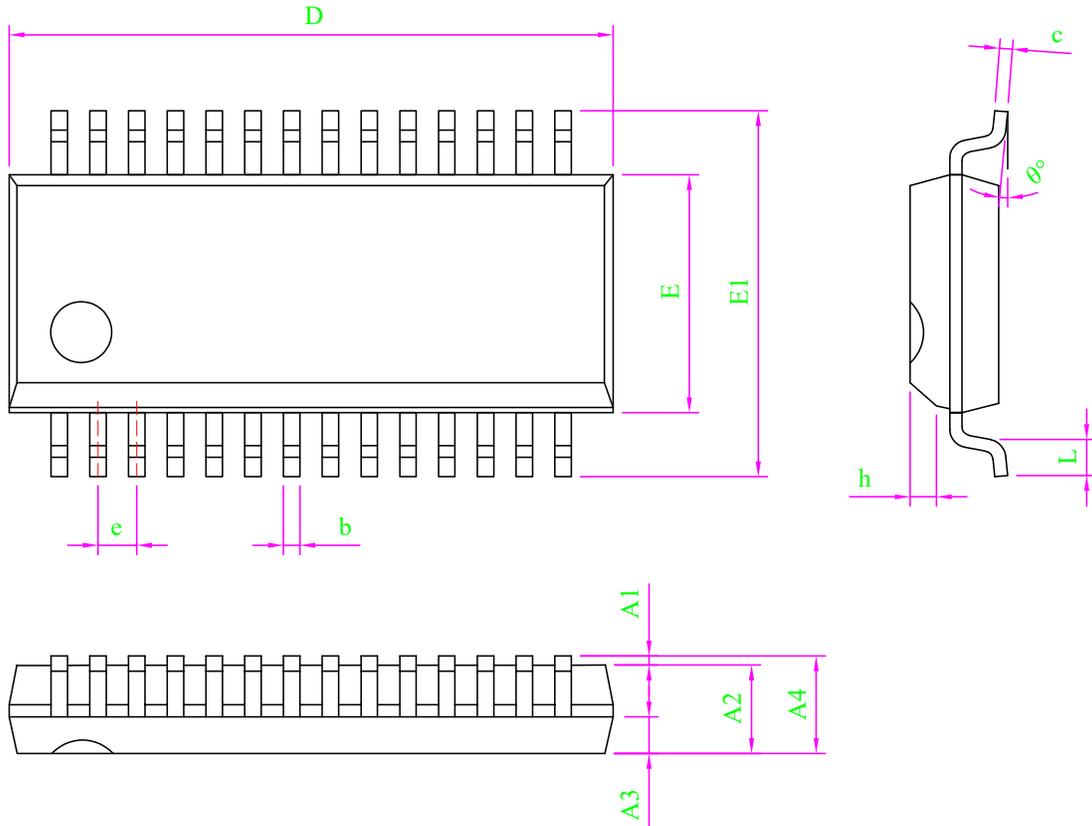
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.05	-	0.23
A2	1.35	1.45	1.55
A3	0.60	0.65	0.70
b	0.23	-	0.31
c	0.19	-	0.25
D	9.80	9.90	10.00
E	3.90	3.90	4.00
E1	5.80	6.00	6.20
e	0.635 BSC		
h	0.30	-	0.50
L	0.60	-	0.80
θ	0	-	8°

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15 Revision History

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Initial release	YES
2	1.1	2018-10-11	Add reference circuit	YES
3	1.2	2019-03-21	Alignment correction	YES
4	1.3	2025-10-14	Change Description	YES

[1] Please refer to the latest version of this document before starting or finalizing any design.

[2] Since the release of this document, the status or availability of this product may have changed. For the most up-to-date information, please visit: https://www.szvinka.com/