# Vinka Microelectronics

# VK1629C Datasheet

## 15×8 LED DRIVER
## Rev.1.3

# 1 General Description

VK1629C is a dedicated chip for digital tube or dot matrix LED driver control with a keyboard scanning interface. It integrates a 3-wire serial interface, data latch, LED driver, keyboard scanning and other circuits internally. The SEG pin is connected to the anode of the LED, and the GRID pin is connected to the cathode of the LED. It can support a dot matrix LED display panel of 15G SEX 8Grid, with a maximum support of 8x1 key matrix. High-end display screen drivers suitable for products such as refrigerators, air conditioners, and home theaters. It adopts the SOP32 packaging form.

# 2 Key Features

- Operating voltage：3.0-5.5V
- Built-in RC oscillator
- 15 SEG pins, 8 GRID pins
- The SEG pin can only be connected to the anode of the LED, and the GRID pin can only be connected to the cathode of the LED
- Maximum support for 8×1 matrix keys
  (key/display multiplexing requires hardware circuit coordination)
- 3-wire serial interface
- The overall brightness is adjustable at 8 levels
- The built-in display RAM is 16×8 bits
- Built-in power-on reset circuit
- Available Packages:
  SOP32（21.00mm×7.50mm PP=1.27mm)

# 3 Application Field

- Small household appliances
- Induction cooker/microwave oven
- Pressure gauge
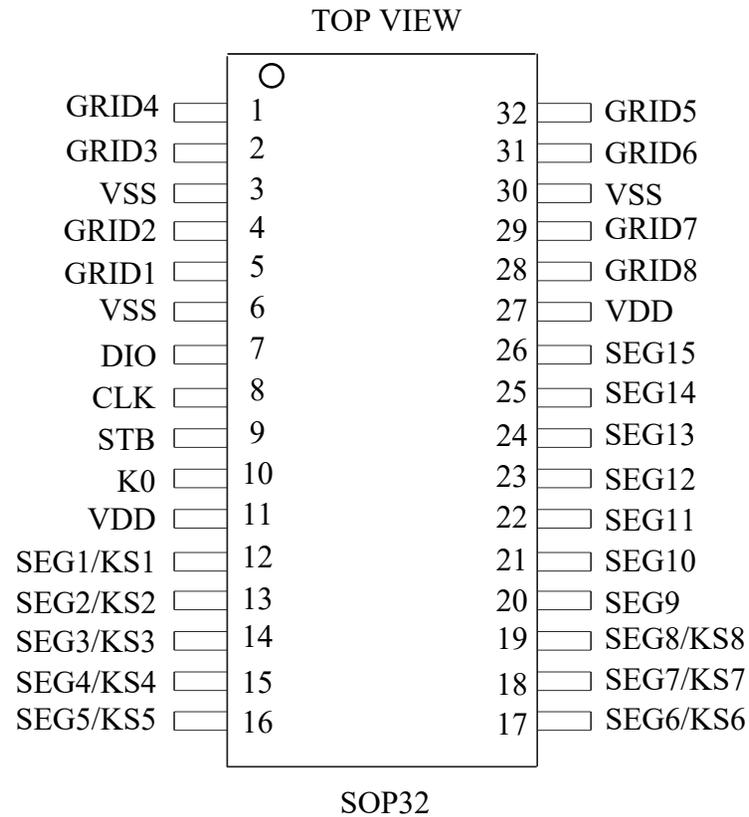
## 4　Product Selection

| Part No. | Common Cathode Drive | Common Anode Drive | Key press | Packaging |
|---|---|---|---|---|
| VK1S38A | 8 / 8 | 8 / 8 | 8×3 | SSOP24 |
| VK1638 | 10 / 8 | 8 / 10 | 8×3 | SOP28 |
| VK1629A | 16 / 8 | 8 / 16 | --- | SOP32 |
| VK1629B | 14 / 8 | 8 / 14 | 8×2 | SOP32 |
| VK1629C | 15 / 8 | 8 / 15 | 8×1 | SOP32 |
| VK1629D | 12 / 8 | 8 / 12 | 8×4 | SOP32 |
| VK1629 | 16 / 8 | 8 / 16 | 8×4 | LQFP44 |
| VK6932 | 8 / 16 | 16 / 8 | --- | SOP32 |

Note: For both common cathode and common anode digital tubes, SEG is connected to the anode and GRID to the cathode.

## 5　Ordering Information

| Part No. | Packaging | Tube Qty | Tray(reel) Qty | Box Qty | Total Qty | Notes |
|---|---|---|---|---|---|---|
| VK1S38A | SSOP24 | 60/tube | | 6000/box | 20800 PCS | |
| VK1638 | SOP28 | 26/tube | | 2080/box | 16000 PCS | |
| VK1629A | SOP32 | 20/tube | | 1600/box | 16000 PCS | |
| VK1629B | SOP32 | 20/tube | | 1600/box | 16000 PCS | |
| VK1629C | SOP32 | 20/tube | | 1600/box | 16000 PCS | |
| VK1629D | SOP32 | 20/tube | | 1600/box | 16000 PCS | |
| VK1629 | LQFP44 | | 160/tray | 1600/box | 16000 PCS | |
| VK6932 | SOP32 | 20/tube | | 1600/box | 16000 PCS | |

## 6 Package Pinout Information(SOP32)

TOP VIEW

| | | | |
|---|---|---|---|
| GRID4 | 1 | 32 | GRID5 |
| GRID3 | 2 | 31 | GRID6 |
| VSS | 3 | 30 | VSS |
| GRID2 | 4 | 29 | GRID7 |
| GRID1 | 5 | 28 | GRID8 |
| VSS | 6 | 27 | VDD |
| DIO | 7 | 26 | SEG15 |
| CLK | 8 | 25 | SEG14 |
| STB | 9 | 24 | SEG13 |
| K0 | 10 | 23 | SEG12 |
| VDD | 11 | 22 | SEG11 |
| SEG1/KS1 | 12 | 21 | SEG10 |
| SEG2/KS2 | 13 | 20 | SEG9 |
| SEG3/KS3 | 14 | 19 | SEG8/KS8 |
| SEG4/KS4 | 15 | 18 | SEG7/KS7 |
| SEG5/KS5 | 16 | 17 | SEG6/KS6 |

SOP32

## 6.1 VK1629C/SOP32 Pin Description

| No. | Name | I/O | Function |
|---|---|---|---|
| 1-2,4-5 32-31 29-28 | GRID1-GRID8 | O | LED GRID output (N-channel open-drain output) |
| 3, 6 30 | VSS | VSS | Negative power supply |
| 7 | DIO | I/O | Bidirectional data (NMOS open leakage), data input/output starts from the lower bit. Write serial data at the rising edge of the clock and read serial data at the rising edge of the clock. |
| 8 | CLK | I | The clock signal reads DIO pin data to the display RAM at the rising edge and outputs data to the DIO pin at the falling edge. |
| 9 | STB | I | Chip selection signal, high level disabled, low level enabled. |
| 10 | K0 | I | Key scanning input, the key signal is latched after the display cycle ends |
| 11,27 | VDD | VDD | Positive power supply |
| 12-19 | SEG1/KS1-SEG8/KS8 | O | LED SEG output (P-channel); Key scan output |
| 20-26 | SEG9-SEG15 | O | LED SEG output (P-channel) |

# 7 Functional Description

## 7.1 Block Diagram
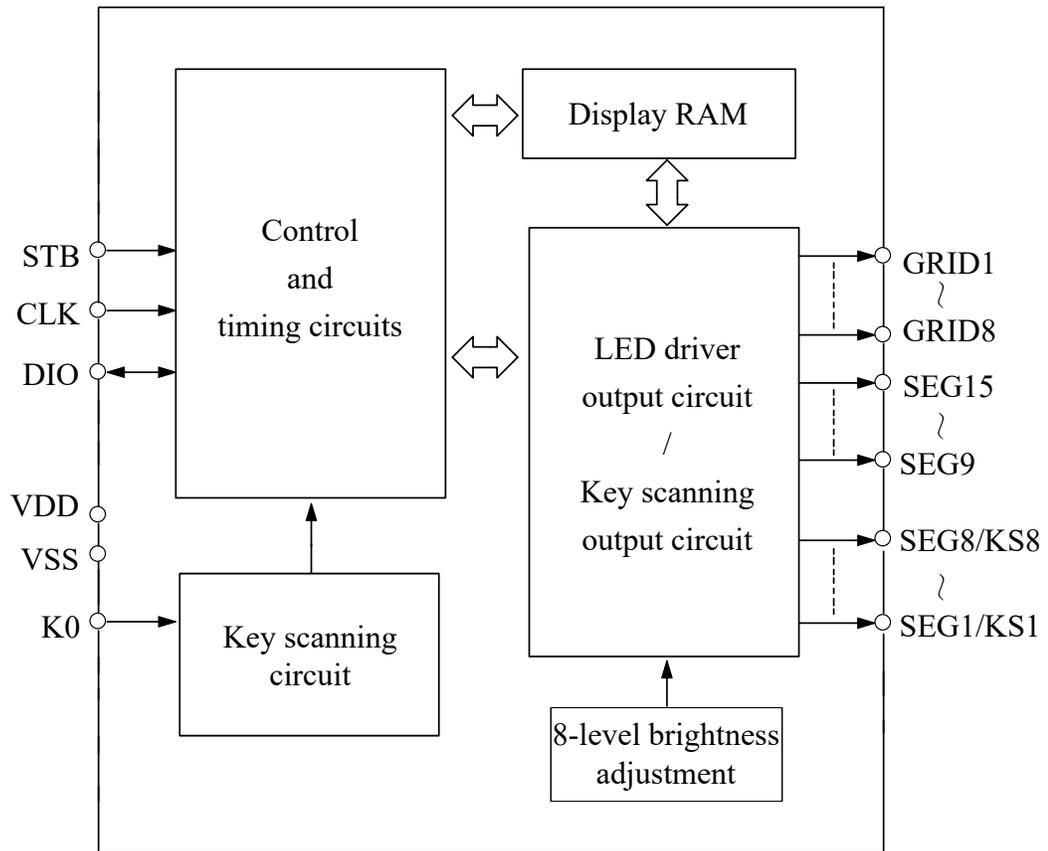
## 7.2 Display RAM- Storage Structure

The static display memory (RAM) has a structure of 16×8 bits and stores the displayed data. The content of RAM is directly mapped to the display content of the LED driver, with display addresses ranging from 0xC0 to 0xCF, and there are a total of 16 display units. If you want to turn on or off a certain LED, simply set the corresponding display RAM position 1 or clear 0. For example, to control the on/off of LED1 driven by pins SEG1 and GRID1, simply set the Bit0 position of the corresponding display RAM (address 0xC0) to 1 or clear 0. Clear the RAM bits corresponding to the unused SEG pins in the application to 0.

The process of mapping the contents in RAM to leds is shown in the following table:

| SEG\GRID | X | SEG15 | SEG14 | SEG13 | SEG12 | SEG11 | SEG10 | SEG9 | Addr | SEG8 | SEG7 | SEG6 | SEG5 | SEG4 | SEG3 | SEG2 | SEG1 | Addr | SEG\GRID |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| GRID1 | | | | | | | | | 0xC1 | | | | | | | | LED1 | 0xC0 | GRID1 |
| GRID2 | | | | | | | | | 0xC3 | | | | | | | | | 0xC2 | GRID2 |
| GRID3 | | | | | | | | | 0xC5 | | | | | | | | | 0xC4 | GRID3 |
| GRID4 | | | | | | | | | 0xC7 | | | | | | | | | 0xC6 | GRID4 |
| GRID5 | | | | | | | | | 0xC9 | | | | | | | | | 0xC8 | GRID5 |
| GRID6 | | | | | | | | | 0xCB | | | | | | | | | 0xCA | GRID6 |
| GRID7 | | | | | | | | | 0xCD | | | | | | | | | 0xCC | GRID7 |
| GRID8 | | | | | | | | | 0xCF | | | | | | | | | 0xCE | GRID8 |
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |

Note:

1. The value stored inside the chip display RAM at the moment of power-on may be random. It is recommended that the customer perform a power-on reset of the display RAM, that is, write all the data 0x00 to the 16-byte display RAM(address 0xC0-0xCF) after power-on.

2. The SEG pin can only be connected to the anode of the LED, and the GRID pin can only be connected to the cathode of the LED. They must not be reversed.

# 8    Key Scanning

## 8.1    Key Data Reading
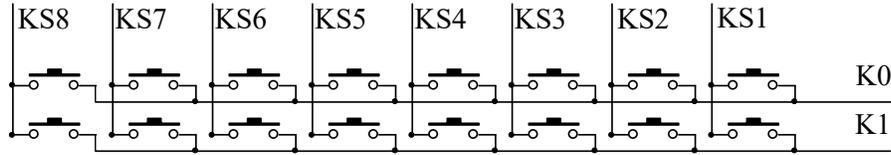


The key scanning is automatically completed by the hardware. Users only need to read the key values in sequence. It takes two display cycles to complete one key scan, with each display cycle approximately taking 4ms. Within 8ms, two different keys were pressed successively, and the key values read twice were those of the first pressed key.

After the host sends the command to read the key, it starts to read the 4-byte key data in sequence. The read key data is output from the lower bit. When a certain key is pressed, the bit position within the corresponding key data byte is 1.

The keys and their corresponding key data are as shown in the following figure:
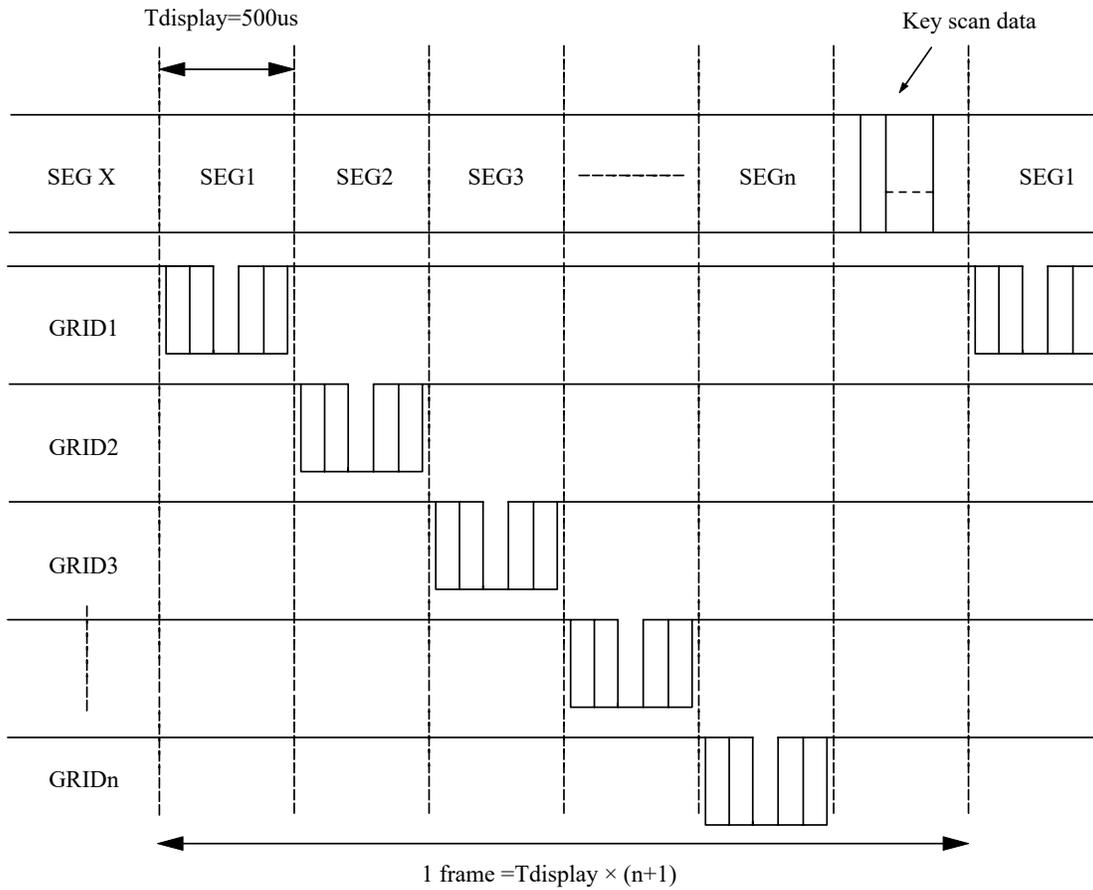
| Key data | K0 | X | X | X | K0 | X | X | X |
|---|---|---|---|---|---|---|---|---|
| Byte 1 | KS2 | | | | KS1 | | | |
| Byte 2 | KS4 | | | | KS3 | | | |
| Byte 3 | KS6 | | | | KS5 | | | |
| Byte 4 | KS8 | | | | KS7 | | | |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Note:
Reading key data must be done in sequence. Cross-byte reading is not allowed, and the reading should not exceed 4 bytes. Combination keys are not supported.

## 8.2 Key Scan Timing

The key scanning and display sequence diagram is as follows:



1 frame =Tdisplay × (n+1)

## 8.3 Key/Display Reuse
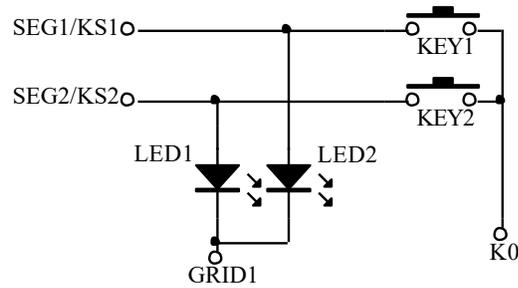


As shown in the above figure, for LED1 to be on and LED2 to be off, SEG1 needs to be in the "0" state and SEG2 in the "1" state. If KEY1 and KEY2 are pressed simultaneously, it is equivalent to SEG1 and SEG2 being short-circuited. At this time, both LED1 and LED2 will be on. This can be solved by connecting a diode in series or a resistor.

As shown in the following figure：
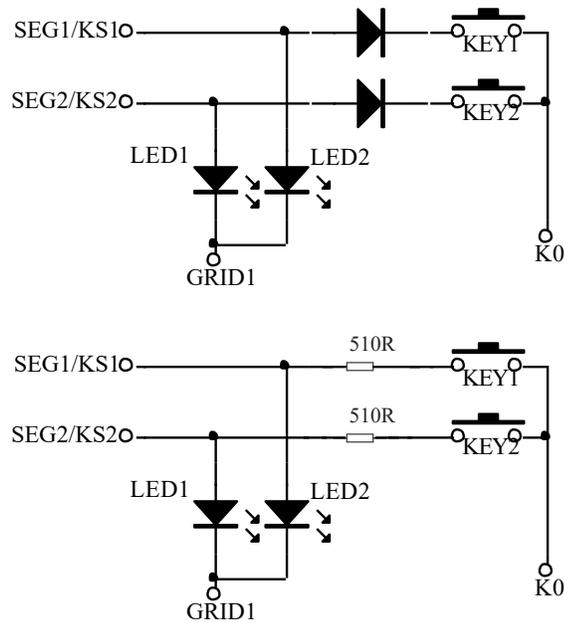




Note: The resistance value of the resistor should be selected at 510 ohms. If it is too high, it may cause the key to fail; if it is too low, it may not solve the problem of display interference.

# 9    Serial Communication Commands

## 9.1    Communication Interface

The VK1629B has three communication pins.

The STB pin signal is used to enable/disable communication with the main controller. A high STB level disables and initializes the internal timing, while a low STB level enables the first byte input from the DIO pin after the falling edge of the STB as an instruction. If the STB is set to a high level during instruction or data transmission, Then the serial communication is initialized, and the instructions or data being transmitted are invalid.

The CLK pin is the clock input pin. Data is written to the DIO pin at the rising edge to the display RAM, and data is read from the DIO pin at the rising edge.

DIO is a serial data input/output pin. Reading/writing data or writing commands must pass through the data pin, starting from the lower bit.

## 9.2    Command Format

Commands are used to set the display mode, write display data and read key values.

The first byte input by DIO after the falling edge of STB is taken as the command. After decoding, the highest two bits, 7 and 6, are selected to distinguish different commands, as shown in the following table:

| bit7 | bit6 | Function |
|------|------|----------|
| 0 | 1 | Data read and write setting command |
| 1 | 0 | Display control command |
| 1 | 1 | Address setting command |

## 10    Command Description

### 10.1  Display Mode Setting Command

This command is used for LED display data writing and key reading as well as related commands. bit1 and bit0 bits are not allowed to be set to 01 or 11.

When powered on, the bit3-bit0 data is 0.

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Function | Note |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 |  |  |  |  | 0 | 0 | Data read and write mode Settings | Write data to display register |
| 0 | 1 |  |  |  |  | 1 | 0 |  | Read the key data |
| 0 | 1 | --- |  |  | 0 |  |  | Address increase mode Settings | Automatic address increment |
| 0 | 1 |  |  |  | 1 |  |  |  | Fixed address |
| 0 | 1 |  |  | 0 |  |  |  | Working mode Settings | Normal mode |
| 0 | 1 |  |  | 1 |  |  |  |  | Test mode |

### 10.2  Address Setting Command

Set the address of the displayed RAM (0×C0-0×CD). When powered on, the address is set to 0×C0 by default.
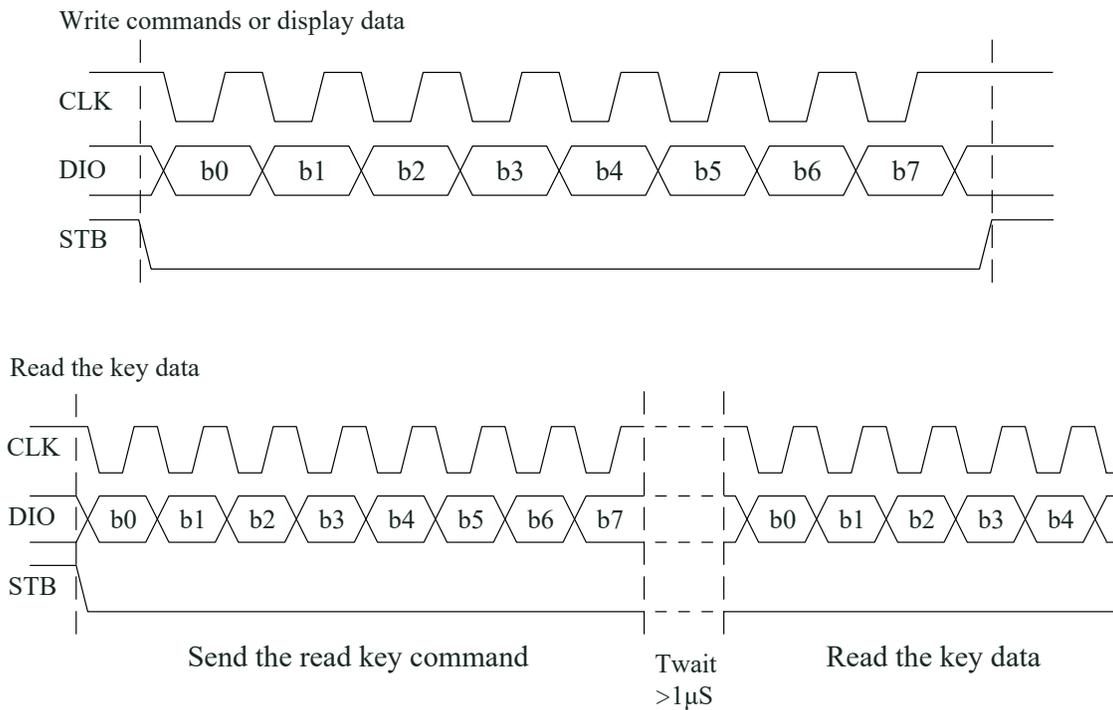
| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Display RAM address |
|---|---|---|---|---|---|---|---|---|
| 1 | 1 |  |  | 0 | 0 | 0 | 0 | 0xC0 |
| 1 | 1 |  |  | 0 | 0 | 0 | 1 | 0xC1 |
| 1 | 1 |  |  | 0 | 0 | 1 | 0 | 0xC2 |
| 1 | 1 |  |  | 0 | 0 | 1 | 1 | 0xC3 |
| 1 | 1 |  |  | 0 | 1 | 0 | 0 | 0xC4 |
| 1 | 1 |  |  | 0 | 1 | 0 | 1 | 0xC5 |
| 1 | 1 |  |  | 0 | 1 | 1 | 0 | 0xC6 |
| 1 | 1 | --- |  | 0 | 1 | 1 | 1 | 0xC7 |
| 1 | 1 |  |  | 1 | 0 | 0 | 0 | 0xC8 |
| 1 | 1 |  |  | 1 | 0 | 0 | 1 | 0xC9 |
| 1 | 1 |  |  | 1 | 0 | 1 | 0 | 0xCA |
| 1 | 1 |  |  | 1 | 0 | 1 | 1 | 0xCB |
| 1 | 1 |  |  | 1 | 1 | 0 | 0 | 0xCC |
| 1 | 1 |  |  | 1 | 1 | 0 | 1 | 0xCD |
| 1 | 1 |  |  | 1 | 1 | 1 | 0 | 0xCE |
| 1 | 1 |  |  | 1 | 1 | 1 | 1 | 0xCF |

## 10.3   Display Control Command

Set the display switch and select the display brightness (8 levels).

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Function | Note |
|------|------|------|------|------|------|------|------|----------|------|
| 1 | 0 | | | | 0 | 0 | 0 | | Set the pulse width to 1/16 |
| 1 | 0 | | | | 0 | 0 | 1 | | Set the pulse width to 2/16 |
| 1 | 0 | | | | 0 | 1 | 0 | | Set the pulse width to 4/16 |
| 1 | 0 | | | | 0 | 1 | 1 | Set the | Set the pulse width to 10/16 |
| 1 | 0 | --- | | | 1 | 0 | 0 | pulse width | Set the pulse width to 11/16 |
| 1 | 0 | | | | 1 | 0 | 1 | | Set the pulse width to 12/16 |
| 1 | 0 | | | | 1 | 1 | 0 | | Set the pulse width to 13/16 |
| 1 | 0 | | | | 1 | 1 | 1 | | Set the pulse width to 14/16 |
| 1 | 0 | | | 0 | | | | Display switch | Show off |
| 1 | 0 | | | 1 | | | | | Display on |

## 10.4   Command Timing

Write commands or display data



Read the key data



Send the read key command          Twait >1μS          Read the key data

# 11    Command Application

## 11.1    Send Display Data (address automatically adds 1)

To transfer display data using the address auto-increment mode, first set the starting address of the data to be transferred (corresponding to the display RAM address). After the starting address command word is sent, the STB does not need to be set high and can directly transmit the display data, with a maximum of 16 sections. After the data is transmitted, the STB is set high, and the display data is output starting from the lower bit.
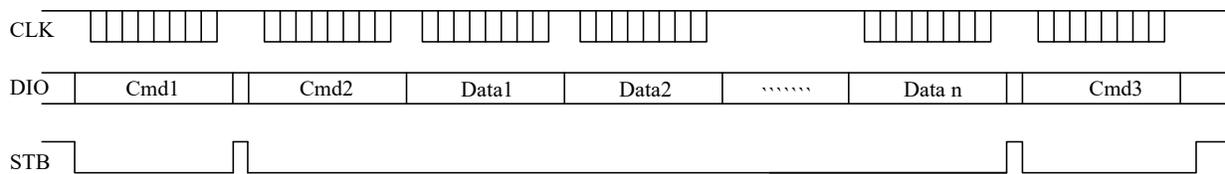


Cmd1: Data Read and Write Setting Command - Set Address to Increase automatically (0×40)
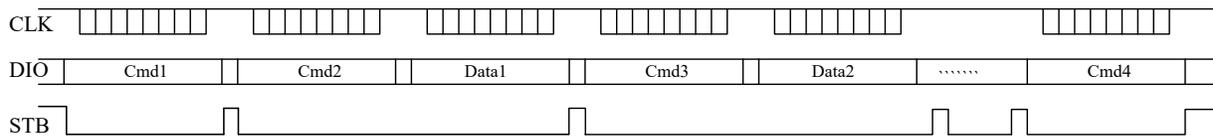
Cmd2: Address Setting Command - Set the display RAM starting address (0×C0-0×CF)

Data1-Datan: Send the display data to the starting address set by Cmd2 and the subsequent display RAM (up to 16 bytes)

Cmd3: Display Control Command - Display on and set the display brightness level

## 11.2 Send Display Data (fixed address)

To transfer display data using the fixed address mode, first set the address of the data to be transferred (corresponding to the display RAM address). After the address is sent, the STB does not need to be set high and can directly transfer 1 byte of display data. After the data is transferred, the STB is set high. Send the address of the next display data. The STB does not need to be set high and can directly send 1 byte of display data. After the data is transmitted, the STB is set high. ... Until the last byte of the display data is transmitted, up to a maximum of 16 bytes, the display data is output starting from the lower bit.



Cmd1: Data Read and Write Settings Command - Set Fixed Address Mode (0×44)

Cmd2: Address Setting Command - Set display RAM Address (0×C0-0×CF)

Data1: Send display data to the display RAM address set by Cmd2

Cmd3: Address Setting Command - Set display RAM Address (0×C0-0×CF)

Data2: Send display data to the display RAM address.... set by Cmd3 A maximum of 16 bytes of data can be transmitted

Cmd4: Display Control Command - Display on and set Display Brightness Level (0×88|0×85)

## 11.3 Read The Key Data

The data read and write setting command is set to read key data, and then starts to read 4 bytes of key data in sequence. The read key data is output starting from the lower bit.
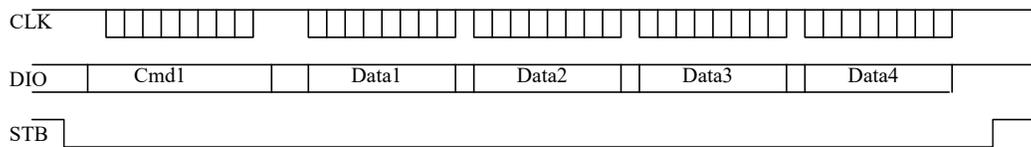


Cmd1: Display Mode Setting Command - Set to read key data (0×42)

Data1-Data4: Read 4 bytes of key data in sequence, and output the key data starting from the lower bit.

永嘉微电
Vinka Microelectronics

# 12 Application Circuits

When the surrounding interference is relatively large, a 10R to 10k resistor and a PF-level small capacitor to ground can be connected in series on the communication pin. When the power supply of the single-chip microcomputer (3.3V) and the driver chip (5V) is inconsistent, it is recommended to add a level conversion circuit on the communication pin
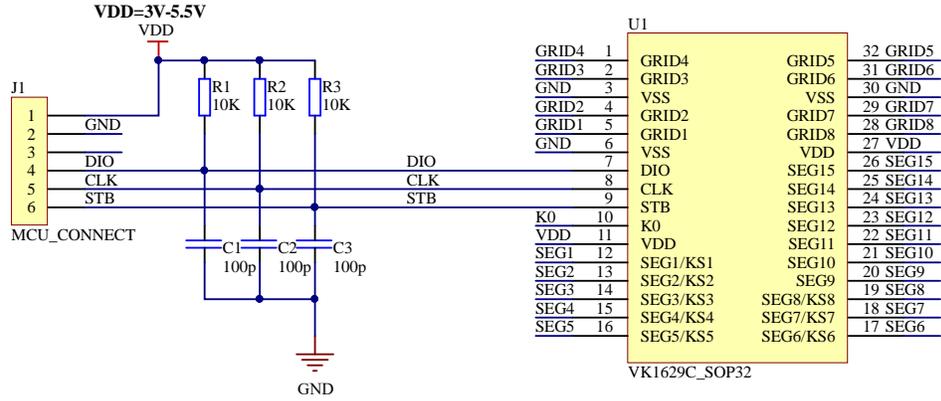
The filter capacitor between VDD and GND should be placed as close to the chip as possible on the PCB board to enhance the filtering effect.
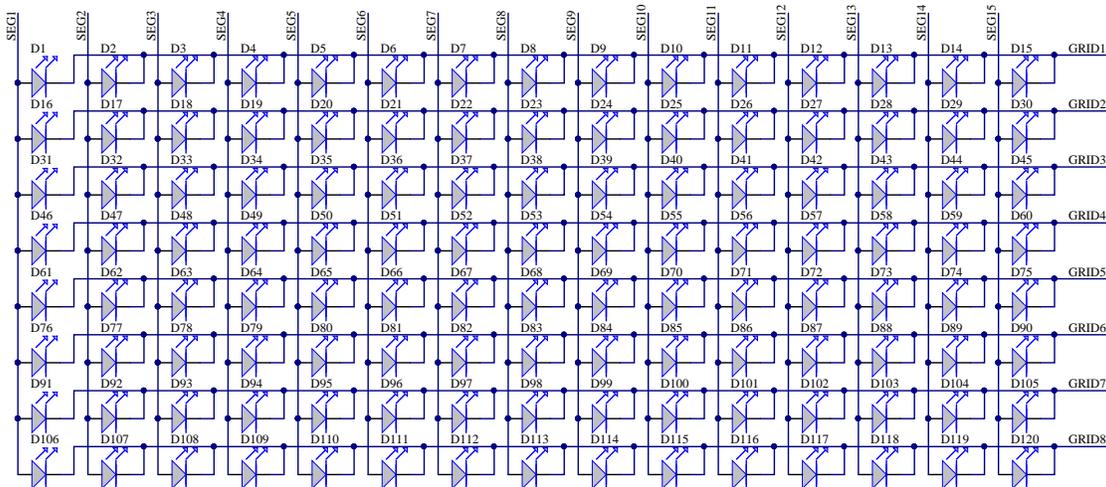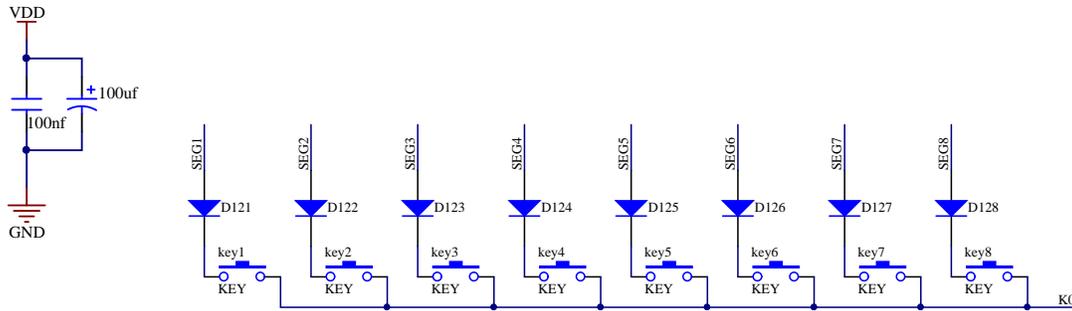
Connect the SEG pin to the anode of the LED and the GRID pin to the cathode of the LED

## 13 Electrical Characteristics

### 13.1 Absolute Maximum Ratings

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | VDD | -0.5～7.0 | V |
| Input Voltage | VIN | VSS-0.5～VDD+0.5 | V |
| Storage Temperature | $T_{STG}$ | -50～+125 | °C |
| Operating Temperature | $T_{OTG}$ | -40～+80 | °C |

### 13.2 DC Electrical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions VDD | Conditions |
|---|---|---|---|---|---|---|---|
| Operating voltage | VDD | 3.0 | — | 5.5 | V | — | — |
| Static current | IDD | — | 0.5 | 1.0 | mA | 5V | No load /LED off |
| High-level output current | $I_{OHSEG1}$ | -20 | -25 | -40 | mA | 5V | VO=VDD-2V SEG1- SEG15 |
| | $I_{OHSEG2}$ | -25 | -30 | -50 | | 5V | VO=VDD-3V SEG1- SEG15 |
| Low-level input current | $I_{OLGRID}$ | 80 | 120 | — | mA | 5V | VO=0.3V GRID1- GRID8 |
| High-level output current tolerance | $I_{TOLSEG}$ | — | — | 5 | % | VDD | VO=VDD-3V(VDD=5V) VO=VDD-2V(VDD=3V) SEG1-SEG15 |
| Low-level Input | $V_{IL}$ | 0 | — | 0.3 | VDD | VDD | STB,CLK,DIO |
| High-level Input | $V_{IH}$ | 0.7 | — | 1.0 | | VDD | |
| Pull-down resistor | $R_L$ | — | 10 | — | kΩ | 5V | K0 |

## 13.3  AC Electrical Characteristics

Switch parameter

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Oscillation frequency | $F_{OSC}$ | — | 500 | — | KHz | |
| Transmission delay time | $t_{PLZ}$ | — | — | 300 | nS | CLK→DOUT CL=15pF,RL=10KΩ |
| | $P_{ZL}$ | — | — | 100 | nS | |
| Rising time | $t_{ZH1}$ | — | — | 2 | μS | CL=300pF SEG1-SEG15 GRID1-GRID8 |
| | $t_{TZH2}$ | — | — | 0.5 | μS | CL=300pF GRID1-GRID8 |
| Decrease time | $t_{THZ}$ | — | — | 120 | μS | CL = 300pF SEGn,GRIDn |
| Maximum input clock frequency | $F_{MAX}$ | — | — | 1 | MHz | Duty cycle: 50% |
| Input capacitance | $C_I$ | — | — | 15 | pF | — |

Timing parameter

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Clock pulse width | $P_{WCLK}$ | 400 | — | — | nS | — |
| Select pulse width | $P_{WSTB}$ | 1 | — | — | μS | — |
| Data establishment time | $t_{SETUP}$ | 100 | — | — | nS | — |
| Data retention time | $t_{HOLD}$ | 100 | — | — | nS | — |
| CLK→STB time | $t_{CLK-STB}$ | 1 | — | — | μS | CLK↑→STB↑ |
| Waiting time | $T_{wait}$ | 1 | — | — | μS | CLK↑→CLK↓ |
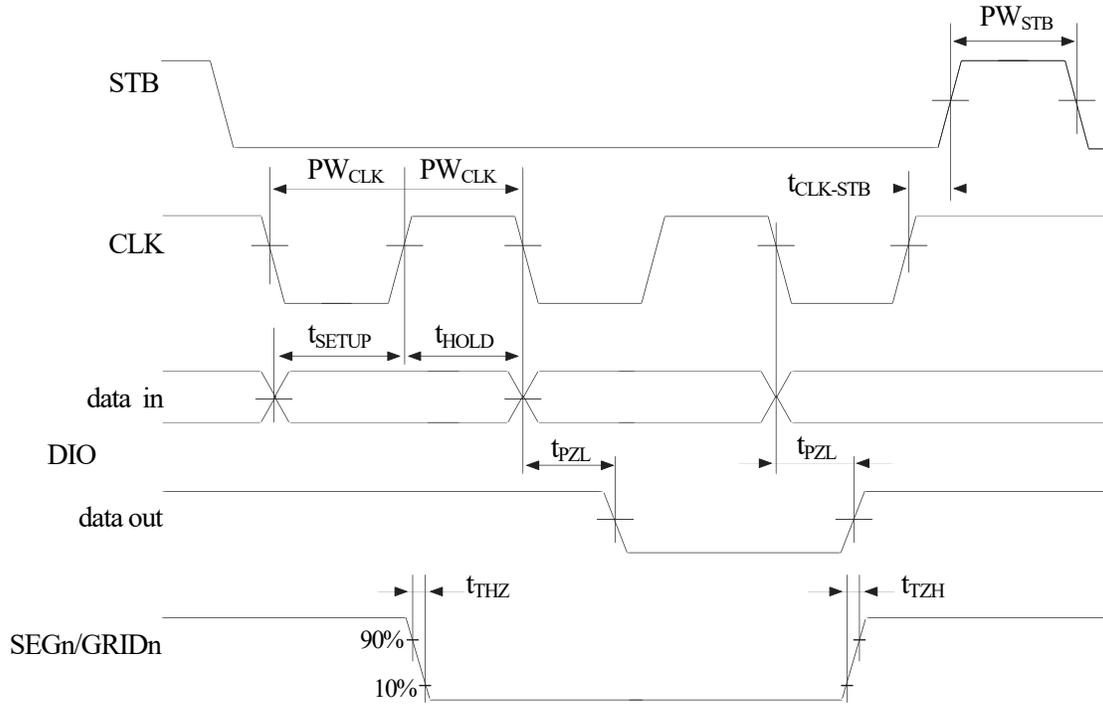
## 14 Package Information

### 14.1 SOP32（21.00mm × 7.50mm PP=1.27mm）



DETALL:"X"
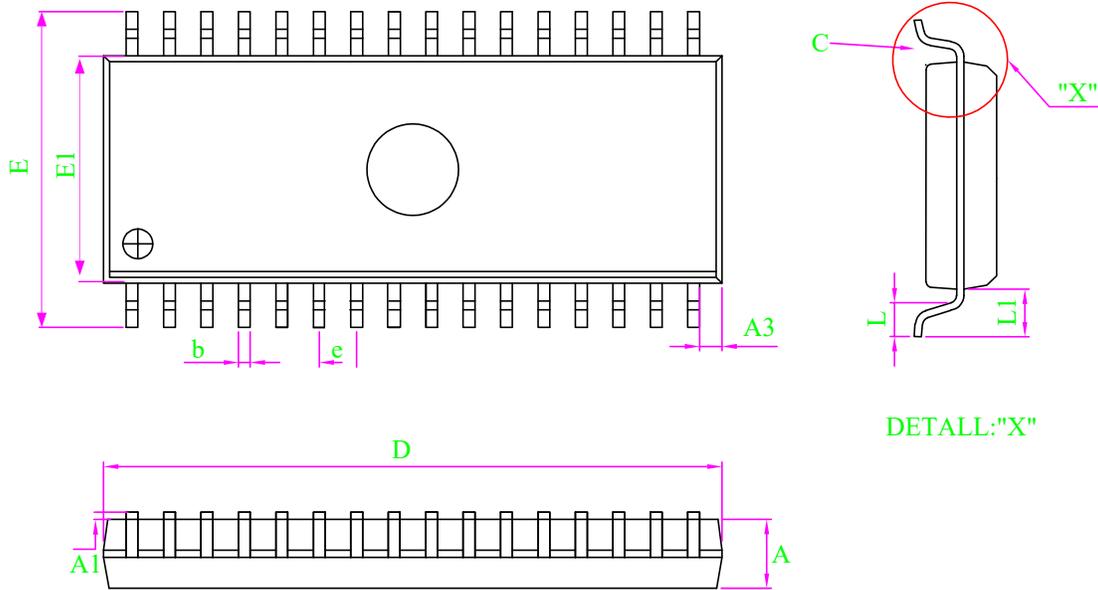
| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | - | - | 2.34 |
| A1 | 0.10 | 0.20 | 0.25 |
| b | 0. 30 | - | 0. 50 |
| b1 | 0.27 | 0.30 | 0.33 |
| c | 0.13 | - | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 20.90 | 21.00 | 21.10 |
| E | 10.2 | 10.4 | 10.6 |
| E1 | 7.40 | 7.50 | 7.60 |
| e | 1.27BSC | | |
| θ | 0 | - | 8° |
| L | 0. 70 | - | 1. 00 |
| L1 | 1.40REF | | |

# 15 Disclaimer

**Warranty and liability** —— The information provided in this document is believed to be accurate and reliable. However, Shenzhen Vinka Microelectronics Co., Ltd. (hereinafter "the Company") makes no warranties, express or implied, as to the completeness or suitability of this information for any specific purpose.

In no event shall the Company be liable for any indirect, incidental, or consequential damages, including but not limited to loss of profits, equipment damage, or system failure, arising out of the use of this product or documentation, regardless of the legal theory under which such liability is asserted.

**Right to change** —— The Company reserves the right to modify any information contained herein without prior notice. The latest version of this document is available at: https://www.szvinka.com/

**Applicability** —— This product is not designed or intended for use in life-critical, medical, or safety systems where failure could result in injury or death. The customer shall assume full responsibility for any such use.

**Application** —— All product application descriptions provided herein are intended for illustrative purposes only.
The Company makes no representations or warranties, express or implied, regarding the suitability of any specific application without further testing or modification.

The customer is solely responsible for determining whether the Company's products are appropriate for their intended applications or end customers.

The customer shall ensure proper design practices, implementation safeguards, and operational validation to minimize risks associated with product use.

The Company shall not be held liable for any defects, losses, costs, or damages arising from weaknesses or failures in the customer's own products or applications, or from the integration or use of third-party products.

Furthermore, the customer shall conduct all necessary testing and validation for any third-party deployment of the Company's products to avoid potential misuse or associated damages. The Company assumes no liability in this regard.

**Commercial terms of sale** —— Unless otherwise agreed in writing, sales of this product are subject to the Company's standard terms and conditions of sale. The Company expressly rejects the applicability of the customer's general terms and conditions.

**Export control** —— This product may be subject to applicable export control regulations. The customer is solely responsible for compliance with such regulations, including obtaining any necessary export licenses.

## 16  Revision History

| No. | Version | Date | Modify the content | Check |
|-----|---------|------|--------------------|-------|
| 1 | 1.0 | 2018-08-10 | Initial release | YES |
| 2 | 1.1 | 2018-10-11 | Add reference circuit | YES |
| 3 | 1.2 | 2019-03-21 | Alignment correction | YES |
| 4 | 1.3 | 2025-10-11 | Change Description | YES |

[1] Please refer to the latest version of this document before starting or finalizing any design.

[2] Since the release of this document, the status or availability of this product may have changed. For the most up-to-date information, please visit: https://www.szvinka.com/