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Vinka Microelectronics

VK1629A Datasheet

16×8 LED DRIVER

Rev.1.3

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1 General Description

VK1629A is a dedicated chip for digital tube or dot matrix LED driver control, which integrates a 3-wire serial interface, data latch, LED driver and other circuits internally. The SEG pin is connected to the anode of the LED, and the GRID pin is connected to the cathode of the LED, which can support a dot matrix LED display panel of 16SEG×8GRID. High-end display screen drivers suitable for products such as refrigerators, air conditioners, and home theaters. It adopts the SOP32 packaging form.

2 Key Features

- Operating voltage：3.0-5.5V
- Built-in RC oscillator
- 16 SEG pins, 8 GRID pins
- The SEG pin can only be connected to the anode of the LED, and the GRID pin can only be connected to the cathode of the LED
- 3-wire serial interface
- The overall brightness is adjustable at 8 levels
- The built-in display RAM is 16×8 bits
- Built-in power-on reset circuit
- Available Packages:
  SOP32 （21.00mm × 7.50mm PP=1.27mm)

3 Application Field

- Small household appliances
- Induction cooker/microwave oven
- Pressure gauge

4 Product Selection

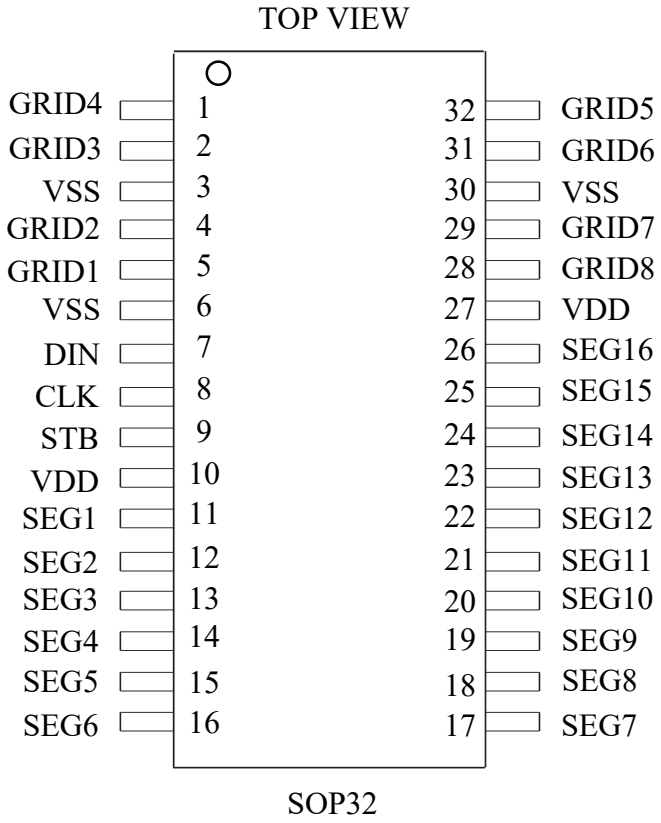
Part No.	Common Cathode Drive	Common Anode Drive	Key press	Packaging
VK1S38A	8 / 8	8 / 8	8×3	SSOP24
VK1638	10 / 8	8 / 10	8×3	SOP28
VK1629A	16 / 8	8 / 16	---	SOP32
VK1629B	14 / 8	8 / 14	8×2	SOP32
VK1629C	15 / 8	8 / 15	8×1	SOP32
VK1629D	12 / 8	8 / 12	8×4	SOP32
VK1629	16 / 8	8 / 16	8×4	LQFP44
VK6932	8 / 16	16 / 8	---	SOP32

Note: For both common cathode and common anode digital tubes, SEG is connected to the anode and GRID to the cathode.

5 Ordering Information

Part No.	Packaging	Tube Qty	Tray(reel) Qty	Box Qty	Total Qty	Notes
VK1S38A	SSOP24	60/tube		6000/box	20800 PCS	
VK1638	SOP28	26/tube		2080/box	16000 PCS	
VK1629A	SOP32	20/tube		1600/box	16000 PCS	
VK1629B	SOP32	20/tube		1600/box	16000 PCS	
VK1629C	SOP32	20/tube		1600/box	16000 PCS	
VK1629D	SOP32	20/tube		1600/box	16000 PCS	
VK1629	LQFP44		160/tray	1600/box	16000 PCS	
VK6932	SOP32	20/tube		1600/box	16000 PCS	

6 Package Pinout Information(SOP32)



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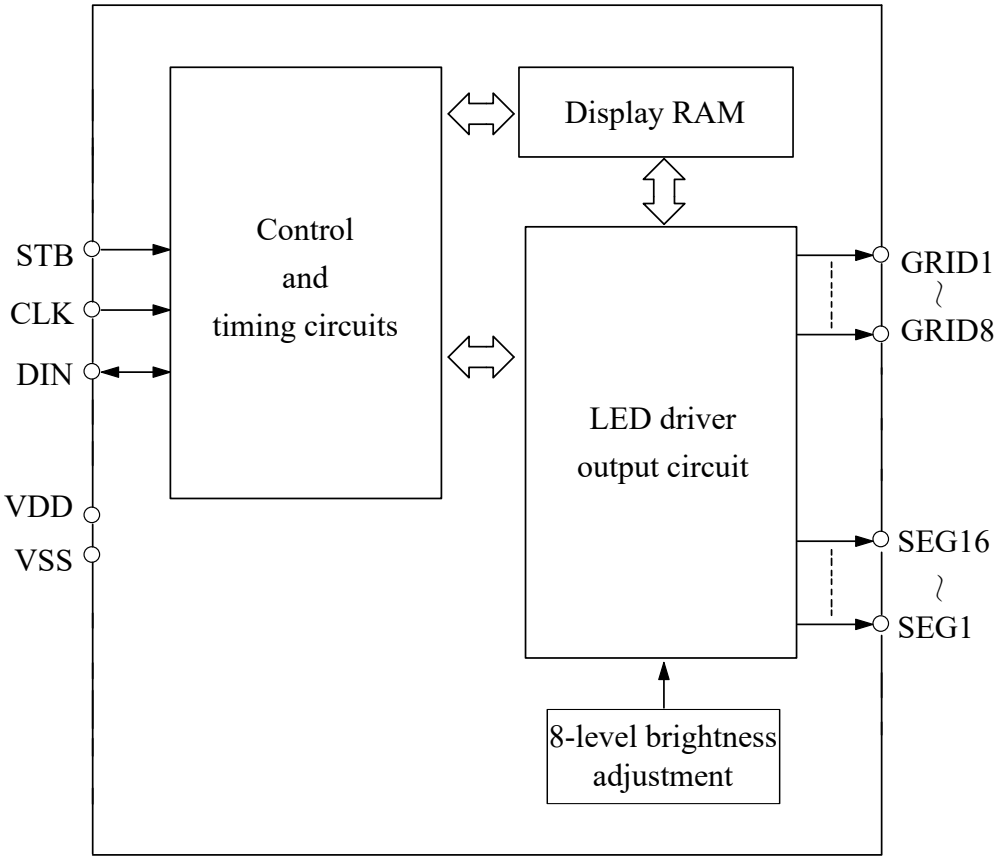
6.1 VK1629A/SOP32 Pin Description

No.	Name	I/O	Function
1-2,4-5 32-31 29-28	GRID1-GRID8	O	LED GRID output (N-channel open-drain output)
3，6 30	VSS	VSS	Negative power supply
7	DIN	I	The data input pin writes serial data at the rising edge of the clock, and the data is input starting from the lower bit.
8	CLK	I	The clock signal reads DIO pin data to the display RAM at the rising edge and outputs data to the DIO pin at the falling edge.
9	STB	I	Chip selection signal, high level disabled, low level enabled.
10,27	VDD	VDD	Positive power supply
11-26	SEG1-SEG16	O	LED SEG output (P-channel)

7 Functional Description

7.1 Block Diagram



7.2 Display RAM- Storage Structure

The static display memory (RAM) has a structure of 16×8 bits and stores the displayed data. The content of RAM is directly mapped to the display content of the LED driver, with the display address being 0×C0-0×CF, and there are a total of 16 display units. If you want to turn on or off a certain LED, simply set the corresponding display RAM position to 1 or clear to 0. For example, to control the on/off of LED1 driven by pins SEG1 and GRID1, simply set the bit0 position of the corresponding display RAM (address 0×C0) to 1 or clear to 0. Clear the RAM bits corresponding to the unused SEG pins in the application to 0.

The process of mapping the contents in RAM to leds is shown in the following table:

SEG GRID	SEG16	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	Addr	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	Addr	SEG GRID
GRID1									0xC1									0xC0	GRID1
GRID2									0xC3									0xC2	GRID2
GRID3									0xC5									0xC4	GRID3
GRID4									0xC7									0xC6	GRID4
GRID5									0xC9									0xC8	GRID5
GRID6									0xCB									0xCA	GRID6
GRID7									0xCD									0xCC	GRID7
GRID8									0xCF									0xCE	GRID8
	D7	D6	D5	D4	D3	D2	D1	D0		D7	D6	D5	D4	D3	D2	D1	D0		

Note:

1. The value stored inside the chip display RAM at the moment of power-on may be random. It is recommended that the customer perform a power-on reset of the display RAM, that is, write all the data 0×00 to the 16-byte display RAM(address 0×C0-0×CF) after power-on.
2. The SEG pin can only be connected to the anode of the LED, and the GRID pin can only be connected to the cathode of the LED. They must not be reversed.

8 Serial Communication Commands

8.1 Communication Interface

The VK1629A has three communication pins.

The STB pin signal is used to enable/disable communication with the main controller. A high STB level disables and initializes the internal timing, while a low STB level enables the first byte input from the DIN pin after the falling edge of the STB as an instruction. If the STB is set to a high level during instruction or data transmission, Then the serial communication is initialized, and the instructions or data being transmitted are invalid.

The CLK pin is the clock input pin, and data is written to the DIN pin on the rising edge to the display RAM.

DIN is a serial data input pin. Writing data or commands must be done through the data pin, starting from the lower bit.

8.2 Command Format

Commands are used to set the display mode and write display data.

The first byte input by DIN after the falling edge of STB is taken as the command. After decoding, the highest bits 7 and 6 are selected to distinguish different commands, as shown in the following table:

bit7	bit6	Function
0	1	Data write setting command
1	0	Display control command
1	1	Address setting command

9 Command Description

9.1 Display Mode Setting Command

This command is used for LED display data writing and related commands. bit1 and bit0 bits are not allowed to be set to 01 or 11.

When powered on, the bit3-bit0 data is 0.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Function	Note
0	1	---				0	0	Data writing	Write the data to display register
0	1				0			Address increase mode Settings	Address increases automatically
0	1				1				Fixed address
0	1			0				Working mode Settings	Normal mode
0	1			1					Test mode

9.2 Address Setting Command

Set the address of the displayed RAM (0×C0-0×CF). When powered on, the address is set to 0×C0 by default.

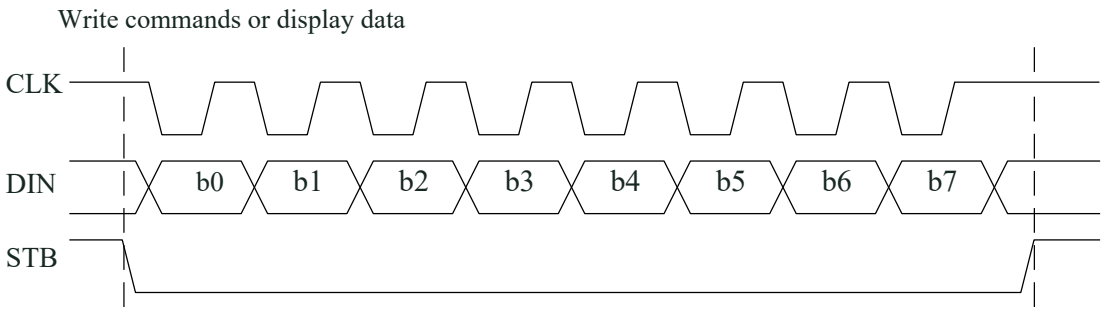
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Display RAM address
1	1	---		0	0	0	0	0xC0
1	1			0	0	0	1	0xC1
1	1			0	0	1	0	0xC2
1	1			0	0	1	1	0xC3
1	1			0	1	0	0	0xC4
1	1			0	1	0	1	0xC5
1	1			0	1	1	0	0xC6
1	1			0	1	1	1	0xC7
1	1			1	0	0	0	0xC8
1	1			1	0	0	1	0xC9
1	1			1	0	1	0	0xCA
1	1			1	0	1	1	0xCB
1	1			1	1	0	0	0xCC
1	1			1	1	0	1	0xCD
1	1			1	1	1	0	0xCE
1	1			1	1	1	1	0xCF

9.3 Display Control Command

Set the display switch and select the display brightness (8 levels).

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Function	Note
1	0	---			0	0	0	Set the pulse width	Set the pulse width to 1/16
1	0				0	0	1		Set the pulse width to 2/16
1	0				0	1	0		Set the pulse width to 4/16
1	0				0	1	1		Set the pulse width to 10/16
1	0				1	0	0		Set the pulse width to 11/16
1	0				1	0	1		Set the pulse width to 12/16
1	0				1	1	0		Set the pulse width to 13/16
1	0				1	1	1		Set the pulse width to 14/16
1	0			0				Display switch	Show off
1	0			1					Display on

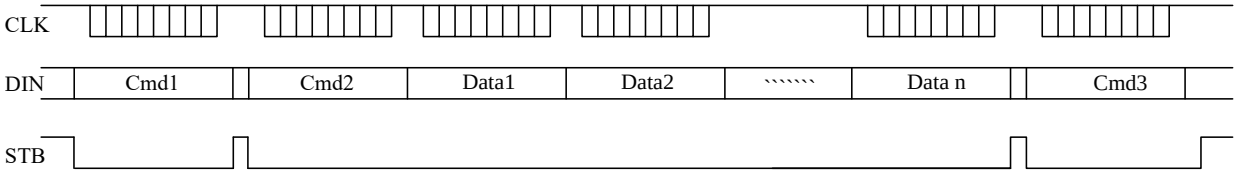
9.4 Command Timing



10 Command Application

10.1 Send Display Data (address automatically adds 1)

To transfer display data using the address auto-increment mode, first set the starting address of the data to be transferred (corresponding to the display RAM address). After the starting address command word is sent, the STB does not need to be set high and directly transmits the display data, with a maximum of 16 bytes. After the data is transmitted, the STB is set high, and the display data is output starting from the lower bit.



Cmd1: Data Write Setting Command - Set address to increase automatically (0×40)

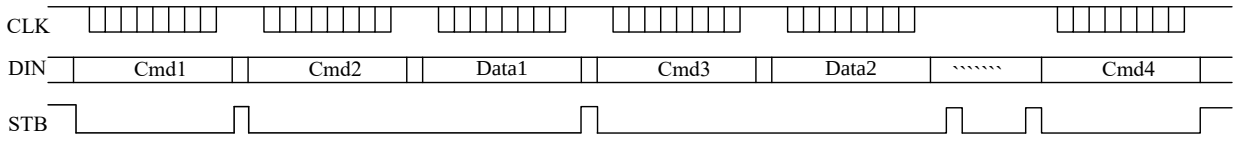
Cmd2: Address Setting Command - Set the display RAM starting address (0×C, 0-0×CF)

Data1-Datan: Send the display data to the starting address set by Cmd2 and the subsequent display RAM (up to 16 bytes)

Cmd3: Display Control Command - Display on and set Display Brightness Level (0×88|0×85)

10.2 Send Display Data (fixed address)

When transmitting display data using the fixed address mode, first set the address of the data to be transmitted (corresponding to the display RAM address). After the address is sent, the STB does not need to be set high and can directly transmit 1 byte of display data. After the data is transmitted, the STB is set high. Send the address of the next display data. The STB does not need to be set high and can directly send 1 byte of display data. After the data is transmitted, the STB is set high. ... Until the last byte of the display data is transmitted, up to a maximum of 16 bytes, the display data is output starting from the lower bit.



Cmd1: Data Write Setting Command - Set Fixed Address Mode (0×44)

Cmd2: Address Setting Command - Set display RAM Address (0×C, 0-0×CF)

Data1: Send display data to the display RAM address set by Cmd2

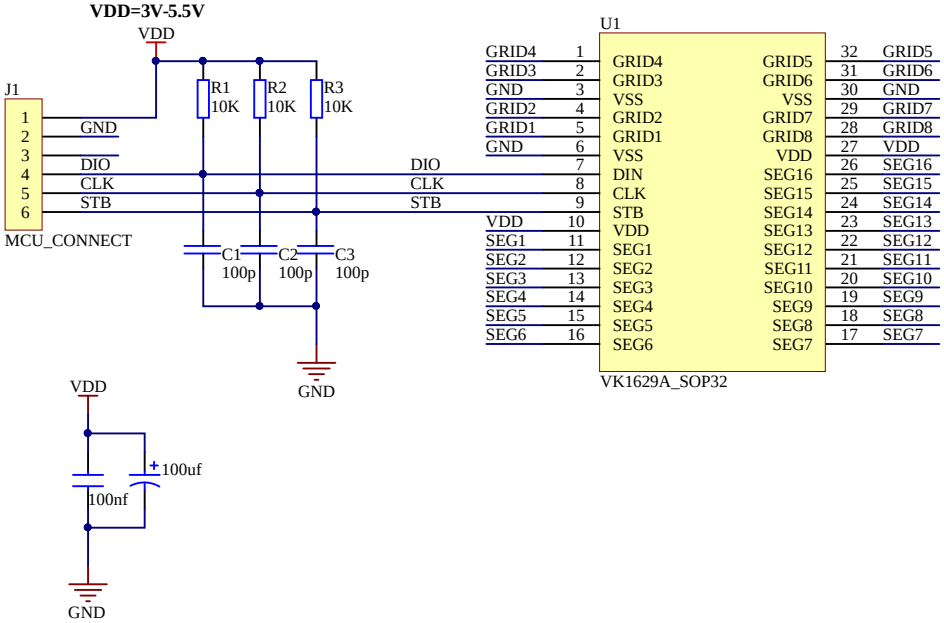
Cmd3: Address Setting Command - Set display RAM Address (0×C, 0-0×CF)

Data2: Send display data to the display RAM address.... set by Cmd3 A maximum of 16 bytes of data can be transmitted

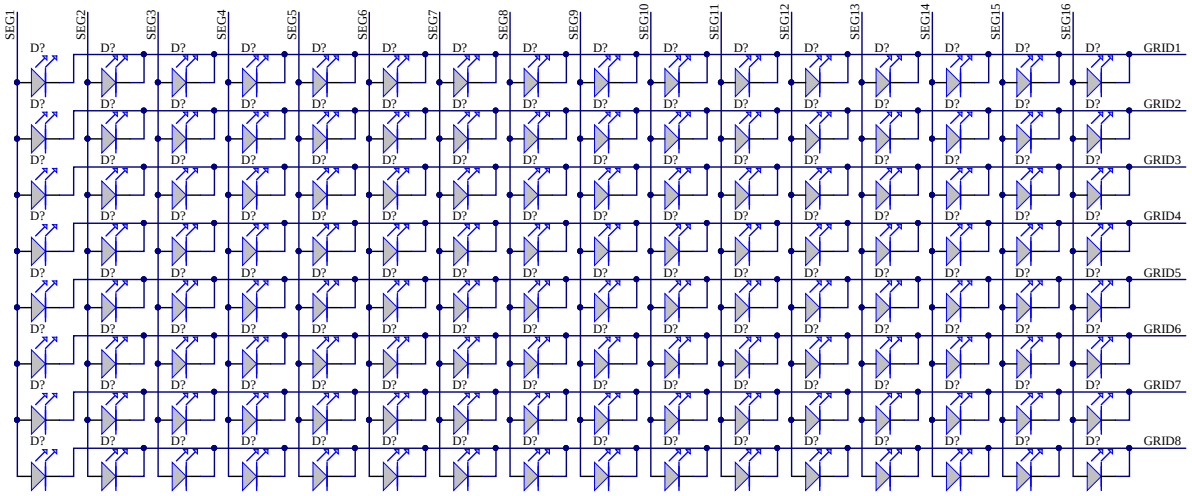
Cmd4: Display Control Command - Display on and set Display Brightness Level (0×88|0×85)

11 Application Circuits

When the surrounding interference is relatively large, a 10R to 10k resistor and a PF-level small capacitor to ground can be connected in series on the communication pin. When the power supply of the single-chip microcomputer (3.3V) and the driver chip (5V) is inconsistent, it is recommended to add a level conversion circuit on the communication pin



The filter capacitor between VDD and GND should be placed as close to the chip as possible on the PCB board to enhance the filtering effect.



Connect the SEG pin to the anode of the LED and the GRID pin to the cathode of the LED

12 Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.5～7.0	V
Input Voltage	VIN	VSS-0.5～VDD+0.5	V
Storage Temperature	TSTG	-60～+150	℃
Operating Temperature	TOTG	-40～+80	℃

12.2 DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	3.0	—	5.5	V	—	—
Static current	IDD	—	0.5	1.0	mA	5V	No load /LED off
High-level output current	IOHSEG1	-20	-25	-40	mA	5V	VO=VDD-2V SEG1- SEG16
	IOHSEG2	-25	-30	-50			VO=VDD-3V SEG1- SEG16
Low-level input current	IOLGRID	80	120	—	mA	5V	VO=0.3V GRID1-GRID8
High-level output current tolerance	ITOLSEG	—	—	5	%	VDD	VO=VDD-3V(VDD=5V) VO=VDD-2V(VDD=3V) SEG1-SEG16
Low-level Input	VIL	0	—	0.3	VDD	VDD	STB, CLK, DIN
High-level Input	VIH	0.7	—	1.0		VDD	

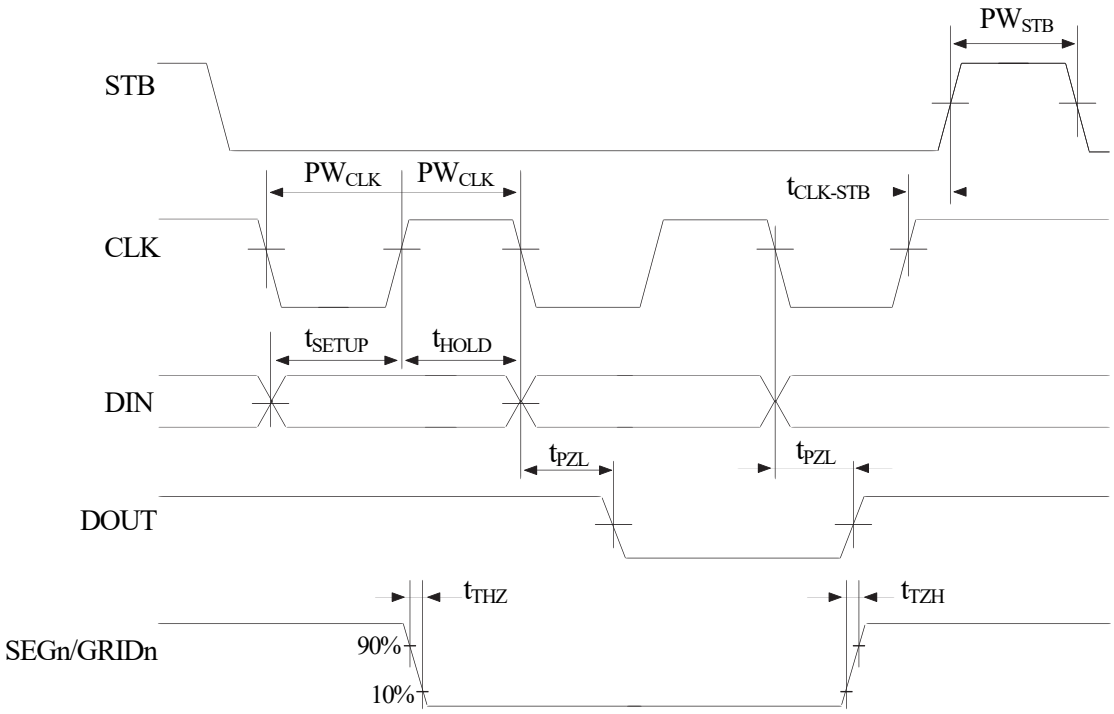
12.3 AC Electrical Characteristics

Switch parameter

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Oscillation frequency	F_{OSC}	—	500	—	KHz	
Transmission delay time	t_{PLZ}	—	—	300	nS	CLK→DOUT CL=15pF,RL=10KΩ
	P_{ZL}	—	—	100	nS	
Rising time	t_{ZH1}	—	—	2	μS	CL=300pF SEG1-SEG16 GRID1-GRID8
	t_{TZH2}	—	—	0.5	μS	CL=300pF GRID1-GRID8
Decrease time	t_{THZ}	—	—	120	μS	CL = 300pF SEGn,GRIDn
Maximum input clock frequency	F_{MAX}	—	—	1	MHz	Duty cycle: 50%
Input capacitance	C_I	—	—	15	pF	—

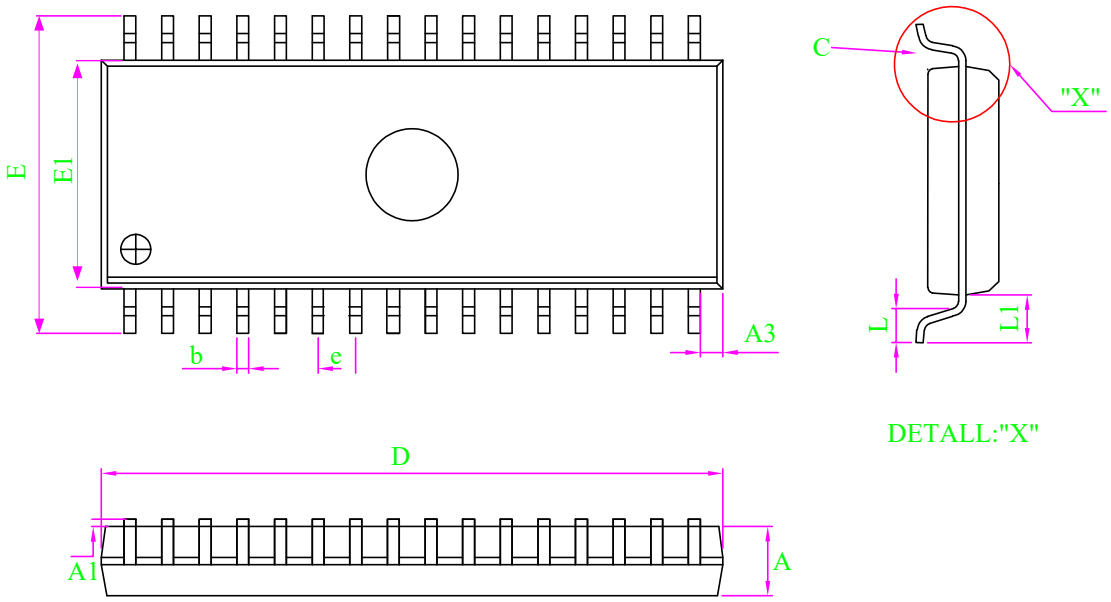
Timing parameter

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Clock pulse width	P_{WCLK}	400	—	—	nS	—
Select pulse width	P_{WSTB}	1	—	—	μS	—
Data establishment time	t_{SETUP}	100	—	—	nS	—
Data retention time	t_{HOLD}	100	—	—	nS	—
CLK→STB time	$t_{CLK-STB}$	1	—	—	μS	CLK↑→STB↑
Waiting time	T_{wait}	1	—	—	μS	CLK↑→CLK↓


PWSTB
STB
PWCLK
PWCLK
tCLK-STB
CLK
tSETUP
tHOLD
DIN
tPZL
tPZL
DOUT
tTHZ
tTZH
SEGn/GRIDn
90%
10%

13 Package Information

13.1 SOP32（21.00mm × 7.50mm PP=1.27mm）



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	2.34
A1	0.10	0.20	0.25
b	0. 30	-	0. 50
b1	0.27	0.30	0.33
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	20.90	21.00	21.10
E	10.2	10.4	10.6
E1	7.40	7.50	7.60
e	1.27BSC		
θ	0	-	8°
L	0. 70	-	1. 00
L1	1.40REF		

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15 Revision History

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Initial release	YES
2	1.1	2018-10-11	Add reference circuit	YES
3	1.2	2019-03-21	Alignment correction	YES
4	1.3	2025-09-28	Change Description	YES

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