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Vinka Microelectronics

VK1603 Datasheet

Three-channel LED driving control circuit

Rev.1.1

1 General Description

VK1603 is a dedicated circuit for driving and controlling three-channel LEDs. It integrates an MCU digital interface, data latch, LED high-voltage driver, and other circuits. Through external MCU control, this chip can achieve independent brightness control and cascaded control, enabling the control of color dot matrix lighting for outdoor large screens. The product has excellent performance and reliable quality.

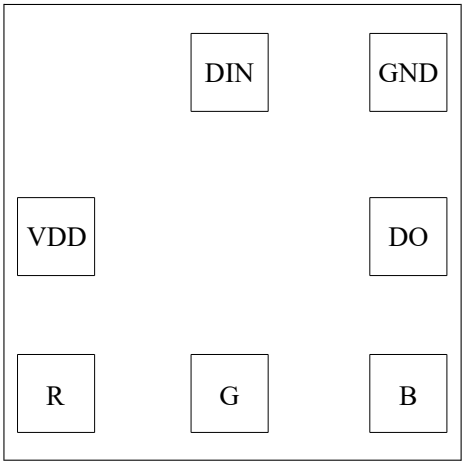
2 Key Features

- Single-line data transmission
- Built-in double RC oscillation, and according to the signal on the data line clock synchronization, after receiving the data of the unit can be automatically
- Subsequent data for plastic forward
- Linear transmission, unlimited cascade
- Any two points transmission distance of more than 10 meters without increasing any circuit
- Data transmission frequency: 800K per second. When the picture refresh rate reaches 30 frames per second, it shall be no less than 1024 points.
- PWM control terminal can achieve a level 256, sweep frequency not less than 3 KHZ
- Output port withstands a voltage of 10.5V.
- After power on the absence of signal input out the lamp
- Available Packages:
  SOP8(150mil)(4.9mm x 3.9mm PP=1.27mm)
  TSOT23-8L

3 Application field

- Carousel lights, ambient lights, sound effect lights, party lighting
- Desktop creative lights, etc.

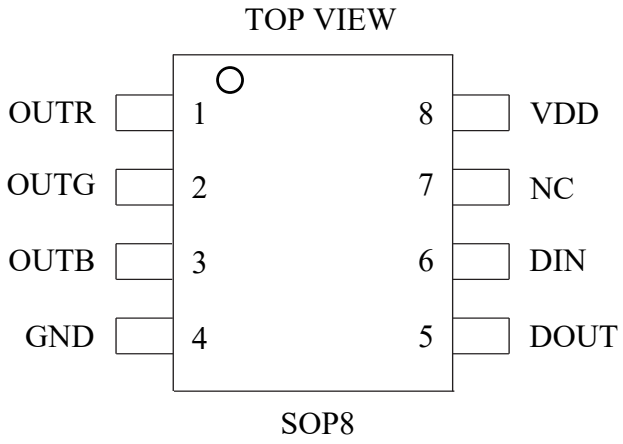
4 Chip pin and coordinates



Chip area：360×360 um^2 Substrate potential：GND
PAD size：60×60 um Minimum spacing：47.5 um Aluminum pad thickness：3um

PAD NAME	PAD SIZE(um^2)	X(Center)um	Y(Center)um
DIN	60*60	150	257.5
GND	60*60	257.5	257.5
DO	60*60	257.5	150
B	60*60	257.5	42.5
G	60*60	150	42.5
R	60*60	42.5	42.5
VDD	60*60	42.5	150

5 Package Pinout Information(SOP8)



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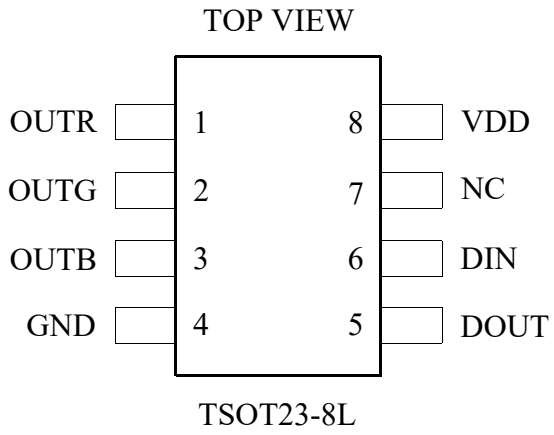
5.1 VK1603/SOP8 Pin Description

No.	Name	I/O	Function Description
1	OUTR	O	Red PWM Control output
2	OUTG	O	Green PWM Control output
3	OUTB	O	Blue PWM Control output
4	GND	GND	Negative power supply
5	DOUT	O	Display data cascading output (800K)
6	DIN	I	Display data input (800K)
7	NC	-	NC
8	VDD	VDD	Positive power supply

6 Package Pinout Information(TSOT23-8L)



TSOT23-8L

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6.1 VK1603/TSOT23-8L Pin Description

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7 Maximum rating

(Unless otherwise specified，TA＝ 25℃，VSS＝ 0V)

Parameters	Symbol	Range	Unit
Logic power supply voltage	V_{DD}	3.0 ～＋6.0	V
Output port withstand voltage	V_{OUT}	9.5	V
Logic input voltage	V_I1	－ 0.5 ～ V_{DD} ＋ 0.5	V
Operating temperature	T_{opt}	－ 30～ ＋ 85	℃
Storage temperature	T_{stg}	－ 55 ～ ＋ 150	℃

7.1 Recommended scope of work

(Unless otherwise specified，TA ＝－20 ～ ＋ 70℃，VSS ＝ 0V)

Parameters	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Logic power supply voltage	V_{DD}	-	5	-	V	-
High-level input voltage	V_{IH}	0.7 V_{DD}	-	V_{DD}	V	-
Low-level input voltage	V_{IL}	0	-	0.2 V_{DD}	V	
Output port withstand voltage	V_{OUT}		9.5		V	

7.2 Electrical parameters

(Unless otherwise specified，TA ＝－20～＋70℃，VDD ＝ 4.5～5.5V，VSS ＝ 0V)

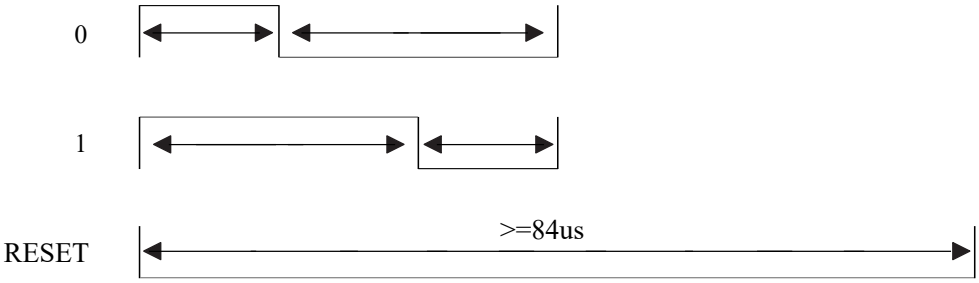
Parameters	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Dout Current injection capability	I_{doutl}	-	30	-	mA	VDD=5V,VO=5V,DOUT
Dout Current carrying capacity	I_{douth}	-	30	-	mA	VDD=5V,VO=0V,DOUT
RGB Output current	i_o	-	12	-	mA	VDD=5V,VO=1.5V
High-level input voltage	V_{IH}	0.7 VDD	-	-	V	DIN
Low-level input voltage	V_{IL}	-	-	0.2 VDD	V	DIN

8 Function Description

Using single chip communication way, with the method of zero code signal. After power-on reset, the chip receives data sent from the DIN terminal. Once it receives 24 bits of data, the DO port starts to forward the data, providing input data for the next chip. Before forwarding, the DO port remains pulled low. At this time, the chip will not accept new data. The OUTR, OUTG, and OUTB three PWM output ports of the chip will emit signals with different duty ratios according to the received 24-bit data. The signal period is 0.3 ms. If the input signal from the DIN terminal is the RESET signal, the chip will send the received data for display. The chip will reaccept new data after this signal ends. After receiving the first 24 bits of data, it will forward the data through the DO port. Before receiving the RESET code, the OUTR, OUTG, and OUTB pins of the chip maintain their original output. When receiving a RESET code of more than 80 μs, the chip will output the 24-bit PWM data pulse width to the OUTR, OUTG, and OUTB pins.

8.1 Timing waveform diagram

1）Input code pattern

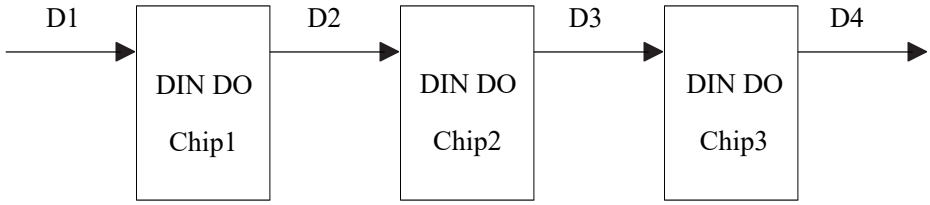


2）Encoding time

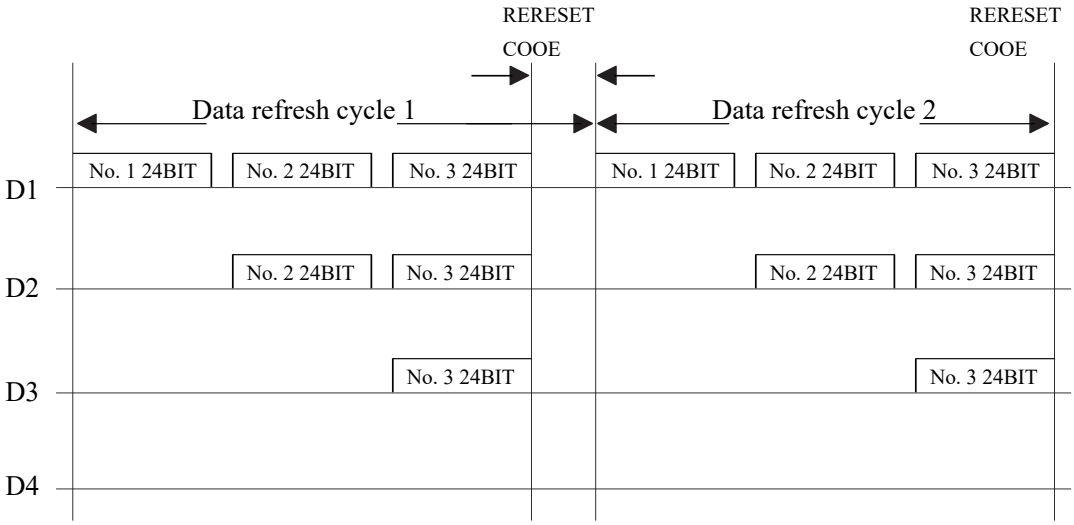
Name	Description	Typical value	Allowable error
T0H	0 code, high level time	0.3μs	±50ns
T1H	1 code, high-level time	0.6μs	±50 ns
T0L	0 code, low-level time	0.6μs	±50 ns
T1L	1 code, low-level time	0.3μs	±50 ns
Tres	Reset code, low level duration	>=84us	

Note: The allowable error refers to the error in the same direction.

3）Connection method



4）Data transmission method



Note: D1 represents the data sent by the MCU end, while D2, D3, and D4 are the data automatically reshaped and forwarded by the cascaded circuit.

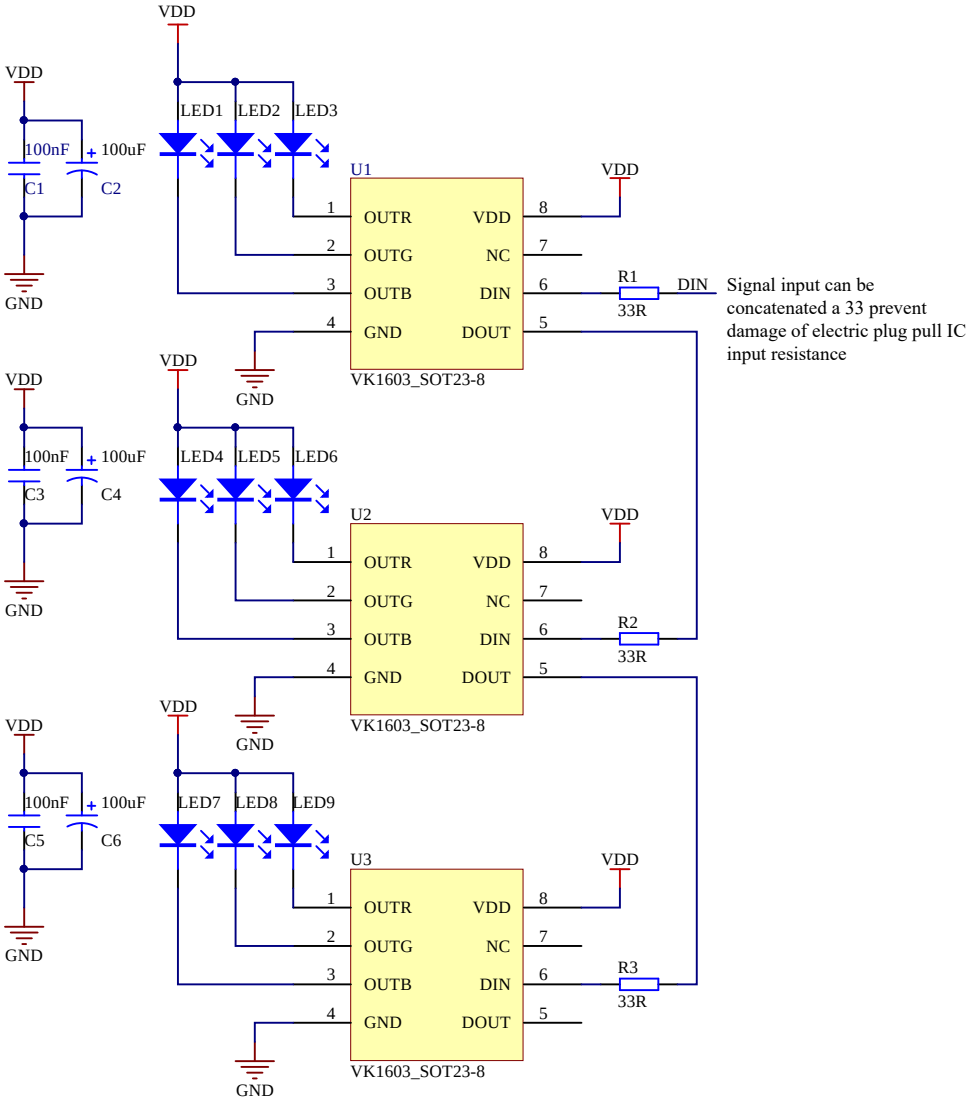
5）24-bit data structure

R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

Note: High position takes the lead and sends data in the order of RGB.

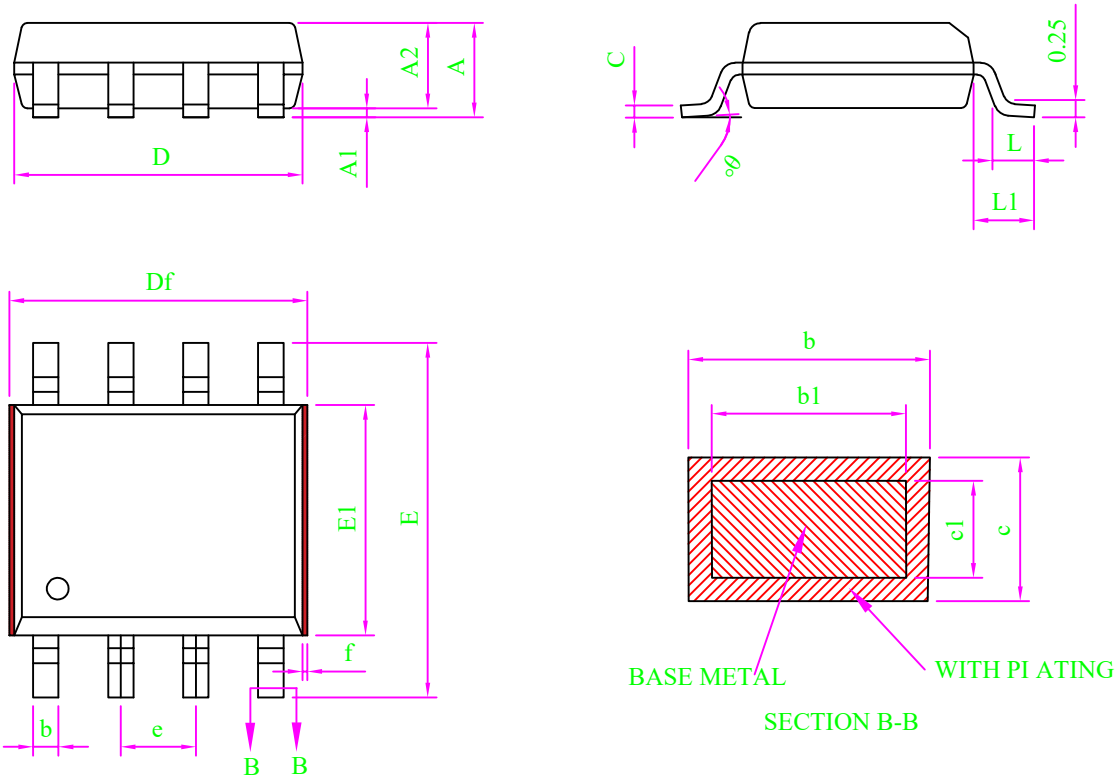
9 Application Circuits

VDD, filter capacitance between GND in PCB wiring should be placed close to the chip, the strengthening effect.



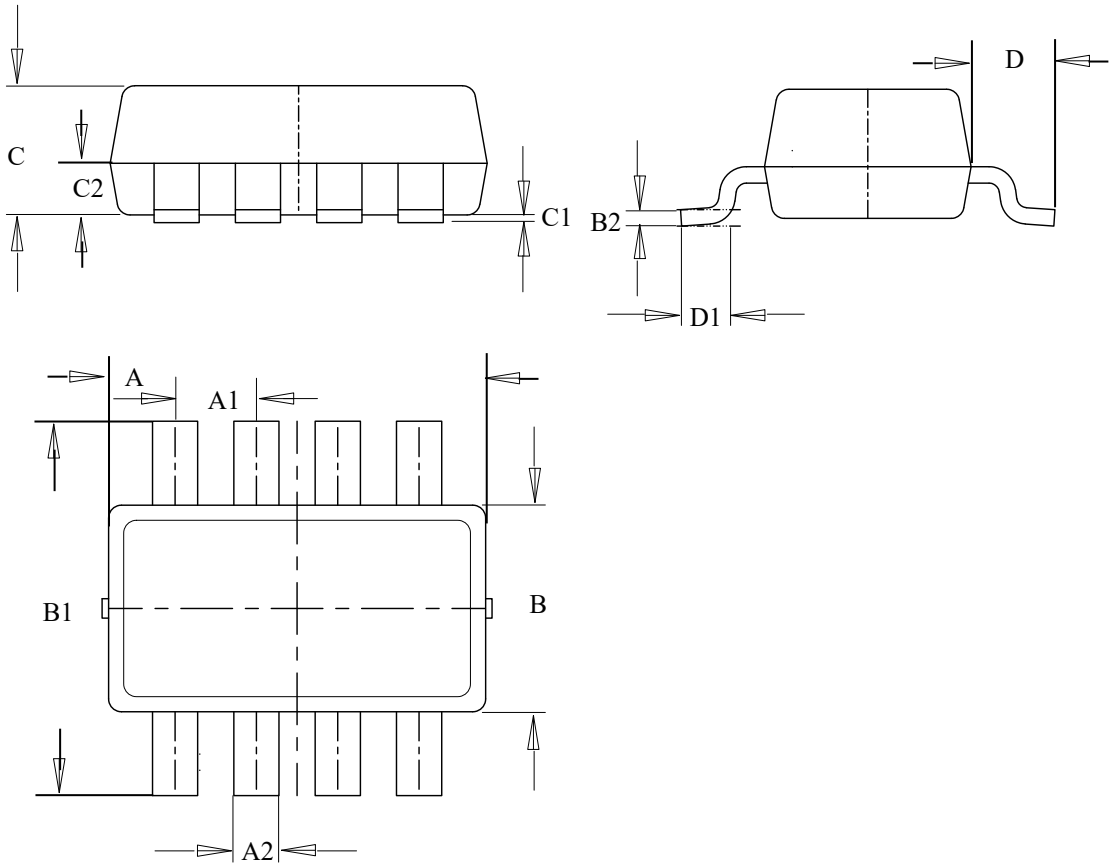
10 Package Information

10.1 SOP8(150mil)(4.9mm x 3.9mm PP=1.27mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	0.15	0.20
A2	1.35	1.45	1.55
b	0.39	-	0.47
b1	0.38	0.41	0.43
c	0.20	-	0.25
c1	0.19	0.20	0.21
D	4.78	4.88	4.98
Df	4.93	-	5.33
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.51	0.66	0.81
L1	0.95	1.05	1.15
θ	0	-	8°
f	0.05	-	0.20

10.2 TSOT23-8L



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.87	2.92	2.97
A1	0.58	0.63	0.68
A2	0.30	0.35	0.40
B	1.55	1.60	1.65
B1	2.75	2.90	3.05
B2	0.127BSC		
C	0.95	1.00	1.05
C1	0.00	0.06	0.12
C2	0.37	0.40	0.43
D	0.57	0.65	0.73
D1	0.30	0.40	0.50

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12 Revision History

No.	Version	Date	Modify the content	Check
1	1.0	2020-08-10	Original version	YES
2	1.1	2025-11-04	Update version	YES

[1] Consult the recently published documents before starting or finishing the design.

[2] Since the release of this document , the device product status described in this document may have changed and may differ in several cases. The latest product status information can be found on the Internet at https://www.szvinka.com/