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Vinka Microelectronics

VK73XX-1 Datasheet

300mA Low Dropout LDO

Rev.1.1

1 General Description

VK73XX-1 is a low-dropout linear regulator that adopts CMOS technology. The maximum output current is 300mA and the maximum allowable input withstand voltage is +48V. It has several fixed output voltages, ranging from +1.8V to +5.0V. COMS technology can ensure that it has the characteristics of low voltage drop and low quiescent current.

2 Key Features

- Low power consumption
- Low dropout voltage
- Lower temperature coefficient
- Maximum input withstand voltage: +48V
- Typical static current: 3uA
- Maximum output current: 300mA
- Output voltage accuracy: ±2%
- Available Packages:
  SOT23-3, SOT89

3 Application Field

- Battery-powered equipment
- Communication equipment
- Audio/video equipment

4 Product Selection

Part No.	Output voltage	Packaging	Official seal
VK7318-1	1.8V	SOT23-3 SOT89	VK73XX-1
VK7325-1	2.5V		
VK7330-1	3.0V		
VK7333-1	3.3V		
VK7336-1	3.6V		
VK7344-1	4.4V		
VK7350-1	5.0V		

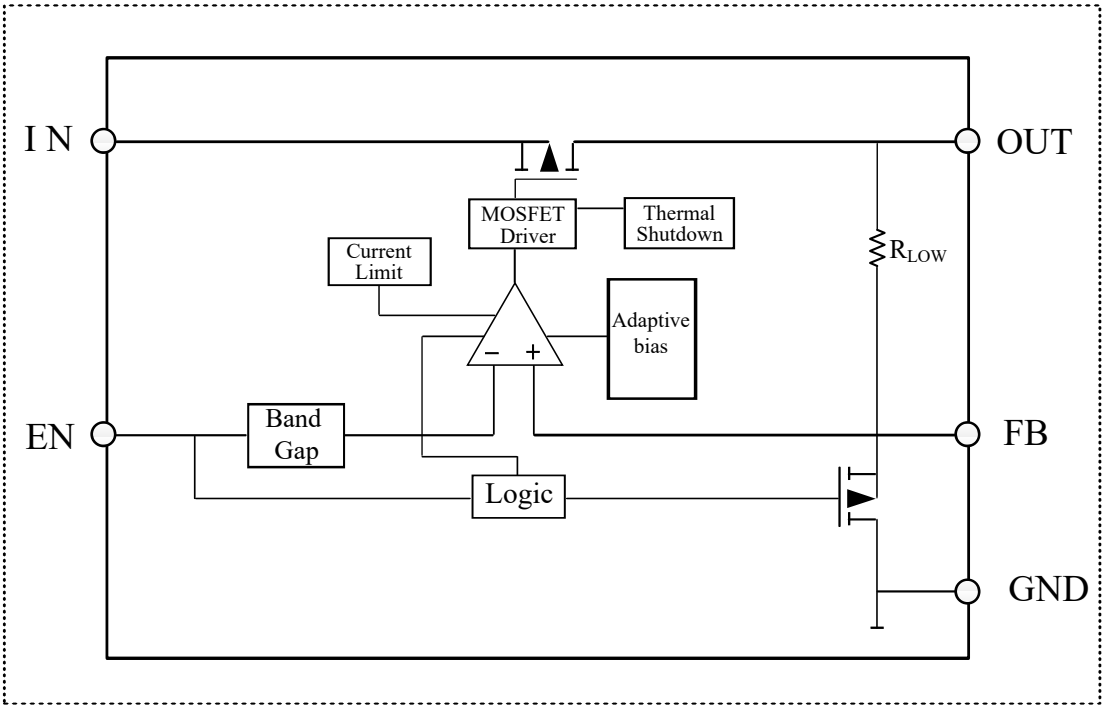
Note: "xx" represents the output voltage.

5 Ordering Information

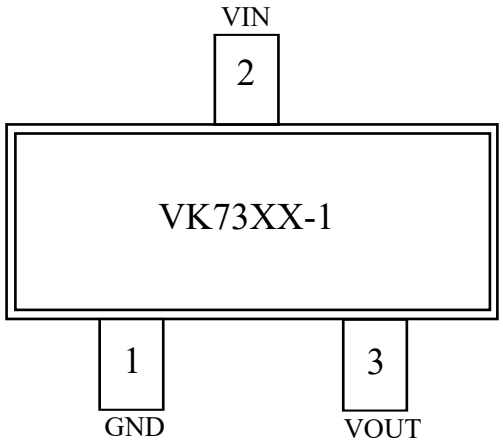
Part No.	Packaging	Tube Qty	Tray(reel)Qty	Box Qty	Total Qty	Notes
VK7318-1	SOT23-3	—	3000/reel	9000/box	108000 PCS	
	SOT89	—	1000/reel	3000/box	36000 PCS	
VK7325-1	SOT23-3	—	3000/reel	9000/box	108000 PCS	
	SOT89	—	1000/reel	3000/box	36000 PCS	
VK7330-1	SOT23-3	—	3000/reel	9000/box	108000 PCS	
	SOT89	—	1000/reel	3000/box	36000 PCS	
VK7333-1	SOT23-3	—	3000/reel	9000/box	108000 PCS	
	SOT89	—	1000/reel	3000/box	36000 PCS	
VK7336-1	SOT23-3	—	3000/reel	9000/box	108000 PCS	
	SOT89	—	1000/reel	3000/box	36000 PCS	
VK7344-1	SOT23-3	—	3000/reel	9000/box	108000 PCS	
	SOT89	—	1000/reel	3000/box	36000 PCS	
VK7350-1	SOT23-3	—	3000/reel	9000/box	108000 PCS	
	SOT89	—	1000/reel	3000/box	36000 PCS	

6 Functional Description

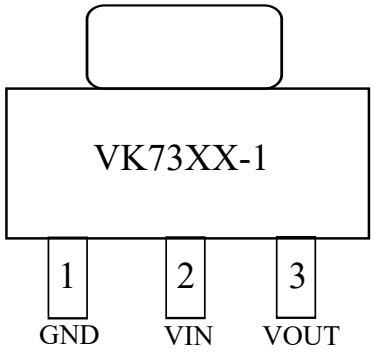
6.1 Block Diagram



7 Package Pinout Information(SOT23-3 / SOT-89)



SOT23-3



SOT-89

For more information: 15-16 page

7.1 VK73XX-1/SOT23-3/SOT-89 Pin Description

No.	Name	Function
1	GND	Negative power supply
2	VIN	Power input pin
3	VOUT	The output pin must be connected to ground with a capacitor of 1uF or more

8 Limit Parameters

Symbol	Parameter	Test Conditions	Unit
Vin	Input voltage	0~+45(Note1)	V
Vout	Output voltage	1.8~5.0	V
T_{STG}	Storage temperature	-45~+140	℃
T_{WK}	Working temperature	-40~+85	℃
ESD_{HBM}	Human body model	4000(Note2)	V
CDM	Charged device mode	1500(Note2)	V
Latch up	The maximum current value of the latch	200(Note2)	mA

Here, only the rated power is emphasized. Exceeding the range specified by the limit parameters will cause damage to the chip. It is impossible to predict the working state of the chip outside the above-mentioned marked range. Moreover, if it operates for a long time under conditions outside the marked range, it may affect the reliability of the chip.

Note 1: Refer to the electrical characteristics and application information.

Note 2: The ESD protection of this series of products is tested through the following methods:

Test the ESD human body mode in accordance with EIA/JESD22-A114.

Test the electrostatic discharge capability according to JESD22-C101.

Test the maximum current value of the latch according to JEDEC78.

8.1 Suggested Working Conditions

Symbol	Parameter	Test Conditions	Unit
V_{IN}	Input voltage	+2.5~+45(Note1)	V
I_{OUT}	Output current	0~300	mA
T_A	Working temperature	-40~+85	℃
C_{IN}	There is a polar capacitor at the input terminal	1~10	uF
C_{OUT}	There is a polar capacitor at the output terminal	1~10	uF
ESR	The equivalent resistance values of the input and output terminal capacitors	5~100	mΩ

Note 1:

*When choosing the input voltage and output current, be sure that the power consumption does not exceed the PD value.

8.2 Thermal Information

Symbol	Parameter	Packaging	Max.	Unit
θ_{JA}	Thermal resistance (connection with the environment) (assuming no environmental airflow and no heat sink)	SOT23-3	360	℃/W
		SOT89	135	℃/W
P_D	Power consumption	SOT23-3	0.2	W
		SOT89	0.5	W

Note: The PD value was measured at Ta=25℃.

8.3 Electrical Characteristics

Ta=25℃

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VIN	Input voltage	—	—	—	+45(Note1)	V
V_{OUT}	Output voltage	TA=+25V℃	−2%		+2%	V
		-40℃ ≤ TA ≤ +-85℃	−3%		+3%	V
V_{DROP} (Note2)	Pressure difference IOUT=300mA	V_{OUT}=1.8V	—	1350	1650	mV
		V_{OUT}=2.5V	—	1150	1450	mV
		V_{OUT}=3.0V	—	1100	1400	mV
		V_{OUT}=3.3V	—	1050	1360	mV
		V_{OUT}=3.6V	—	1000	1300	mV
		V_{OUT}=4.4V	—	950	1250	mV
		V_{OUT}=5V	—	900	1200	mV
I_{OUT}	Output current	V_{IN}=V_{OUT}+2V	—	300	—	mA
$Load_{Reg}$	Load regulation rate	1mA≤I_{OUT}≤300mA V_{IN} =V out+1V	—	—	40	mV
I_LMT	Limiting current	V_{IN}=V_{OUT}+1V	300	450	—	mA
I_{SHORT}	Short-circuit limiting current	V_{OUT} =0V	—	100	—	mA
I_Q	Static current	No load(I_{OUT}=0mA)	—	3	4.0	uA
PSRR	Power supply rejection ratio	V_{IN}=V_{OUT}+1V, I_{OUT}=20mA f=1KHz	—	60	—	dB
eN	Output noise voltage	V_{IN}=V_{OUT}+1V, I_{OUT}=1mA f=10Hz~100KHz (V_{OUT}=3V) C_{OUT}=1uF	—	100	—	uVrms
R_{LOW}	Output discharge resistance	C_{IN}=24V， Ven=0V	—	70	—	Ω
$\frac{\Delta VOUT}{\Delta VIN \times VOUT}$	Input voltage regulation rate	Vo+1V≤V_{IN}≤45V I_{OUT} =1mA	—	—	0.2	%/V
$\frac{\Delta VOUT}{\Delta Ta \times VOUT}$	Temperature coefficient	I_{OUT} =10mA -40℃<Ta<85℃	—	100	—	ppm/℃

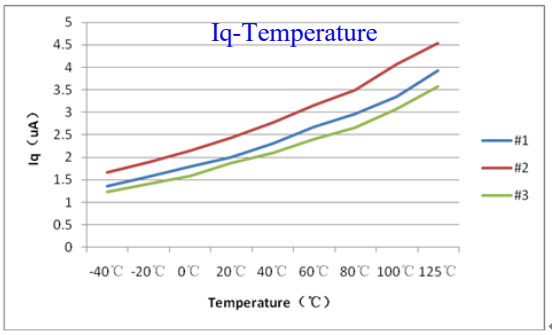
Note 1: Avoid the internal power consumption (PD) of the IC exceeding the maximum power consumption value allowed by the package.

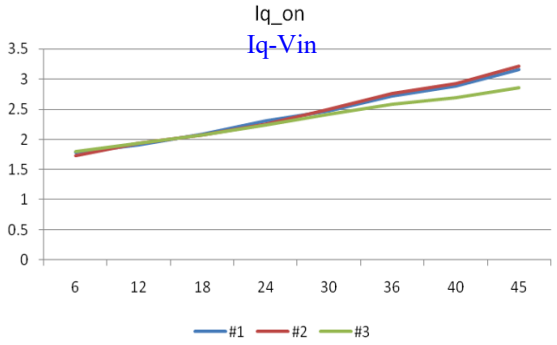
The calculation method of PD: PD=(VIN-VOUT)×IOUT

For example, in the SOT89 package, when VIN=12V and IOUT=100mA, PD= (12-5) ×100mA=0.7W. Exceeding the specification of 0.5W May damage the IC. For PD values of different packages, please refer to the "Thermal Energy Information" column.

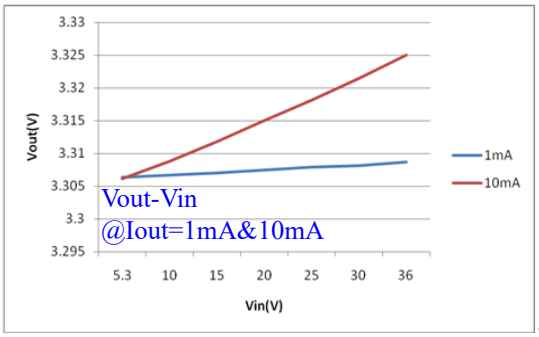
Note 2: Under the condition of VIN=VOUT+2V and a fixed load, the output voltage is reduced by 2%. At this time, the input voltage minus the output voltage is the Dropout voltage.

9 Typical Performance Characteristics

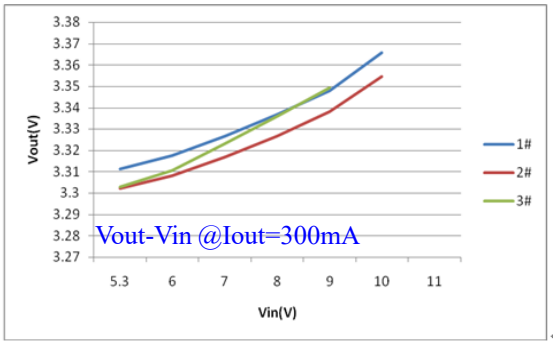




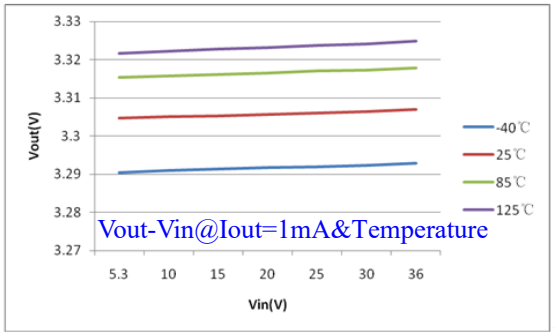
DC Supply Quiescent Current



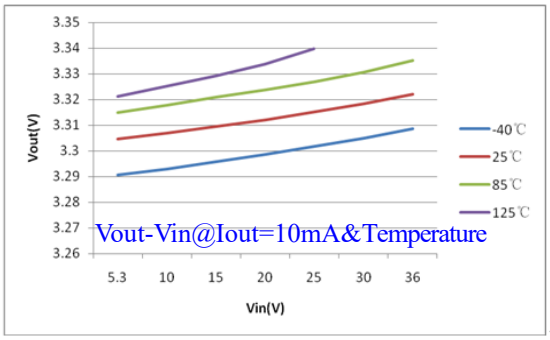
Line Regulation



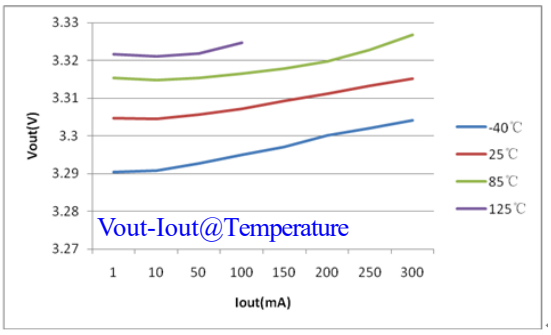
Iout=300mA Line Regulation



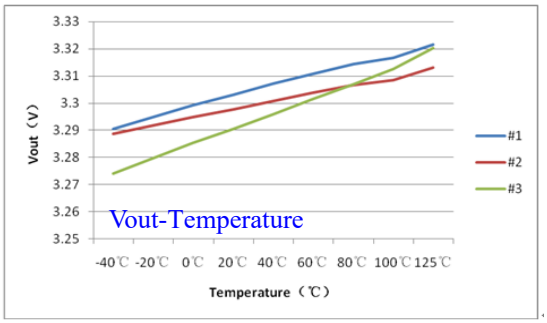
Line Regulation Iout=1mA



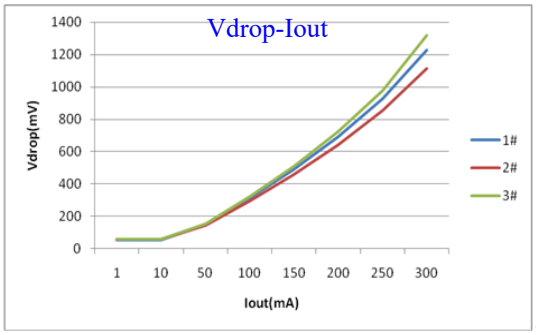
Line Regulation Iout=10mA

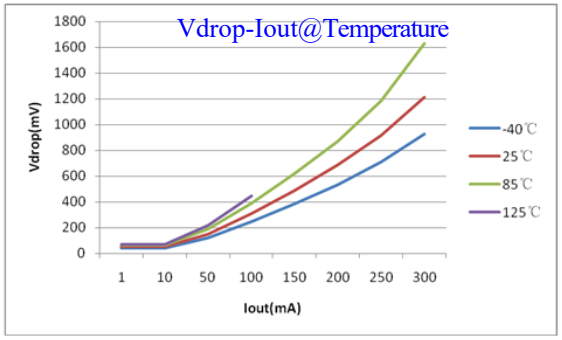


Load Regulation

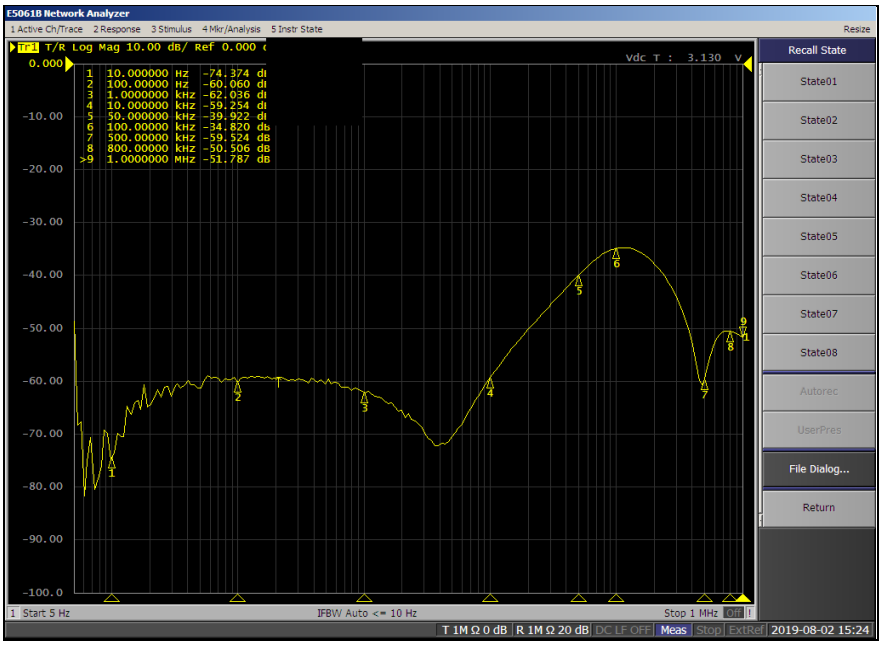


Output Voltage

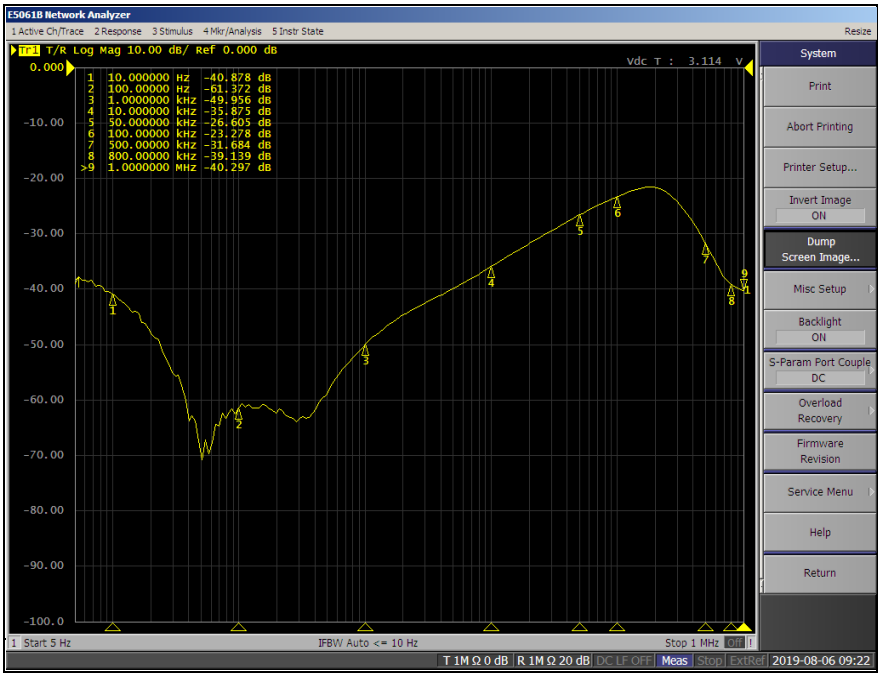




9.1 PSSR

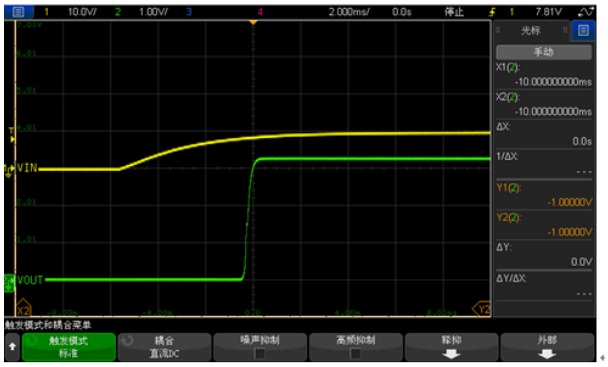


PSRR @Iout=20mA

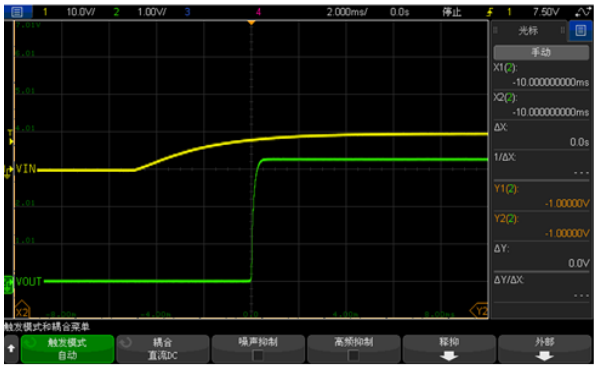


PSRR @Iout=300mA

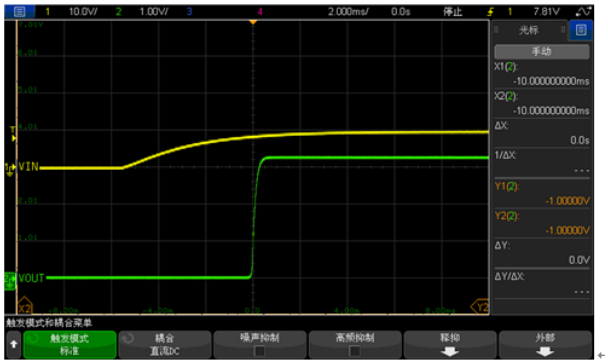
9.2 Startup Characteristics



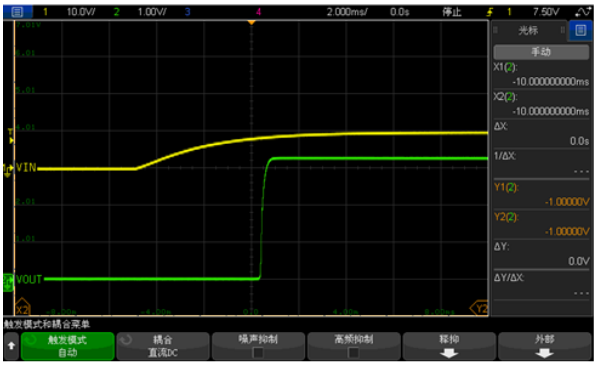
Vin=10V, Iout=0mA,Cout=0.1uF



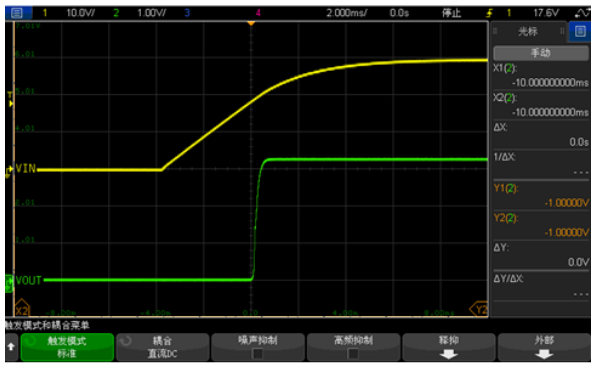
Vin=10V, Iout=0mA,Cout=10uF



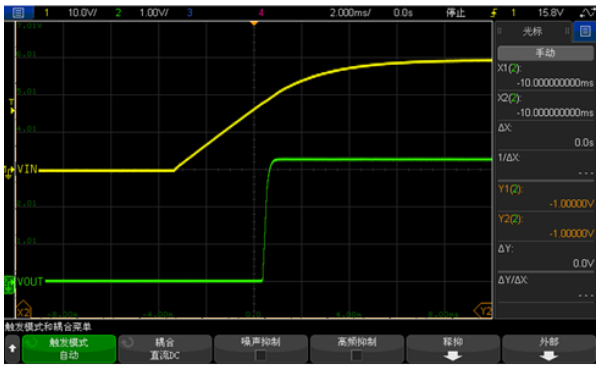
Vin=10V, Iout=30mA,Cout=0.1uF



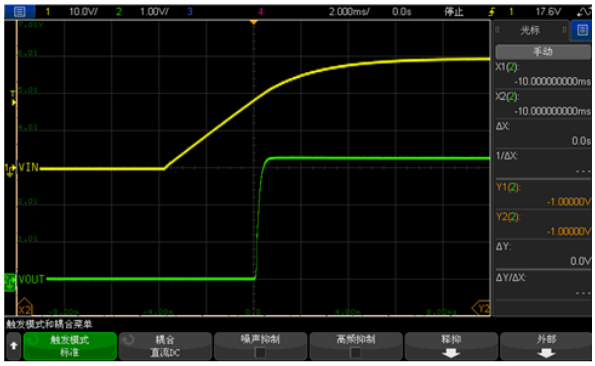
Vin=10V, Iout=30mA,Cout=10uF



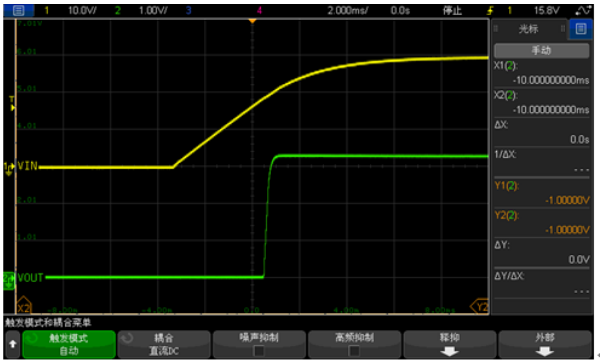
Vin=30V, Iout=0mA,Cout=0.1uF



Vin=30V, Iout=0mA,Cout=10uF



Vin=30V, Iout=30mA,Cout=0.1uF



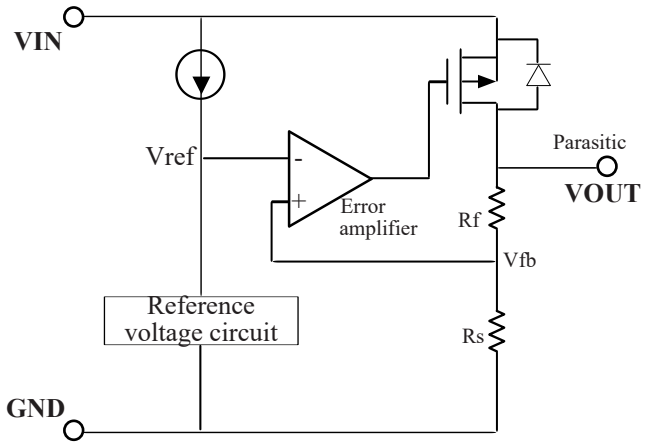
Vin=30V, Iout=30mA,Cout=10uF

10 Pressure Difference

It has a current-limiting function to prevent the equipment from being damaged in case of overload or short circuit. This current is detected by the internal induction transistor.

10.1 Function Description

The error amplifier compares the input voltage Vfb of the voltage divider resistor composed of the feedback resistors Rs and Rf with the reference voltage Vref. The necessary gate voltage is provided to the output transistor through this error amplifier, so that the output voltage remains constant without being affected by the input voltage or temperature changes.



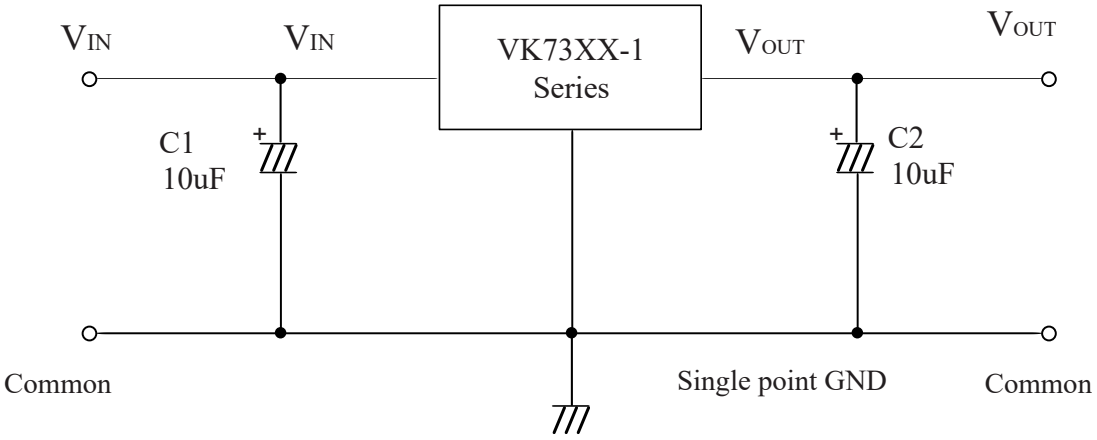
Usage Precautions:

1) The circuit internally employs a phase compensation circuit and uses the ESR of the output capacitor for compensation. Therefore, it is recommended to connect a capacitor larger than 1uF to the output ground.

2) It is recommended that 10uF polarized capacitors be used for input and output during application, and the capacitors be placed as close as possible to the VIN and VOUT pins of the LDO.

3) Pay attention to the usage conditions of input and output voltages and load currents to avoid the internal power consumption (PD) of the IC exceeding the maximum power consumption value allowed by the package.

11 Application Circuits

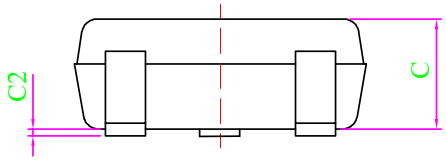


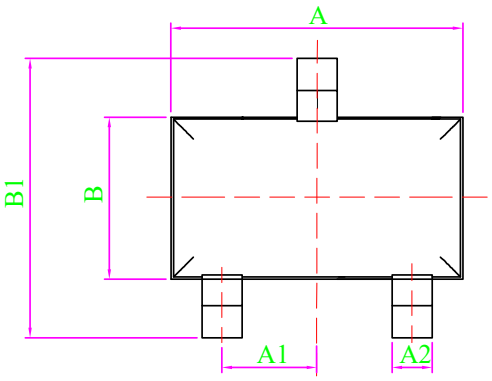
Layout suggestions:

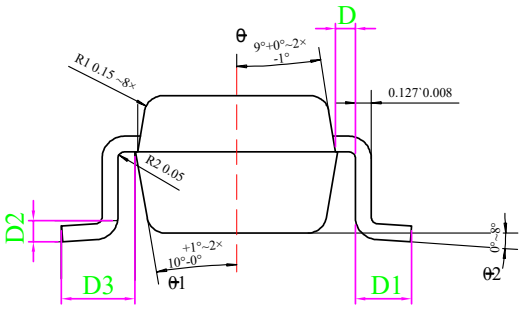
1. The input and output capacitors should be as close to the device as possible.
2. Use copper planes for equipment connection to optimize thermal performance.
3. Simulate thermal through holes around the device to disperse heat.

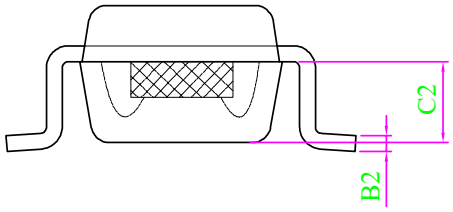
12 Package Information

12.1 SOT23-3 Package size



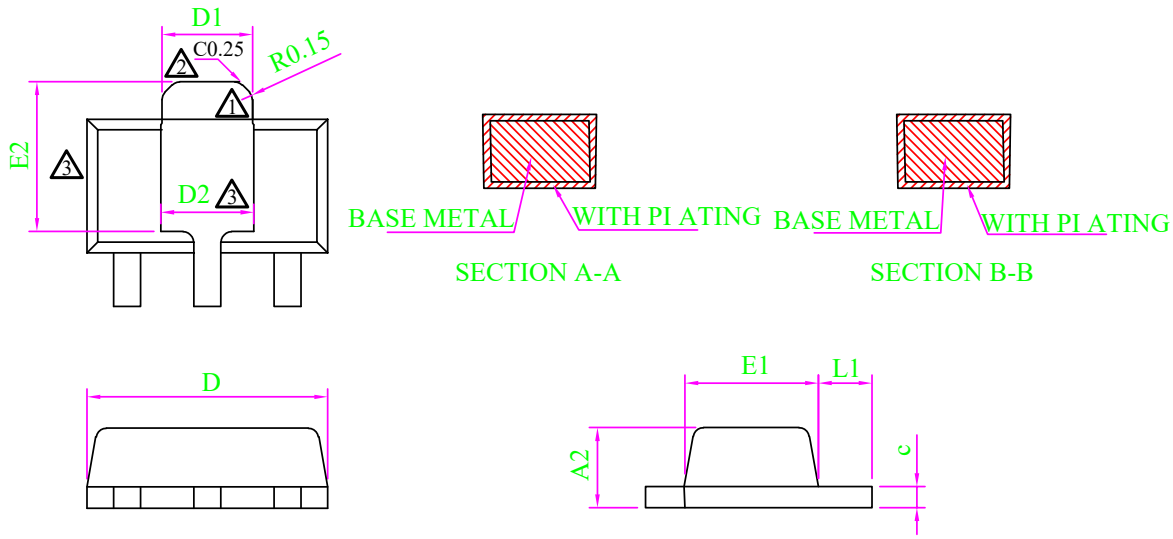






COMMON DIMENSIONS CUNITS MEASURE=MILLIMETER			
SYMBOL	MIN	MID	MAX
A	2.82	2.92	3.02
A1	0.90	0.95	1.00
A3	0.30	0.35	0.40
B	1.52	1.62	1.72
B1	2.80	2.90	3.00
B2	0.12	0.128	0.135
C	1.05	1.10	1.15
C1	0.03	0.08	0.13
C2	0.60	0.65	0.70
D	0.03	0.08	0.13
D1	0.40	0.45	0.50
D2	0.25TYP		
D3	0.60	0.65	0.70

12.2 SOT-89 Package size



	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
	A2	1.40	1.50	1.60
4	b	0.38	-	0.46
	b1	0.37	0.40	0.43
4	c	0.38	-	0.42
4	c1	0.37	0.38	0.39
	a	0.46	-	0.56
	a1	0.45	0.48	0.51
4	D	4.40	4.50	4.60
5	D1	1.62	-	1.83
5	E	3.95	-	4.25
4	E1	2.40	2.50	2.60
	e	1.50BSC		
5	L1	0.89	-	1.20

L/F Size (mil) \ Size(mm)	5 D2	3 E2
66.9*63	1.75REF	2.84REF

13 Disclaimer

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14 Revision History

No.	Version	Date	Modify the content	Check
1	1.0	2020-08-10	initial release	YES
2	1.1	2025-11-07	Change Description	YES

[1] Please refer to the latest version of this document before starting or finalizing any design.

[2] Since the release of this document, the status or availability of this product may have changed. For the most up-to-date information, please visit: https://www.szvinka.com/