VKS232 Datasheet

116×1/116×2 LCD DRIVER

Rev.1.3

1 General Description

VKS232 is a dot-matrix storage mapping dual-mode LCD driver that can support LCD screens with a maximum of 116 static scanning points (116SEG×1COM) as well as 232 dynamic scanning points (116SEG×2COM). The single-chip microcomputer can be configured to display parameters and read and write display data through a 3/4-wire serial interface, and can also enter power-saving mode through instructions. It has the characteristics of good contrast, wide viewing Angle and no flicker. It is suitable for products that require high display quality, such as washing machine panels, automotive instruments, and household appliances.

2 Key Features

- Operating voltage：2.4-5.2V
- Built-in RC oscillator (default)
- Two modes are available (selected through the DS pin)：
  Mode 0 - Drive display points 116×2, dynamic display, 1/2 bias 50% duty cycle (DS pin grounded)
  Mode 1 - Drive display points 116×1, static display, 100% duty cycle without bias (DS pin connected to a pull-up resistor to VDD)
- Built-in 58×4-bit display RAM，Two RAM mapping modes, corresponding to Mode 0 and Mode 1 respectively
- Power-saving mode (accessed by turning off the display and the oscillator)
- 4-wire serial interface
- Software-configurable LCD parameters
- There are two command formats: writing commands and reading and writing data
- Auto-increment addressing for sequential read/write
- The VLCD pin provides the LCD drive voltage source (≤VDD).
- Three access methods for displaying data
- Available Packages:
  LQFP128(14.0mm × 14.0mm PP=0.4mm)

3 Product Selection

Part No.	SEG/COM	Bias	Duty	Packaging
VKS114	58×1/57×2/56×3/55×4	1/1, 1/2,1/3 1/4	1/1, 1/2,1/3 1/4	LQFP64
VKS118	118×1	1/1	1/1	LQFP128
VKS146	74×1/73×2/72×3/71×4	1/1, 1/2,1/3 1/4	1/1, 1/2,1/3 1/4	LQFP80
VKS232	116×1/116×2	1/1，1/2	1/1，1/2	LQFP128

4 Ordering Information

Part No.	Packaging	Tube Qty	Tray(reel)Qty	Box Qty	Total Qty	Notes
VKS114	LQFP64	-	250/tray	2500/box	15000 PCS	
VKS118	LQFP128	-	90/tray	900/box	5400 PCS	
VKS146	LQFP80	-	90/tray	900/box	54000 PCS	
VKS232	LQFP128	-	90/tray	900/box	5400 PCS	

5 Package Pinout Information(LQFP128)

Top pins (left to right): /RD, /CS, /WR, DATA, TEST, DS, GND, VDD, VLCD, VB, COM1, COM0, SEG115, SEG114, SEG113, SEG112, SEG111, SEG110, SEG109, SEG108, SEG107, SEG106, SEG105, SEG104, SEG103, SEG102, SEG101, SEG100, SEG99, SEG98, SEG97, SEG96

Top pin numbers: 128 127 126 125 124 123 122 121 120 119 118 117 116 115 114 113 112 111 110 109 108 107 106 105 104 103 102 101 100 99 98 97

Left side:
SEG0 — 1
SEG1 — 2
SEG2 — 3
SEG3 — 4
SEG4 — 5
SEG5 — 6
SEG6 — 7
SEG7 — 8
SEG8 — 9
SEG9 — 10
SEG10 — 11
SEG11 — 12
SEG12 — 13
SEG13 — 14
SEG14 — 15
SEG15 — 16
SEG16 — 17
SEG17 — 18
SEG18 — 19
SEG19 — 20
SEG20 — 21
SEG21 — 22
SEG22 — 23
SEG23 — 24
SEG24 — 25
SEG25 — 26
SEG26 — 27
SEG27 — 28
SEG28 — 29
SEG29 — 30
SEG30 — 31
SEG31 — 32

VKS232

LQFP128

Right side:
96 — SEG95
95 — SEG94
94 — SEG93
93 — SEG92
92 — SEG91
91 — SEG90
90 — SEG89
89 — SEG88
88 — SEG87
87 — SEG86
86 — SEG85
85 — SEG84
84 — SEG83
83 — SEG82
82 — SEG81
81 — SEG80
80 — SEG79
79 — SEG78
78 — SEG77
77 — SEG76
76 — SEG75
75 — SEG74
74 — SEG73
73 — SEG72
72 — SEG71
71 — SEG70
70 — SEG69
69 — SEG68
68 — SEG67
67 — SEG66
66 — SEG65
65 — SEG64

Bottom pin numbers: 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64

Bottom pins: SEG32, SEG33, SEG34, SEG35, SEG36, SEG37, SEG38, SEG39, SEG40, SEG41, SEG42, SEG43, SEG44, SEG45, SEG46, SEG47, SEG48, SEG49, SEG50, SEG51, SEG52, SEG53, SEG54, SEG55, SEG56, SEG57, SEG58, SEG59, SEG60, SEG61, SEG62, SEG63

For more information:

5.1 VKS232/LQFP128 Pin Description

No.	Name	I/O	Function
1-116	SEG0-SEG115	O	LCD SEG drive outputs
117-118	COM0,COM1	O	LCD COM drive outputs
119	VB	O	The 1/2 bias voltage output pin is connected to an external capacitor to ensure the stability of the 1/2 bias voltage.
120	VLCD	I	LCD driver voltage
121	VDD	VDD	Positive power supply
122	GND	GND	Negative power supply
123	DS	I	Mode selection DS= "1" : Mode 1 - Drive display points 116×1, static display, 100% duty cycle without bias DS= "0" : Mode 0 - drive display points 116×2, dynamic display, 1/2 bias 50% duty cycle
124	TEST	I	Keep, NC
125	DATA	I/O	The bidirectional data pin is equipped with a built-in pull-up resistor
126	/WR	I	The write signal is equipped with an internal pull-up resistor, and the rising edge of the signal locks the data to the display RAM.
127	/CS	I	The chip selection signal is equipped with an internal pull-up resistor, which is disabled at high levels and enabled at low levels.
128	/RD	I	Read the signal with an internal pull-up resistor. Read the DATA to the DATA pin along the falling edge of the signal.

6　Functional Description

6.1　Block Diagram
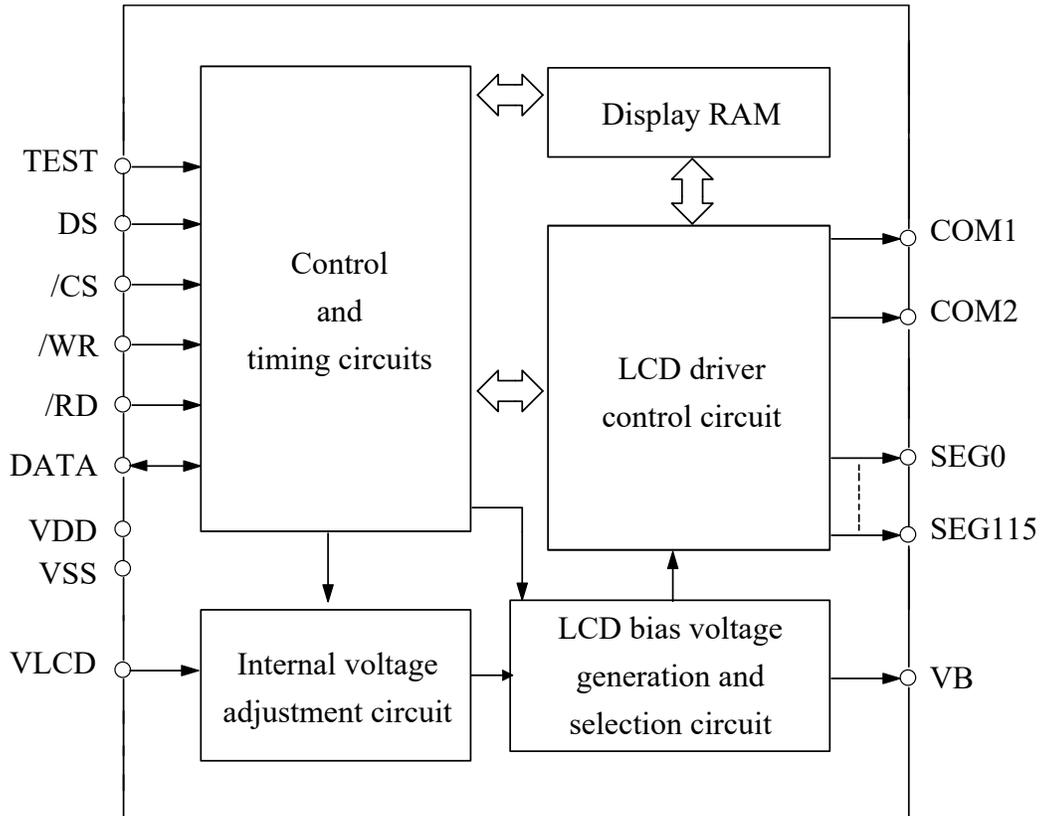
6.2 Display RAM- Storage structure

The static display memory (RAM) has a structure of 58×4 and stores the displayed data. The content of the display RAM is directly mapped to the display content of the LCD driver. Data is stored in RAM through three command forms: read, write, and Read - Modify - write. The mapping relationship between the data in the RAM and the LCD and the working mode of the circuit are related. The working mode is defined by the DS port and is described as follows:

Mode 0: Drive display points 116×2, dynamic display, 1/2 bias, 50% duty cycle (DS pin grounded)

COM1	COM0	COM1	COM0	Address	
SEG0		SEG1		0	
SEG2		SEG3		1	
SEG4		SEG5		2	Address 6
SEG6		SEG7		3	(A5----A0)
⋮		⋮		⋮	
SEG114		SEG115		57	
D3	D2	D1	D0	Data/Addr	

Mode 1: Drive display points 116×1, static display, 100% duty cycle without bias (connect a pull-up resistor to the DS pin to the VDD)

COM0				Address	
SEG0	SEG1	SEG2	SEG3	0	
SEG4	SEG5	SEG6	SEG7	1	
SEG8	SEG9	SEG10	SEG11	2	Address 6
SEG12	SEG13	SEG14	SEG15	3	(A5----A0)
⋮	⋮	⋮	⋮	⋮	
SEG112	SEG113	SEG114	SEG115	28	
D3	D2	D1	D0	Data/Addr	

6.3 LCD Driver

VKS232 is a dot-matrix storage mapping dual-mode LCD driver. The display mode can be selected through the DS pin:

Mode 0 - Drive display points 116×2, dynamic display, 1/2 bias 50% duty cycle (DS pin grounded)
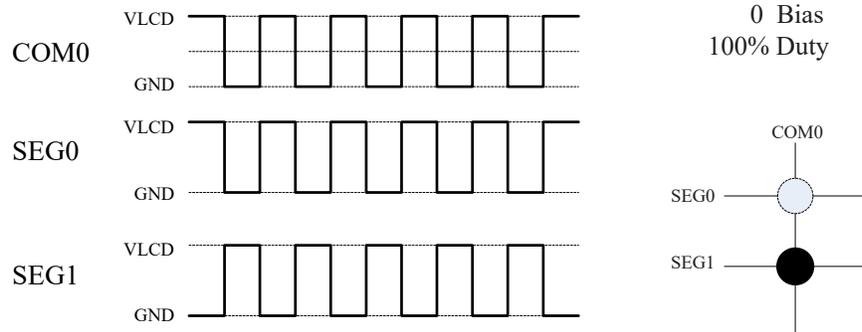
Mode 1 - Drive display points 116×1, static display, 100% duty cycle without bias (DS pin connected to a pull-up resistor to VDD)

LCD driver output waveforms are as follows:

Mode 0-1/2 bias, 50% duty cycle:
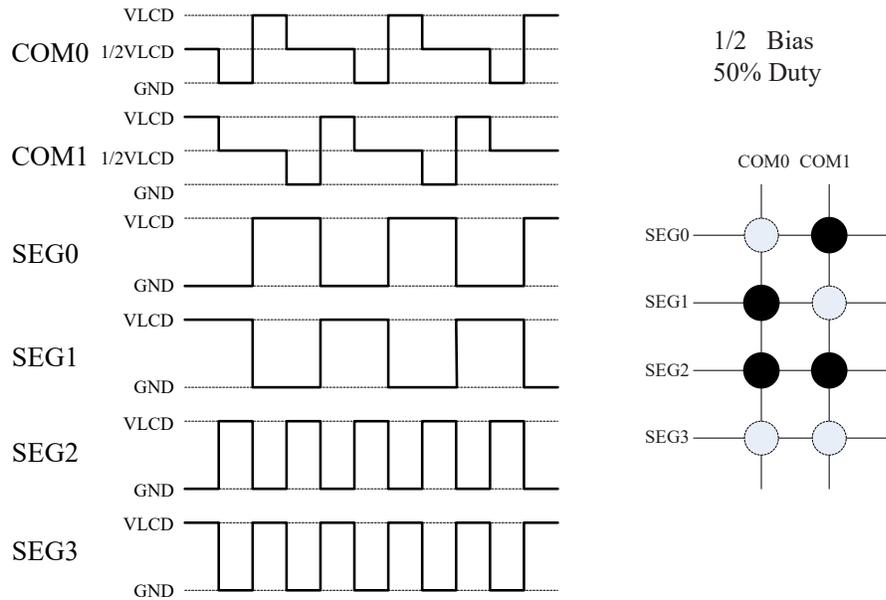
Mode 1-0 bias, 100% duty cycle:

6.4 Communication Interface

The VKS232 has four communication pins.

The /CS pin signal is used to enable/disable communication with the main controller. A high /CS level disables and initializes the internal timing, while a low /CS level enables.

The DATA pin is a serial data input/output pin. Reading/writing data or writing commands must be done through the data pin.

The /RD pin is the READ clock input. DATA from RAM is output to the Data pin at the falling edge of the /RD,and the main controller reads the correct data between the rising edge and the next falling edge of the read signal.

The /WR pin is a clock input pin. The DATA, address or command on the data pin is latched into VKS232 at the rising edge of the /WR.

6.5 Command Format

VKS232 can be operated through software. There are two modes for configuring VKS232 parameters and transmitting LCD display data commands, namely command mode and data mode. The configuration of VKS232 is called command mode, with the ID being 100. The data modes are respectively reading data and writing data. The operation ID for reading data is 110, the operation ID for writing data is 101, and the operation ID for Read-Modify-Write data is also 101.

The ID codes are shown in the table below

Command	MODE	ID
READ	DATA	110
WRITE	DATA	101
Read-Modify-Write	DATA	101
COMMAND	COMMAND	100

7 CMD/Data Timing Diagrams

7.1 READ Mode

Command Code : 110
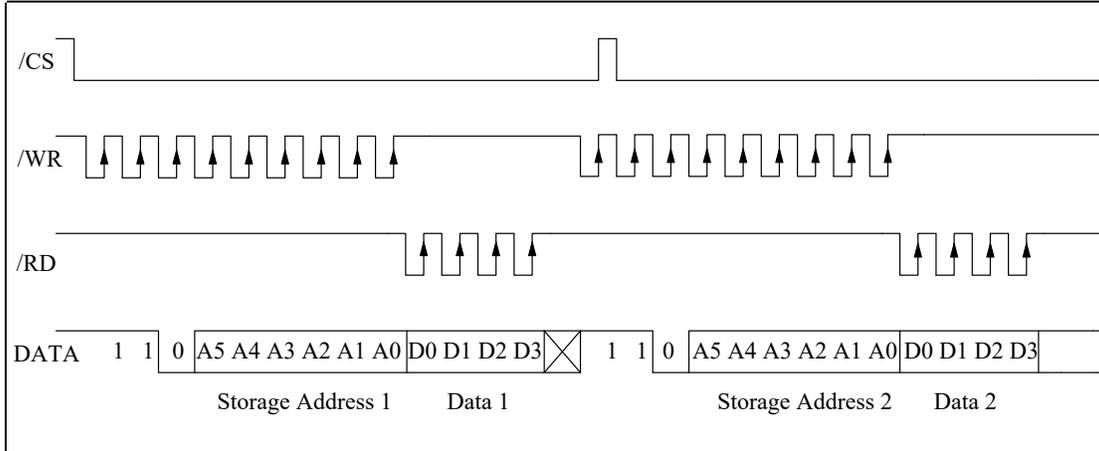
Successive Address Reading

Note: For each 4-bit data read, the address is automatically incremented by 1
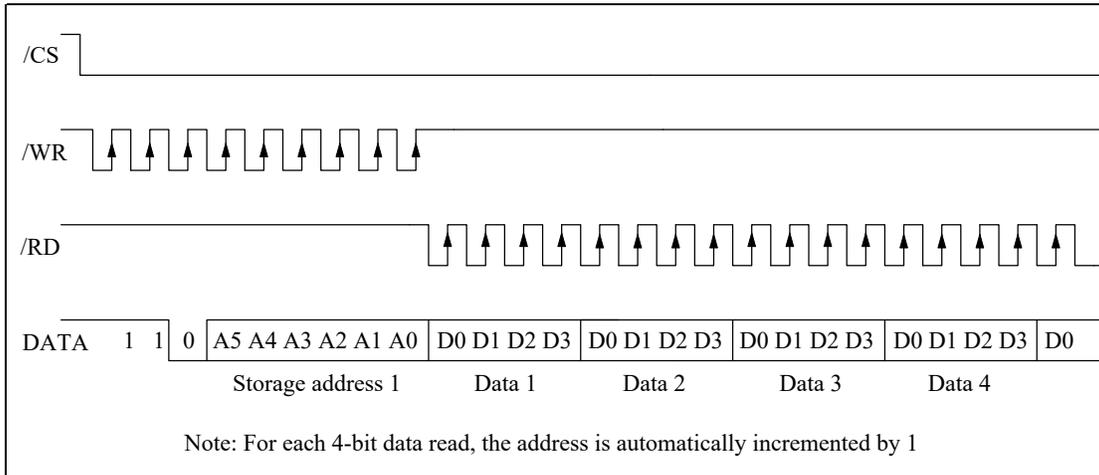
7.2 WRITE Mode
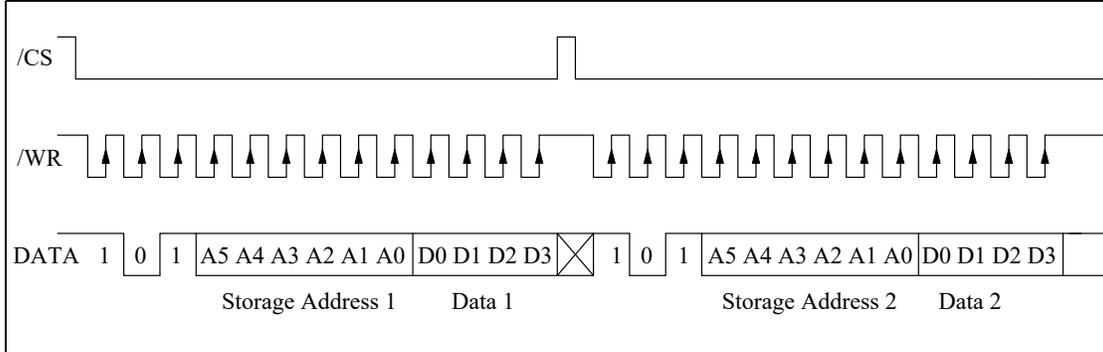
Command Code : 101

Successive Address Writing
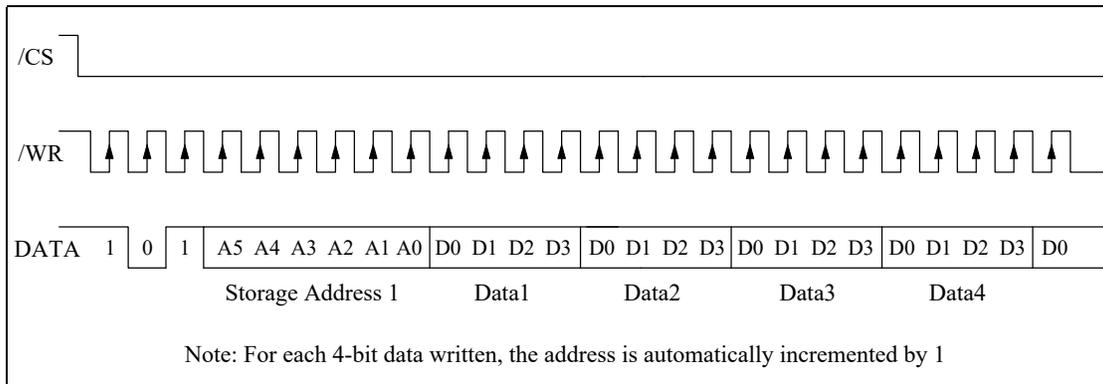
7.3   Read-Modify-Write Mode

Command Code : 101

/CS

/WR

/RD

DATA 1 0 1 | A5 A4 A3 A2 A1 A0 | D0 D1 D2 D3 | D0 D1 D2 D3 | ✕ | 1 0 1 | A5 A4 A3 A2 A1 A0 | D0 D1 D2 D3 |

Storage Address 1   Data 1   Data 1   Storage Address 2   Data 2

Note: After reading 4-bit data, the address remains unchanged. After writing 4-bit data is the same address.
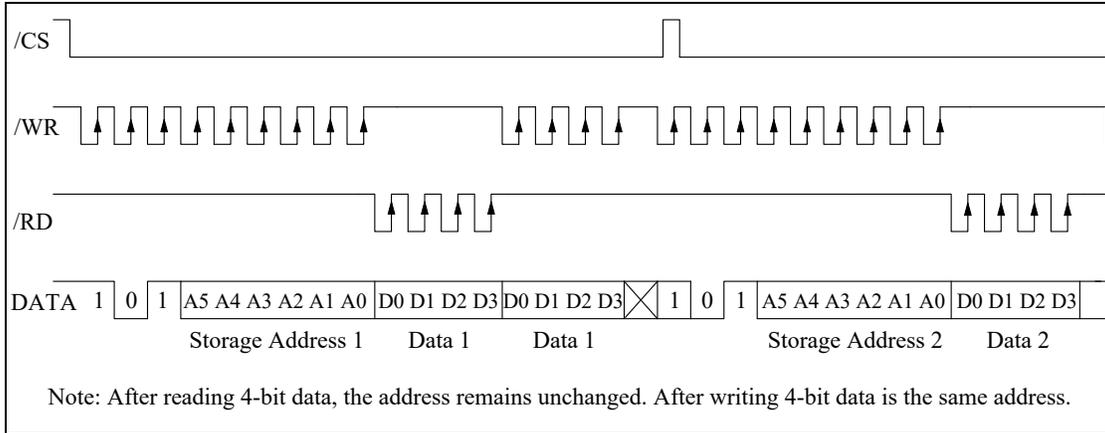
Successive Address Accessing

/CS

/WR

/RD

DATA 1 0 1 | A5 A4 A3 A2 A1 A0 | D0 D1 D2 D3 | D0 D1 D2 D3 | D0 D1 D2 D3 | D0 D1 D2 D3 | D0 D1 D2 D3 | D0 |

Storage Address 1   Data1   Data1   Data2   Data2   Data3

Note: After reading 4-bit data, the address remains unchanged. After writing 4-bit data, the address automatically increase by 1.
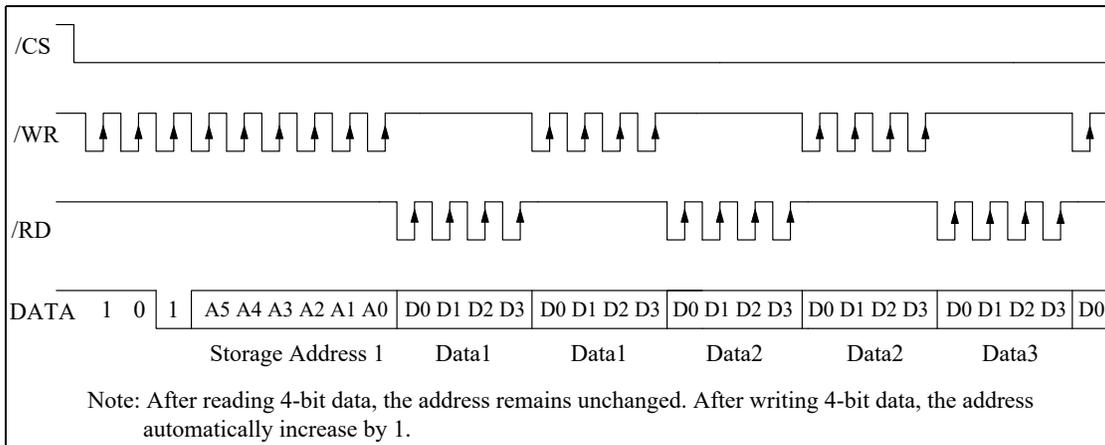
7.4 Command Mode

Command Code : 100
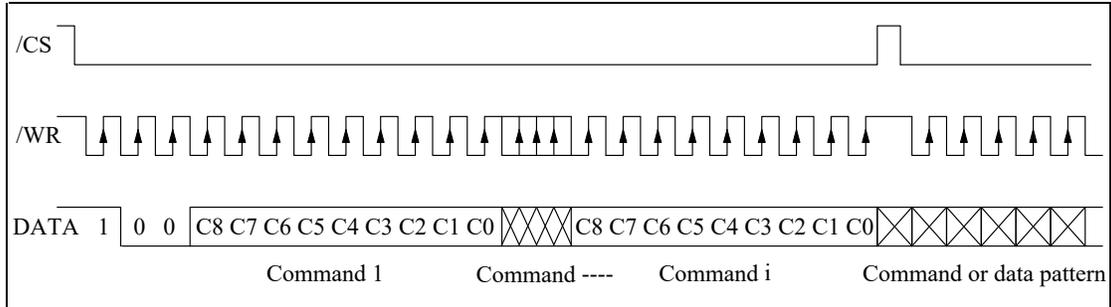
8 Command Summary

Name	ID	Command Code	D/C	Function	Def.
READ	110	A5A4A3A2A1A0D0D1D2D3	D	Read data from RAM	
WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	Write the data into RAM	
READ-MODIFY-WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	Read and write data from RAM	
SYS DIS	100	0000-0000- X	C	Turn off system oscillator	YES
SYS EN	100	0000-0001- X	C	Turn on the system clock	
LCD OFF	100	0000-0010- X	C	Turn off the LCD bias generator	YES
LCD ON	100	0000-0011- X	C	Turn on the LCD bias generator	

Note: X: 0 or 1   D/C: Data/Command Mode

A5-A0: Display the RAM bit address   Reset: Default state upon power-on

D3-D0: 4-bit display data   110,101 and 100 are instruction ids

Vinka Microelectronics

9 Application Circuits

When the power supply for the single-chip microcomputer (3.3V) and the driver chip (5V) is inconsistent, it is recommended to add a level conversion circuit to the communication pin

R6	R5	Display mode
Welding	Not welded	Dynamic 1/2BIAS 2COM
Not welded	Welding	Static COM0 = COM1

When VDD=5V and VR=7.6K:
The VLCD is approximately 4.2V
It is recommended to use a 20K adjustable resistor for VR to achieve the best display effect and take the resistance value at this time.

VDD=2.4V-5.2V

These four weak pull-up resistors are optional, but recommended under high-interference conditions.

VDD

J1
MCU_CONNECT

R1 4.7K R1 4.7K R3 4.7K R4 4.7K

1
2
3 CS
4 RD
5 WR
6 DATA

CS
RD
WR
DATA
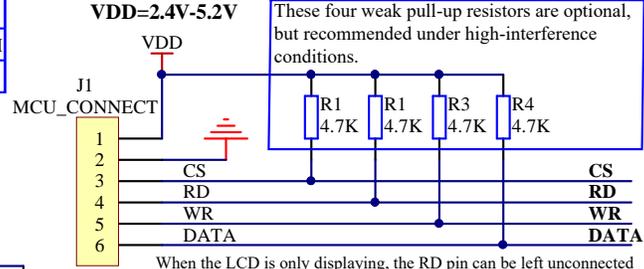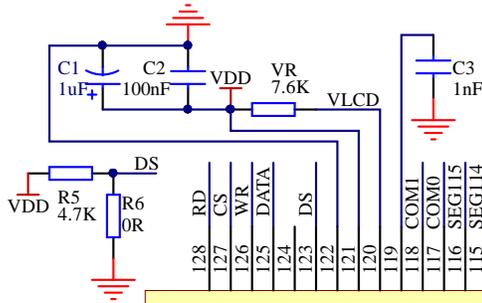
When the LCD is only displaying, the RD pin can be left unconnected
For high interference, connect a 10R-1k resistor in series with a small capacitor (pF) to ground.

C1 1uF C2 100nF VDD VR 7.6K VLCD C3 1nF

VDD R5 4.7K R6 0R DS

U1
VK232_LQFP128(0.4)

SEG0–SEG95, COM0, COM1, RD, CS, WR, DATA, TEST, DS, VSS, VDD, VLCD, VCAP

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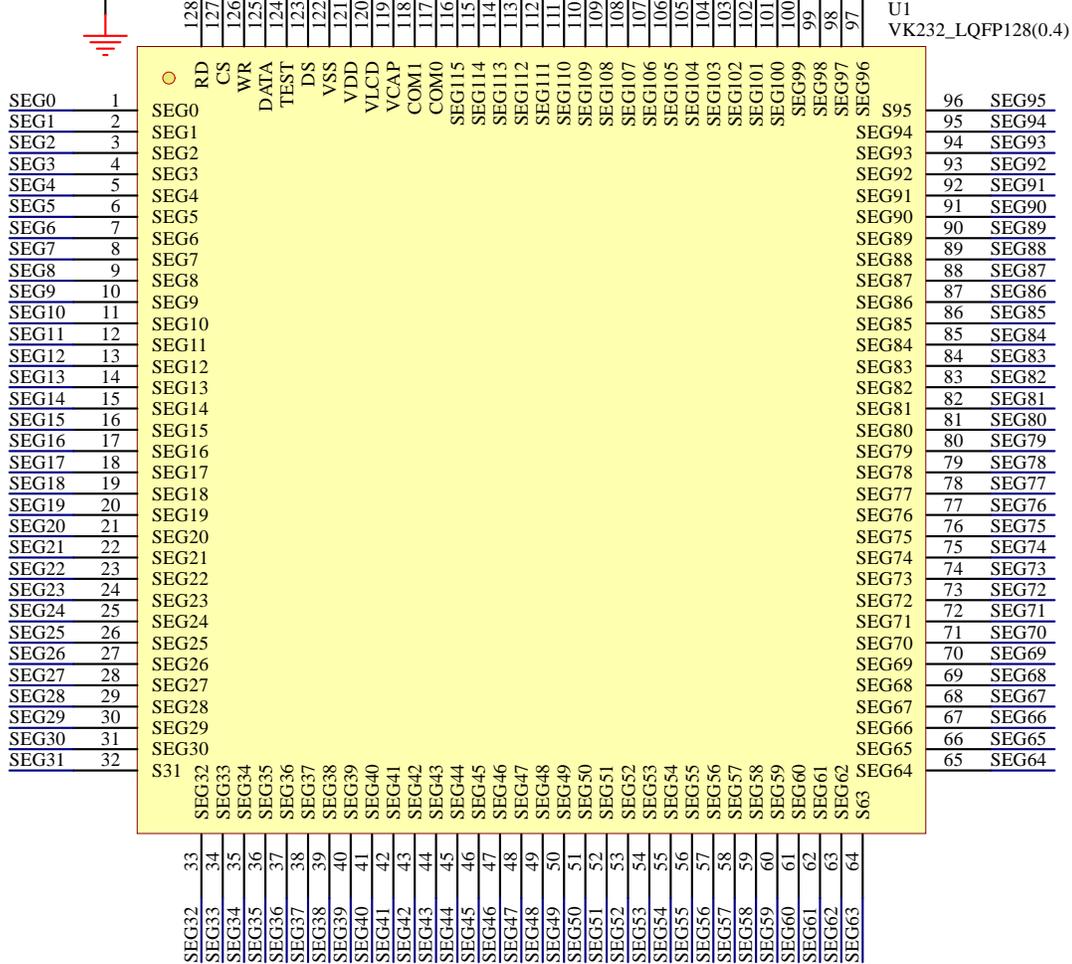
The SEG pins can be shuffled for the convenience of PCB routing
Note that when writing software, the sequence corresponding to the displayed RAM should also be changed

Dynamic LCD 1/2BIAS 2COM

COM1 COM0 LCD2COM

C1 C0 | C1 C0

LCD116X2

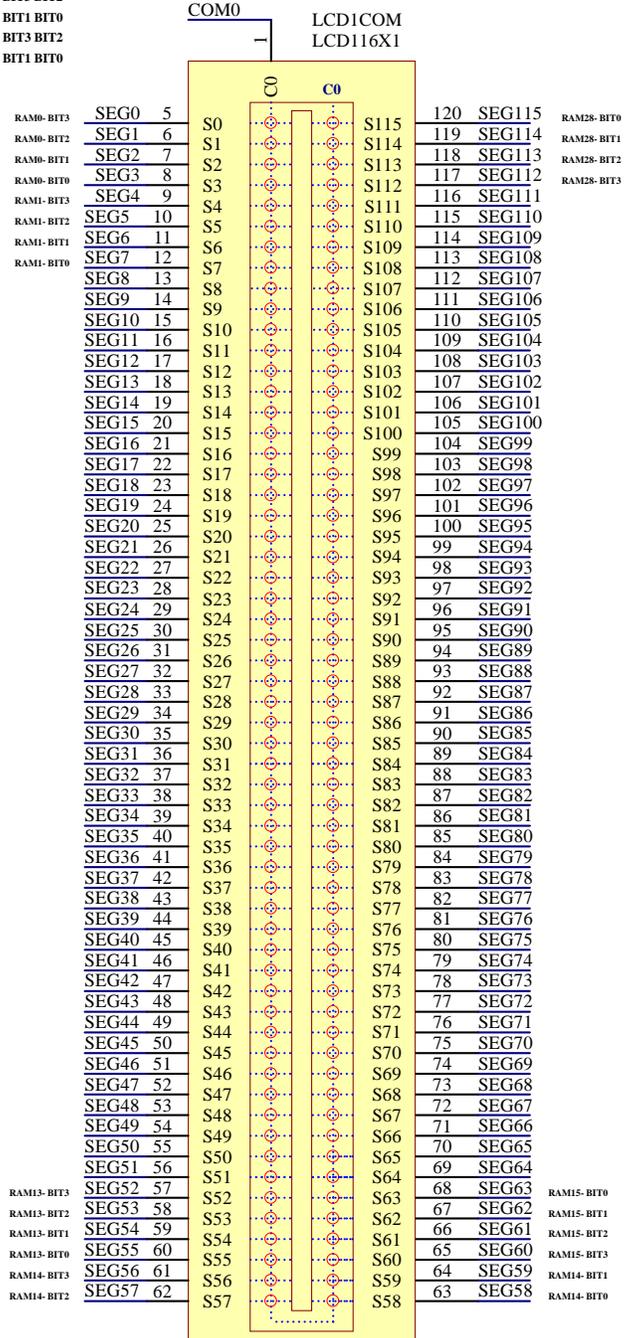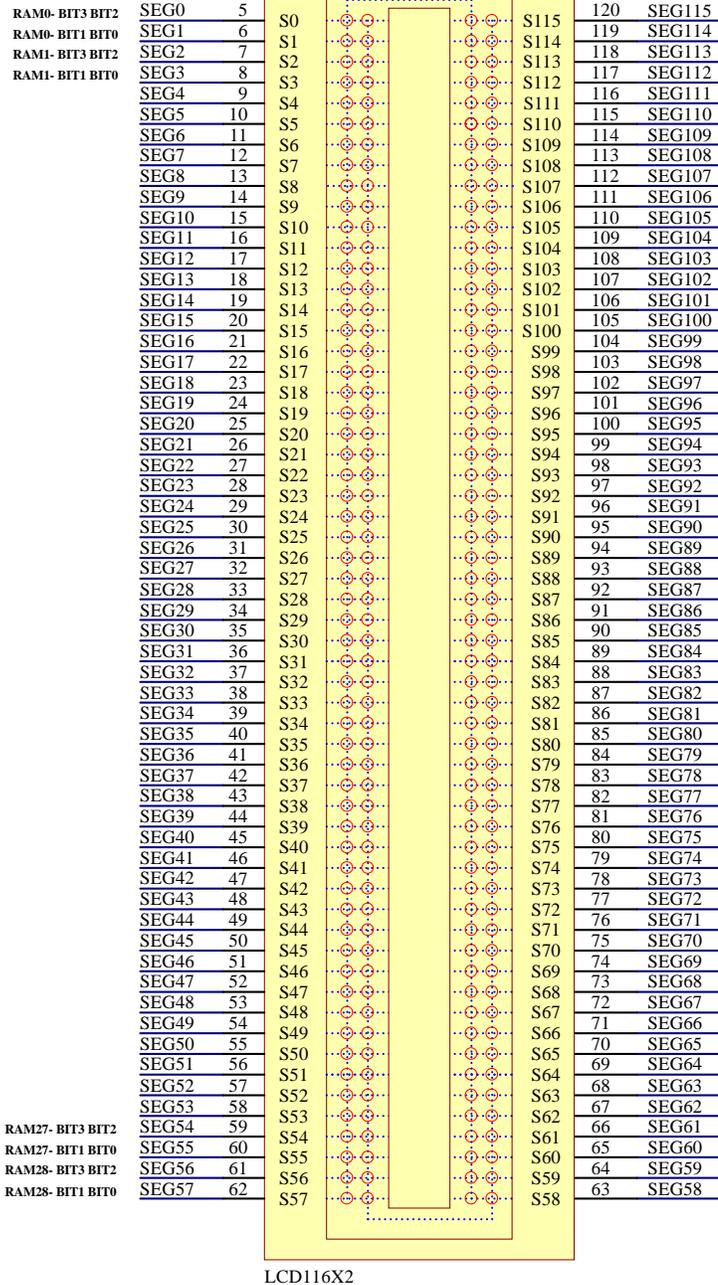| RAM	SEG	Pin	S		S	Pin	SEG	RAM
RAM0- BIT3 BIT2	SEG0	5	S0		S115	120	SEG115	RAM57- BIT3 BIT2
RAM0- BIT1 BIT0	SEG1	6	S1		S114	119	SEG114	RAM57- BIT1 BIT0
RAM1- BIT3 BIT2	SEG2	7	S2		S113	118	SEG113	RAM56- BIT3 BIT2
RAM1- BIT1 BIT0	SEG3	8	S3		S112	117	SEG112	RAM56- BIT1 BIT0
	SEG4	9	S4		S111	116	SEG111	
	SEG5	10	S5		S110	115	SEG110	
	SEG6	11	S6		S109	114	SEG109	
	SEG7	12	S7		S108	113	SEG108	
	SEG8	13	S8		S107	112	SEG107	
	SEG9	14	S9		S106	111	SEG106	
	SEG10	15	S10		S105	110	SEG105	
	SEG11	16	S11		S104	109	SEG104	
	SEG12	17	S12		S103	108	SEG103	
	SEG13	18	S13		S102	107	SEG102	
	SEG14	19	S14		S101	106	SEG101	
	SEG15	20	S15		S100	105	SEG100	
	SEG16	21	S16		S99	104	SEG99	
	SEG17	22	S17		S98	103	SEG98	
	SEG18	23	S18		S97	102	SEG97	
	SEG19	24	S19		S96	101	SEG96	
	SEG20	25	S20		S95	100	SEG95	
	SEG21	26	S21		S94	99	SEG94	
	SEG22	27	S22		S93	98	SEG93	
	SEG23	28	S23		S92	97	SEG92	
	SEG24	29	S24		S91	96	SEG91	
	SEG25	30	S25		S90	95	SEG90	
	SEG26	31	S26		S89	94	SEG89	
	SEG27	32	S27		S88	93	SEG88	
	SEG28	33	S28		S87	92	SEG87	
	SEG29	34	S29		S86	91	SEG86	
	SEG30	35	S30		S85	90	SEG85	
	SEG31	36	S31		S84	89	SEG84	
	SEG32	37	S32		S83	88	SEG83	
	SEG33	38	S33		S82	87	SEG82	
	SEG34	39	S34		S81	86	SEG81	
	SEG35	40	S35		S80	85	SEG80	
	SEG36	41	S36		S79	84	SEG79	
	SEG37	42	S37		S78	83	SEG78	
	SEG38	43	S38		S77	82	SEG77	
	SEG39	44	S39		S76	81	SEG76	
	SEG40	45	S40		S75	80	SEG75	
	SEG41	46	S41		S74	79	SEG74	
	SEG42	47	S42		S73	78	SEG73	
	SEG43	48	S43		S72	77	SEG72	
	SEG44	49	S44		S71	76	SEG71	
	SEG45	50	S45		S70	75	SEG70	
	SEG46	51	S46		S69	74	SEG69	
	SEG47	52	S47		S68	73	SEG68	
	SEG48	53	S48		S67	72	SEG67	
	SEG49	54	S49		S66	71	SEG66	
	SEG50	55	S50		S65	70	SEG65	
	SEG51	56	S51		S64	69	SEG64	
	SEG52	57	S52		S63	68	SEG63	
	SEG53	58	S53		S62	67	SEG62	
RAM27- BIT3 BIT2	SEG54	59	S54		S61	66	SEG61	
RAM27- BIT1 BIT0	SEG55	60	S55		S60	65	SEG60	
RAM28- BIT3 BIT2	SEG56	61	S56		S59	64	SEG59	
RAM28- BIT1 BIT0	SEG57	62	S57		S58	63	SEG58	

Static LCD
COM0 and COM1 can be short-circuited together

COM0 LCD1COM LCD116X1

C0 | C0

RAM	SEG	Pin	S		S	Pin	SEG	RAM
RAM0- BIT3	SEG0	5	S0		S115	120	SEG115	RAM28- BIT0
RAM0- BIT2	SEG1	6	S1		S114	119	SEG114	RAM28- BIT1
RAM0- BIT1	SEG2	7	S2		S113	118	SEG113	RAM28- BIT2
RAM0- BIT0	SEG3	8	S3		S112	117	SEG112	RAM28- BIT3
RAM1- BIT3	SEG4	9	S4		S111	116	SEG111	
RAM1- BIT2	SEG5	10	S5		S110	115	SEG110	
RAM1- BIT1	SEG6	11	S6		S109	114	SEG109	
RAM1- BIT0	SEG7	12	S7		S108	113	SEG108	
	SEG8	13	S8		S107	112	SEG107	
	SEG9	14	S9		S106	111	SEG106	
	SEG10	15	S10		S105	110	SEG105	
	SEG11	16	S11		S104	109	SEG104	
	SEG12	17	S12		S103	108	SEG103	
	SEG13	18	S13		S102	107	SEG102	
	SEG14	19	S14		S101	106	SEG101	
	SEG15	20	S15		S100	105	SEG100	
	SEG16	21	S16		S99	104	SEG99	
	SEG17	22	S17		S98	103	SEG98	
	SEG18	23	S18		S97	102	SEG97	
	SEG19	24	S19		S96	101	SEG96	
	SEG20	25	S20		S95	100	SEG95	
	SEG21	26	S21		S94	99	SEG94	
	SEG22	27	S22		S93	98	SEG93	
	SEG23	28	S23		S92	97	SEG92	
	SEG24	29	S24		S91	96	SEG91	
	SEG25	30	S25		S90	95	SEG90	
	SEG26	31	S26		S89	94	SEG89	
	SEG27	32	S27		S88	93	SEG88	
	SEG28	33	S28		S87	92	SEG87	
	SEG29	34	S29		S86	91	SEG86	
	SEG30	35	S30		S85	90	SEG85	
	SEG31	36	S31		S84	89	SEG84	
	SEG32	37	S32		S83	88	SEG83	
	SEG33	38	S33		S82	87	SEG82	
	SEG34	39	S34		S81	86	SEG81	
	SEG35	40	S35		S80	85	SEG80	
	SEG36	41	S36		S79	84	SEG79	
	SEG37	42	S37		S78	83	SEG78	
	SEG38	43	S38		S77	82	SEG77	
	SEG39	44	S39		S76	81	SEG76	
	SEG40	45	S40		S75	80	SEG75	
	SEG41	46	S41		S74	79	SEG74	
	SEG42	47	S42		S73	78	SEG73	
	SEG43	48	S43		S72	77	SEG72	
	SEG44	49	S44		S71	76	SEG71	
	SEG45	50	S45		S70	75	SEG70	
	SEG46	51	S46		S69	74	SEG69	
	SEG47	52	S47		S68	73	SEG68	
	SEG48	53	S48		S67	72	SEG67	
	SEG49	54	S49		S66	71	SEG66	
	SEG50	55	S50		S65	70	SEG65	
	SEG51	56	S51		S64	69	SEG64	
RAM13- BIT3	SEG52	57	S52		S63	68	SEG63	RAM15- BIT0
RAM13- BIT2	SEG53	58	S53		S62	67	SEG62	RAM15- BIT1
RAM13- BIT1	SEG54	59	S54		S61	66	SEG61	RAM15- BIT2
RAM13- BIT0	SEG55	60	S55		S60	65	SEG60	RAM15- BIT3
RAM14- BIT3	SEG56	61	S56		S59	64	SEG59	RAM14- BIT1
RAM14- BIT2	SEG57	62	S57		S58	63	SEG58	RAM14- BIT0

10　Electrical Characteristics

10.1　Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	$-0.3\sim5.5$	V
Input voltage	VIN	$V_{SS}-0.3\sim V_{DD}+0.3$	V
Storage temperature	T_{STG}	$-50\sim+125$	℃
Operating Temperature	T_{OTG}	$-40\sim+85$	℃

10.2　DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	2.4	—	5.2	V	—	—
Operating current	I_{DD1}	—	150	300	μA	3V	No load/LCD ON On-chip RC oscillator
		—	300	600		5V	
Standby Current	I_{STB}	—	0.1	5	μA	3V	No load, Power down mode
		—	0.3	10		5V	
Low-level Input	V_{IL}	0	—	0.6	V	3V	DATA,/WR,/CS
		0	—	1.0		5V	
High-level Input	V_{IH}	2.4	—	3.0	V	3V	DATA,/WR,/CS
		4.0	—	5.0		5V	
DATA	I_{OL}	0.5	1.2	—	mA	3V	VOL=0.3V
		1.3	2.6	—		5V	VOL=0.5V
DATA	I_{OH}	-0.4	-0.8	—	mA	3V	VOL=2.7V
		-0.9	-1.8	—		5V	VOL=4.5V
LCD COM Sink Current	I_{OL1}	80	150	—	μA	3V	VOL=0.3V
		150	250	—		5V	VOL=0.5V
LCD COM Source Current	I_{OH1}	-80	-120	—	μA	3V	VOH=2.7V
		-120	-200	—		5V	VOH=4.5V
LCD SEG Sink Current	I_{OL2}	60	120	—	μA	3V	VOL=0.3V
		-120	200	—		5V	VOL=0.5V
LCD SEG Source Current	I_{OH2}	-40	-70	—	μA	3V	VOH=2.7V
		-70	-100	—		5V	VOH=4.5V
Pull-UP Resistor RUP	R_{PH}	40	80	150	KΩ	3V	DATA,/WR,/CS
		30	60	100		5V	

10.3 AC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
System Clock	f_{SYS1}	192	256	320	kHz	3V	On-chip RC oscillator
		—	256	—		5V	
LCD Clock	f_{LCD1}	—	$f_{SYS1}/1024$	—	Hz	—	On-chip RC oscillator
LCD Common Period	t_{COM}	—	n/f_{LCD}	—	sec	—	N：Number of COM
Serial Data Clock （/WR，/RD ）	F_{CLK1}	—	—	150	kHz	3V	Duty cycle 50%
		—	—	300		5V	
Serial Interface Reset PW	t_{CS}	—	250	—	ns	—	/CS
/WR，/RD Input pulse width	t_{CLK}	3.34	—	—	μA	3V	Write mode
		1.67	—	—	μA	5V	Write mode
Rise/fall time serial data time width	t_r，t_f	—	120	—	ns	3V	—
						5V	
Setup Time for DATA to /WR,/RD Clock Width	t_{su}	—	120	—	ns	3V	—
						5V	
Hold Time for DATA to /WR,/RD Clock Width	t_h	—	120	—	ns	3V	—
						5V	
Setup Time for /CS to /WR,/RD Clock Width	t_{su1}	—	100	—	ns	3V	—
						5V	
Hold Time for /CS to /WR,/RD Clock Width	t_{h1}	—	100	—	ns	3V	—
						5V	

11   Package Information

11.1   LQFP128(14.0mm×14.0mm PP=0.4mm)

DETALL:F

BASE METAL   WITH PLATING

SECTION B-B
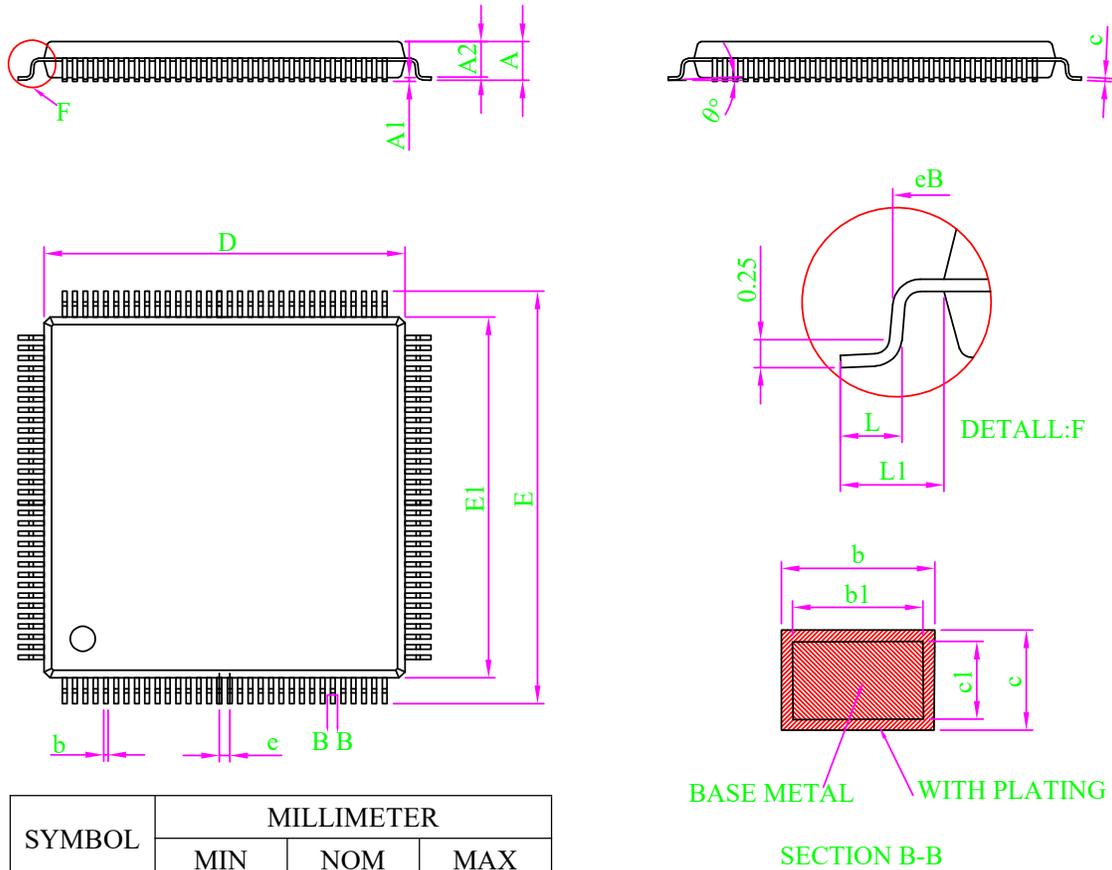
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.70
A1	0.10	0.15	0.20
A2	1.30	1.40	1.50
b	0.14	-	0.22
b1	0.13	0.16	0.19
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
eB	15.05	-	15.40
e	0.40 BSC		
L	0.42	0.57	0.72
L1	0.95	1.00	1.15
θ	0	-	10°

Note：

1. All dimension are in mm.

2. Dim D&El does not include plastic flash；
    Flash:Plastic residual around body edge after
    de junk/singulation.

3. Dim b does not include dambar protrusion/
    intrusion.

4. Plating thickness 0.007mm-0.015mm

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13 Revision History

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Initial release	YES
2	1.1	2018-10-11	Add reference circuit	YES
3	1.2	2019-03-21	Alignment correction	YES
4	1.3	2025-08-29	Change Description	YES

[1] Please refer to the latest version of this document before starting or finalizing any design.

[2] Since the release of this document, the status or availability of this product may have changed. For the most up-to-date information, please visit: https://www.szvinka.com/