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# VKS118 Datasheet

## 118×1 LCD DRIVER

### Rev.1.3

# 1   General Description

VKS118 is a dot-matrix store-mapped LCD driver that can support LCD screens with a maximum of 118 static scanning points (118SEG×1COM). The single-chip microcomputer can be configured to display parameters and read and write display data through a 5-wire (with 2 chip pins) serial interface, and can also enter power-saving mode through instructions. It has the characteristics of good contrast, wide viewing Angle and no flicker. It is suitable for products that require high display quality, such as washing machine panels, automotive instruments, and household appliances.

# 2   Key Features

- Operating voltage：2.4-5.2V
- Built-in RC oscillator (default)
- Static display, 100% duty cycle without bias
- Built-in display RAM
- Power-saving mode (accessed by turning off the display and the oscillator)
- 5-wire (2 pin headers) serial interface
- Display mode: 118×1
- Software-configurable LCD parameters
- There are two command formats: writing commands and reading and writing data
- Auto-increment addressing for sequential read/write
- The VLCD pin provides the LCD drive voltage source (≤VDD).
- Three access methods for displaying data
- Available Packages:
  LQFP128(14.0mm × 14.0mm PP=0.4mm)

# 3 Product Selection

| Part No. | SEG/COM | Bias | Duty | Packaging |
|---|---|---|---|---|
| VKS114 | 58×1/57×2/56×3/55×4 | 1/1, 1/2,1/3 1/4 | 1/1, 1/2,1/3 1/4 | LQFP64 |
| VKS118 | 118×1 | 1/1 | 1/1 | LQFP128 |
| VKS146 | 74×1/73×2/72×3/71×4 | 1/1, 1/2,1/3 1/4 | 1/1, 1/2,1/3 1/4 | LQFP80 |
| VKS232 | 116×1/116×2 | 1/1，1/2 | 1/1，1/2 | LQFP128 |

# 4 Ordering Information

| Part No. | Packaging | Tube Qty | Tray(reel)Qty | Box Qty | Total Qty | Notes |
|---|---|---|---|---|---|---|
| VKS114 | LQFP64 | - | 250/tray | 2500/box | 15000 PCS | |
| VKS118 | LQFP128 | - | 90/tray | 900/box | 5400 PCS | |
| VKS146 | LQFP80 | - | 90/tray | 900/box | 54000 PCS | |
| VKS232 | LQFP128 | - | 90/tray | 900/box | 5400 PCS | |

## 5 Package Pinout Information(LQFP128)



For more information:

## 5.1　VKS118/LQFP128 Pin Description

| No. | Name | I/O | Function |
|-----|------|-----|----------|
| 1-118 | SEG0-SEG117 | O | LCD SEG drive outputs |
| 119-120 | COM0,COM1 | O | LCD COM drive outputs |
| 121 | VLCD | I | LCD driver voltage |
| 122 | VDD | VDD | Positive power supply |
| 123 | GND | GND | Negative power supply |
| 124 | DATA | I/O | The bidirectional data pin is equipped with a built-in pull-up resistor |
| 125 | /WR | I | The write signal is equipped with an internal pull-up resistor, and the rising edge of the signal locks the data to the display RAM. |
| 126 | /CS1 | I | Select 1 on the page, corresponding to SEG0-SEG63 |
| 127 | /CS2 | I | Select 2 on the page, corresponding to SEG64-SEG117 |
| 128 | /RD | I | Read the signal with an internal pull-up resistor. Read the DATA to the DATA pin along the falling edge of the signal. |

# 6    Functional Description

## 6.1    Block Diagram
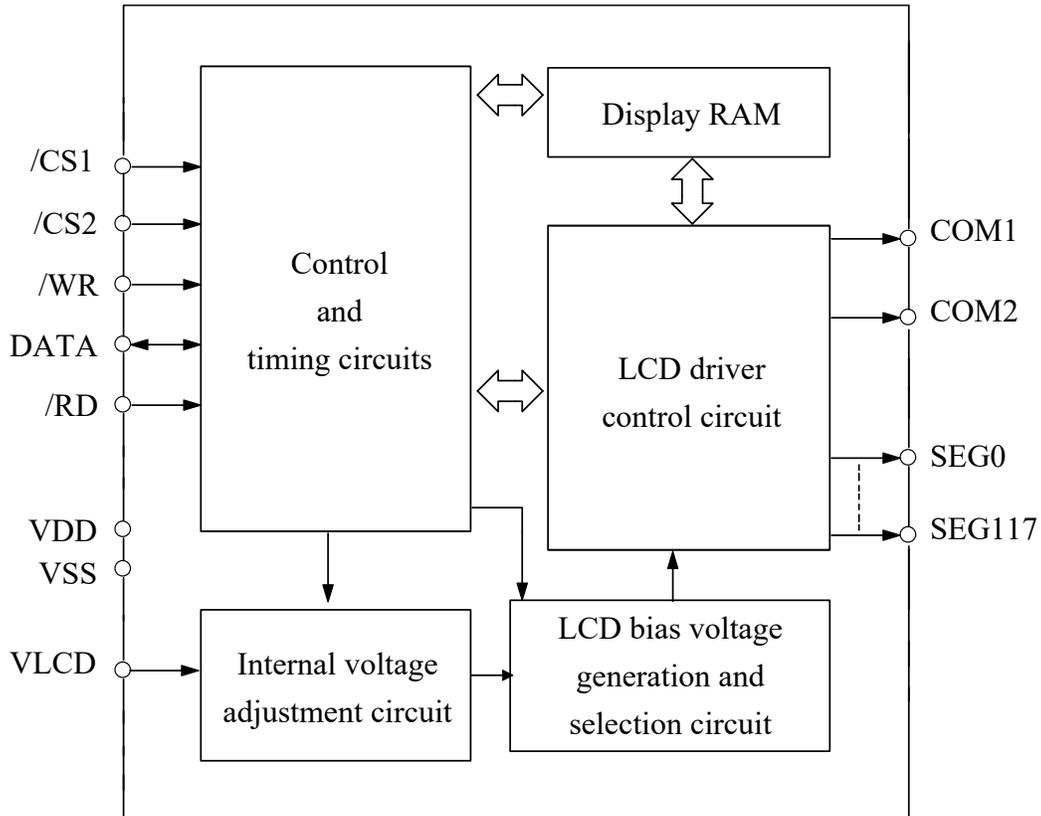
## 6.2 Display RAM- Storage structure

The static display memory (RAM) structure is 118 bits and stores the displayed data. The content of the display RAM is directly mapped to the display content of the LCD driver. Store data in RAM by writing commands. The built-in RAM is divided into two pages, with the corresponding enable terminals being /CS1 and /CS2 respectively. The first page is 32×2 bits corresponding to SEG0-SEG63, and the second page is 27×2 bits corresponding to SEG64-SEG117.

The process of mapping the contents in the RAM to the LCD is shown in the following table:

Two static channels (COM0.COM1 signals are the same) :

| | | COM0 | | | |
|---|---|---|---|---|---|
| | | SEG0 | SEG1 | 0 | |
| | | SEG2 | SEG3 | 1 | Page 1 |
| | | SEG4 | SEG5 | 2 | Address: 6 digits |
| | | SEG6 | SEG7 | 3 | (A5,A4-- A0) |
| | | ⋮ | ⋮ | | Triggered by /CS1 |
| | | SEG62 | SEG63 | 31 | |
| D3 | D2 | D1 | D0 | Data/Addr | |

| | | SEG64 | SE65 | 0 | |
|---|---|---|---|---|---|
| | | SEG66 | SEG67 | 1 | Page 2 |
| | | SEG68 | SEG69 | 2 | Address: 6 digits |
| | | SEG70 | SEG71 | 3 | (A5,A4-- A0) |
| | | ⋮ | ⋮ | | Triggered by /CS2 |
| | | SEG116 | SEG117 | 26 | |
| D3 | D2 | D1 | D0 | Data/Addr | |

## 6.3  LCD Driver

The VKS118 is a dot-matrix LCD driver that drives 118×1 display points, providing static display with a 100% duty cycle without bias. The on-chip RC oscillator frequency is adopted.

The output voltage waveform of the LCD driver terminal is as follows:
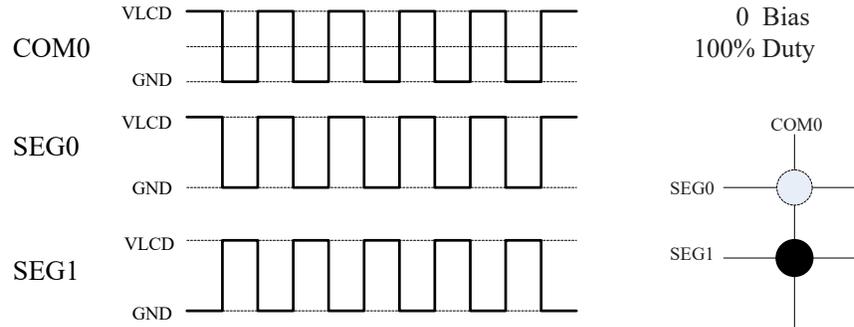


Note: To enhance the driving capability of COM0, the output of COM1 is the same as that of COM0.

## 6.4  Communication Interface

The VKS118 has five communication pins (including two chip selection pins). The signals on pins CS1 and /CS2 are used to enable/disable communication with the main controller. High levels of CS1 and /CS2 disable and initialize the internal timing, while low levels enable CS1 and /CS2. The following are the precautions for pin selection when using the two chips:

1) The command mode is only valid for /CS1.
2) Both write modes /CS1 and /CS2 are effective. (When both /CS1 and /CS2 are low, data will be written to 2 pages of RAM simultaneously. This situation should be avoided.)
3) In read mode, it is not allowed for both /CS1 and /CS2 to be low at the same time; otherwise, it will cause status conflicts and display errors.

The DATA pin is a serial data input/output pin. Reading/writing data or writing commands must be done through the data pin.
The /RD pin is the READ clock input. The DATA in the RAM is read to the Data pin at the falling edge of the /RD signal, and the main controller reads the correct data between the rising edge and the next falling edge of the read signal.
The /WR pin is the clock input pin. The DATA, address or command on the data pin is read to VKS118 at the rising edge of the /WR signal.

## 6.5  Command Format

The VKS118 can be operated through software. There are two modes for configuring VKS118 parameters and transmitting LCD display data commands, namely command mode and data mode. The configuration of VKS118 is called command mode, with the ID being 100. The data modes are respectively reading data and writing data. The operation ID for reading data is 110, the operation ID for writing data is 101, and the operation ID for Read-Modify-Write data is also 101.

The ID codes are shown in the table below：

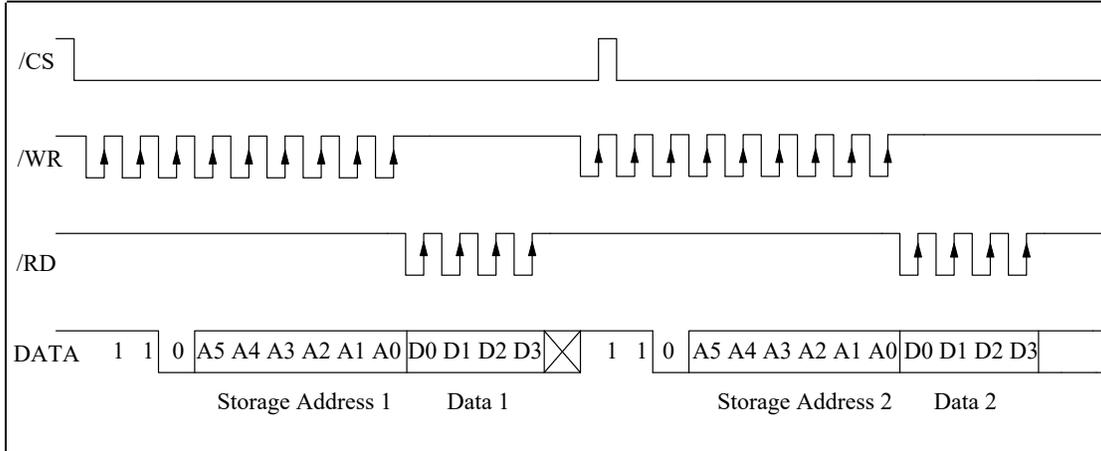| Command | MODE | ID |
|---|---|---|
| READ | DATA | 110 |
| WRITE | DATA | 101 |
| Read-Modify-Write | DATA | 101 |
| COMMAND | COMMAND | 100 |

Note:

When both /CS1 and /CS2 are at low levels in command mode, only /CS1 is valid. In write mode, it is valid simultaneously when both /CS1 and /CS2 are at low levels. In the reading mode /CS1 and /CS2, low levels must not occur simultaneously; otherwise, internal circuit state conflicts will arise, causing internal short circuits and display errors.
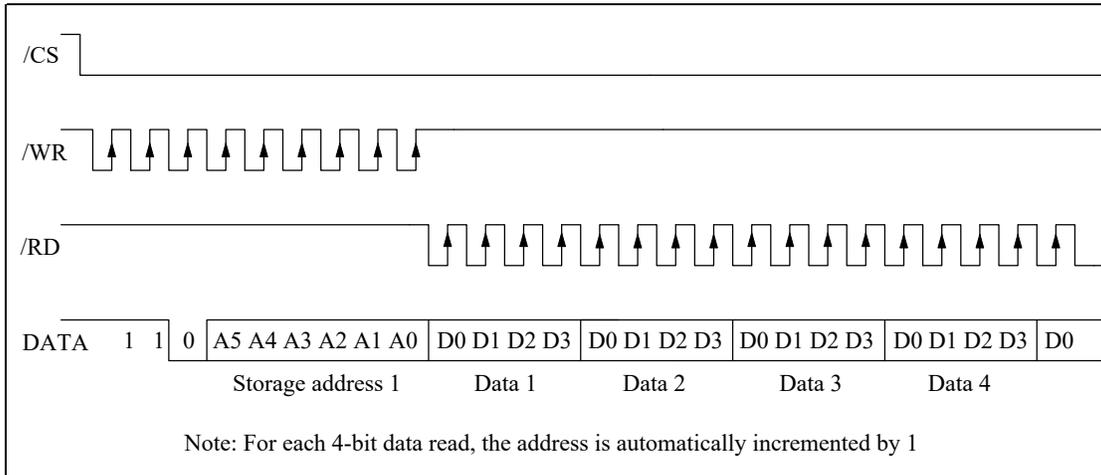
# 7 CMD/Data Timing Diagrams
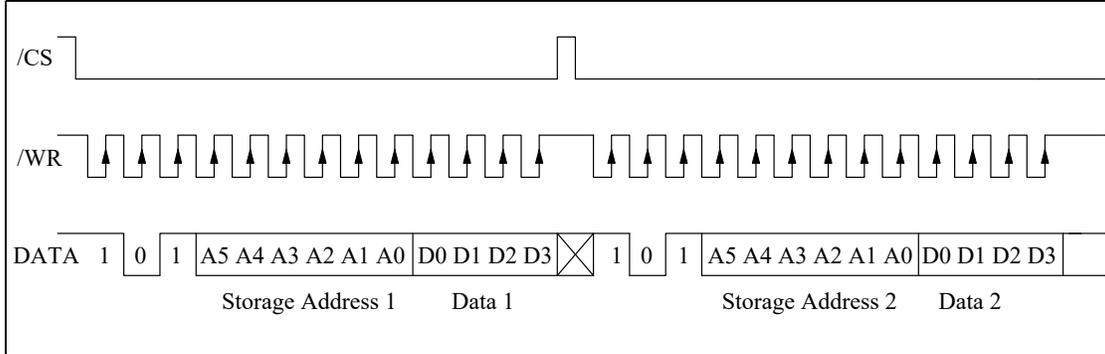
## 7.1 READ Mode

Command Code : 110



Successive Address Reading

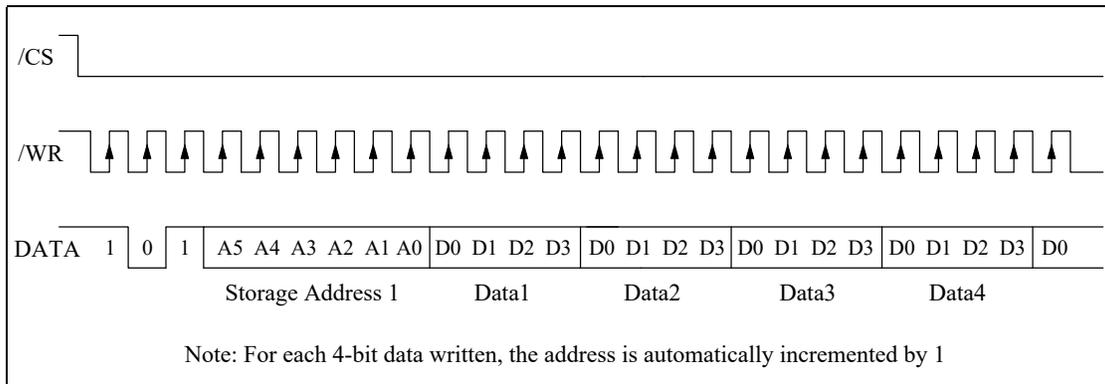## 7.2 WRITE Mode

Command Code : 101



Successive Address Writing

## 7.3 Read-Modify-Write Mode

Command Code : 101



Note: After reading 4-bit data, the address remains unchanged. After writing 4-bit data is the same address.
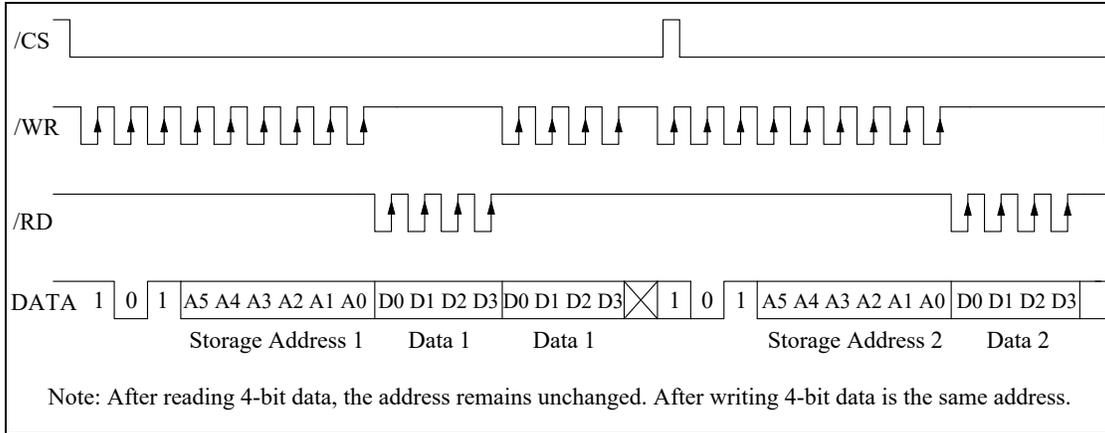
Successive Address Accessing



Note: After reading 4-bit data, the address remains unchanged. After writing 4-bit data, the address automatically increase by 1.
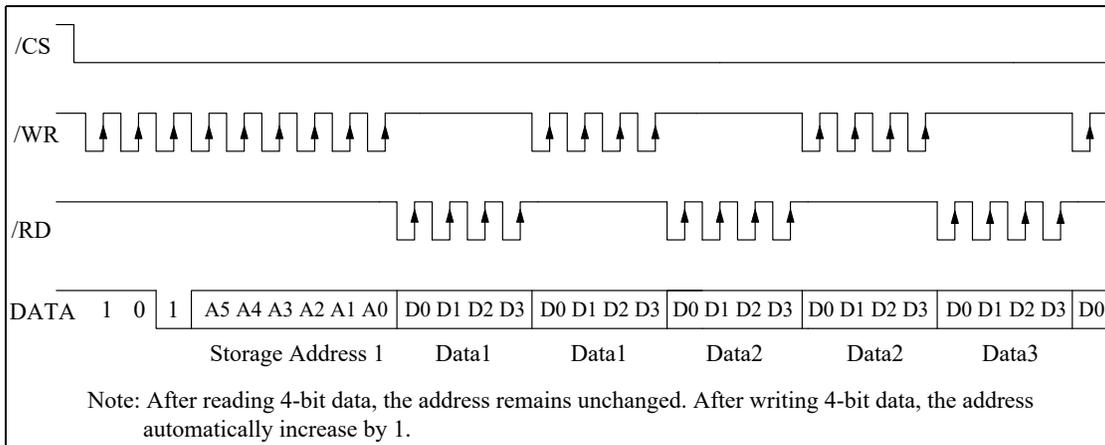
## 7.4 Command Mode

Command Code : 100



## 8 Command Summary

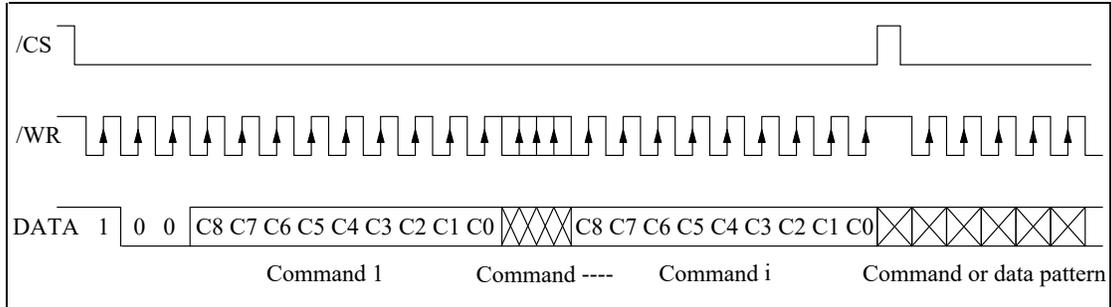| Name | ID | Command Code | D/C | Function | Def. |
|---|---|---|---|---|---|
| READ | 110 | A5A4A3A2A1A0D0D1D2D3 | D | Read data from RAM | |
| WRITE | 101 | A5A4A3A2A1A0D0D1D2D3 | D | Write the data into RAM | |
| READ-MODIFY-WRITE | 101 | A5A4A3A2A1A0D0D1D2D3 | D | Read and write data from RAM | |
| SYS DIS | 100 | 0000-0000- X | C | Turn off system oscillator | YES |
| SYS EN | 100 | 0000-0001- X | C | Turn on the system clock | |
| LCD OFF | 100 | 0000-0010- X | C | Turn off the LCD bias generator | YES |
| LCD ON | 100 | 0000-0011- X | C | Turn on the LCD bias generator | |

Note: X: 0 or 1                      D/C: Data/Command Mode

A5-A0: Display the RAM bit address      Reset: Default state upon power-on

D3-D0: 4-bit display data               110,101 and 100 are instruction ids

# 9 Application Circuits

When the power supply for the single-chip microcomputer (3.3V) and the driver chip (5V) is inconsistent, it is recommended to add a level conversion circuit to the communication pin. When the LCD only displays, the RD pin can be left unconnected. When the surrounding interference is relatively large, a 10R to 1k resistor and a PF-class small capacitor to ground can be connected in series on the communication pin
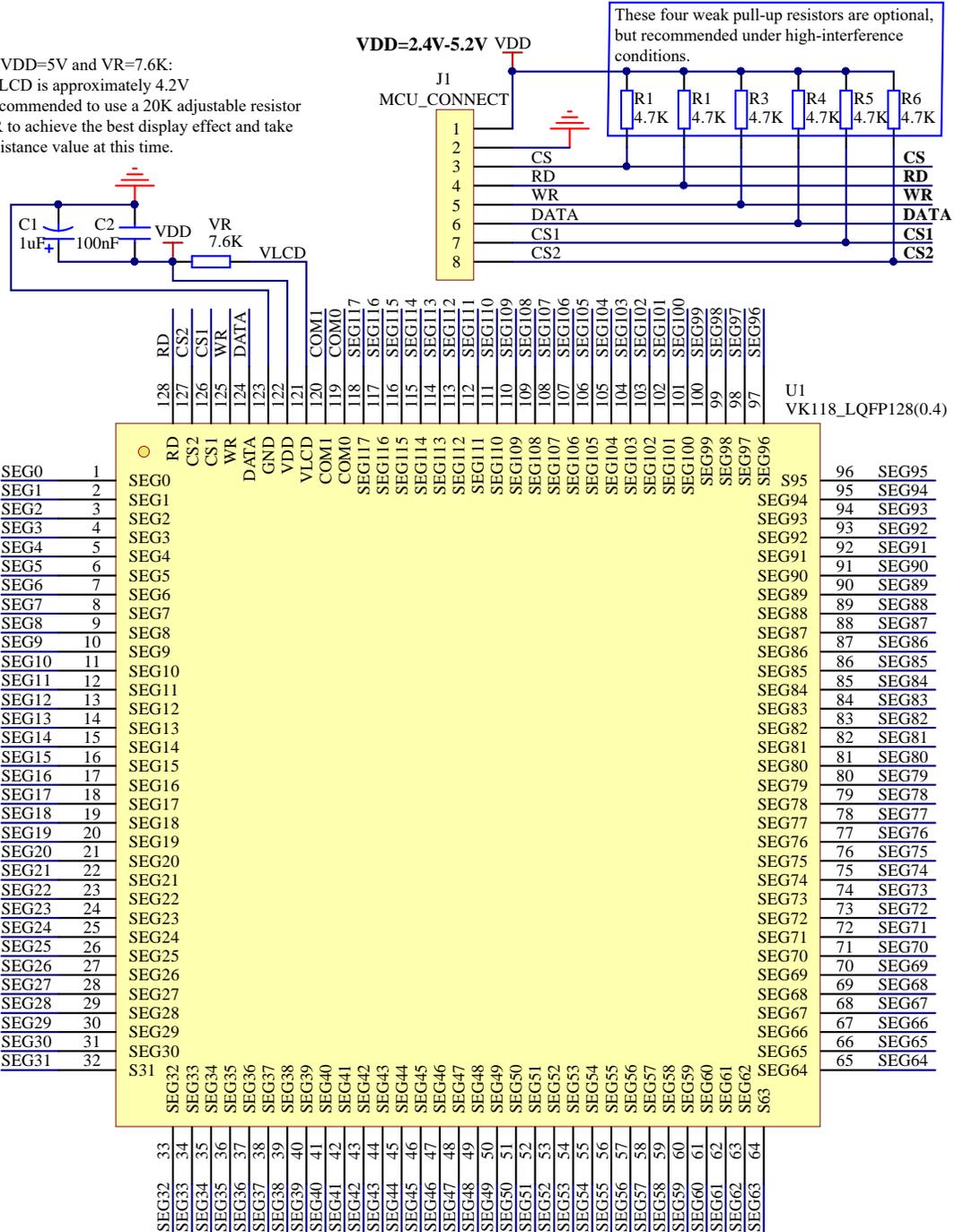
Static LCD
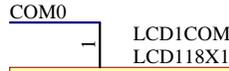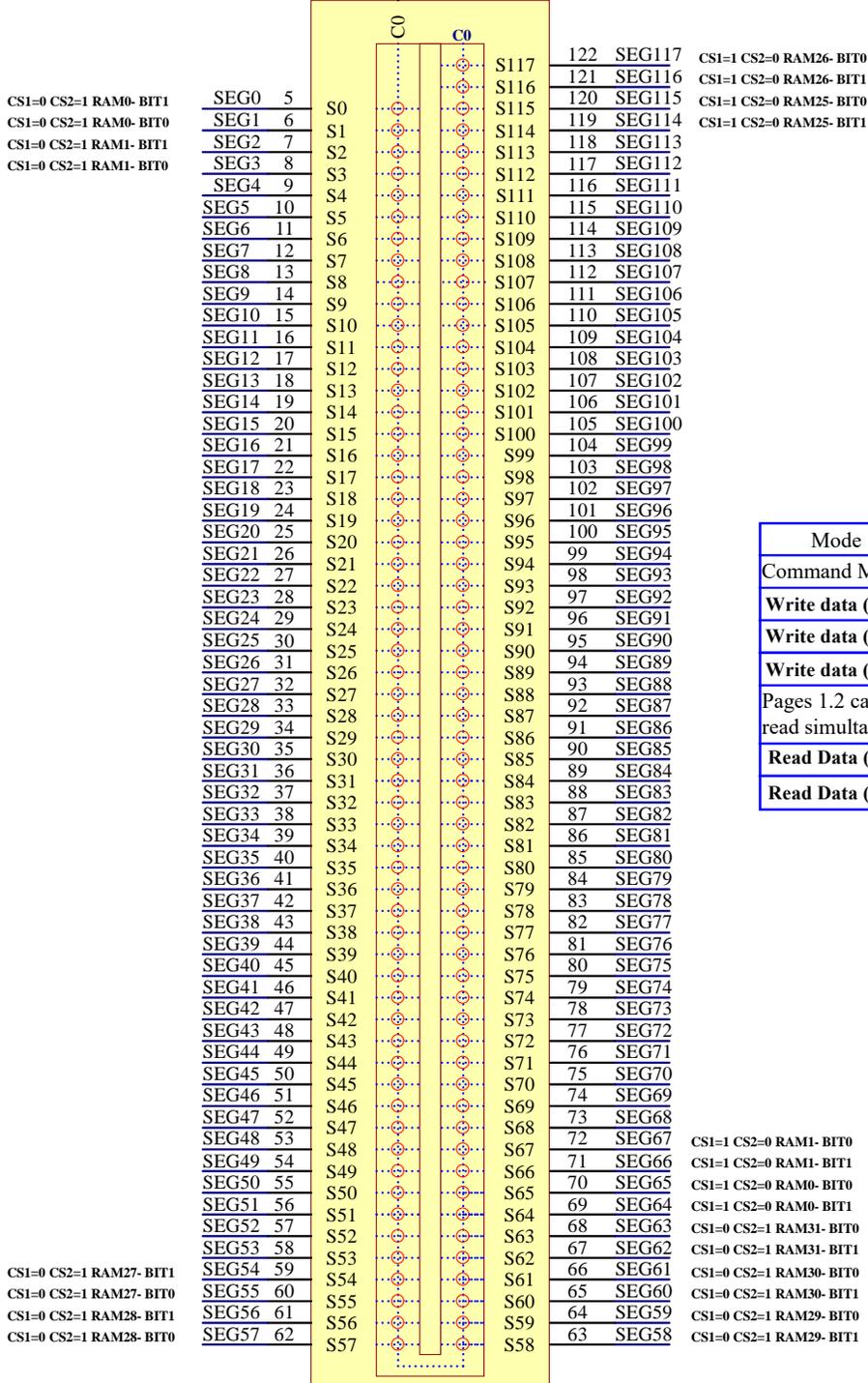COM0 and COM1 can be short-circuited together

COM0

LCD1COM
LCD118X1

The SEG pins can be shuffled for the convenience of PCB routing
Note that when writing software, the sequence corresponding to the displayed RAM should also be changed

**Left side SEG labels:**

CS1=0 CS2=1 RAM0- BIT1
CS1=0 CS2=1 RAM0- BIT0
CS1=0 CS2=1 RAM1- BIT1
CS1=0 CS2=1 RAM1- BIT0

| SEG | Pin | | SEG | Pin |
| --- | --- | --- | --- | --- |
| SEG0 | 5 | | SEG29 | 34 |
| SEG1 | 6 | | SEG30 | 35 |
| SEG2 | 7 | | SEG31 | 36 |
| SEG3 | 8 | | SEG32 | 37 |
| SEG4 | 9 | | SEG33 | 38 |
| SEG5 | 10 | | SEG34 | 39 |
| SEG6 | 11 | | SEG35 | 40 |
| SEG7 | 12 | | SEG36 | 41 |
| SEG8 | 13 | | SEG37 | 42 |
| SEG9 | 14 | | SEG38 | 43 |
| SEG10 | 15 | | SEG39 | 44 |
| SEG11 | 16 | | SEG40 | 45 |
| SEG12 | 17 | | SEG41 | 46 |
| SEG13 | 18 | | SEG42 | 47 |
| SEG14 | 19 | | SEG43 | 48 |
| SEG15 | 20 | | SEG44 | 49 |
| SEG16 | 21 | | SEG45 | 50 |
| SEG17 | 22 | | SEG46 | 51 |
| SEG18 | 23 | | SEG47 | 52 |
| SEG19 | 24 | | SEG48 | 53 |
| SEG20 | 25 | | SEG49 | 54 |
| SEG21 | 26 | | SEG50 | 55 |
| SEG22 | 27 | | SEG51 | 56 |
| SEG23 | 28 | | SEG52 | 57 |
| SEG24 | 29 | | SEG53 | 58 |
| SEG25 | 30 | | SEG54 | 59 |
| SEG26 | 31 | | SEG55 | 60 |
| SEG27 | 32 | | SEG56 | 61 |
| SEG28 | 33 | | SEG57 | 62 |

CS1=0 CS2=1 RAM27- BIT1
CS1=0 CS2=1 RAM27- BIT0
CS1=0 CS2=1 RAM28- BIT1
CS1=0 CS2=1 RAM28- BIT0

**Internal segment lines:** S0–S117

**Right side SEG labels:**

| Pin | SEG |
| --- | --- |
| 122 | SEG117 |
| 121 | SEG116 |
| 120 | SEG115 |
| 119 | SEG114 |
| 118 | SEG113 |
| 117 | SEG112 |
| 116 | SEG111 |
| 115 | SEG110 |
| 114 | SEG109 |
| 113 | SEG108 |
| 112 | SEG107 |
| 111 | SEG106 |
| 110 | SEG105 |
| 109 | SEG104 |
| 108 | SEG103 |
| 107 | SEG102 |
| 106 | SEG101 |
| 105 | SEG100 |
| 104 | SEG99 |
| 103 | SEG98 |
| 102 | SEG97 |
| 101 | SEG96 |
| 100 | SEG95 |
| 99 | SEG94 |
| 98 | SEG93 |
| 97 | SEG92 |
| 96 | SEG91 |
| 95 | SEG90 |
| 94 | SEG89 |
| 93 | SEG88 |
| 92 | SEG87 |
| 91 | SEG86 |
| 90 | SEG85 |
| 89 | SEG84 |
| 88 | SEG83 |
| 87 | SEG82 |
| 86 | SEG81 |
| 85 | SEG80 |
| 84 | SEG79 |
| 83 | SEG78 |
| 82 | SEG77 |
| 81 | SEG76 |
| 80 | SEG75 |
| 79 | SEG74 |
| 78 | SEG73 |
| 77 | SEG72 |
| 76 | SEG71 |
| 75 | SEG70 |
| 74 | SEG69 |
| 73 | SEG68 |
| 72 | SEG67 |
| 71 | SEG66 |
| 70 | SEG65 |
| 69 | SEG64 |
| 68 | SEG63 |
| 67 | SEG62 |
| 66 | SEG61 |
| 65 | SEG60 |
| 64 | SEG59 |
| 63 | SEG58 |

CS1=1 CS2=0 RAM26- BIT0
CS1=1 CS2=0 RAM26- BIT1
CS1=1 CS2=0 RAM25- BIT0
CS1=1 CS2=0 RAM25- BIT1

CS1=1 CS2=0 RAM1- BIT0
CS1=1 CS2=0 RAM1- BIT1
CS1=1 CS2=0 RAM0- BIT0
CS1=1 CS2=0 RAM0- BIT1
CS1=0 CS2=1 RAM31- BIT0
CS1=0 CS2=1 RAM31- BIT1
CS1=0 CS2=1 RAM30- BIT0
CS1=0 CS2=1 RAM30- BIT1
CS1=0 CS2=1 RAM29- BIT0
CS1=0 CS2=1 RAM29- BIT1

| Mode | CS1 | CS2 |
| --- | --- | --- |
| Command Mode | 0 | X |
| Write data (1 page) | 0 | 0 |
| Write data (1 page) | 0 | 1 |
| Write data (2 page) | 1 | 0 |
| Pages 1.2 cannot be read simultaneously | It cannot be 0 simultaneously | |
| Read Data (1 page) | 0 | 1 |
| Read Data (2 page) | 1 | 0 |

# 10 Electrical Characteristics

## 10.1 Absolute Maximum Ratings

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | VDD | -0.3～5.5 | V |
| Input voltage | VIN | $V_{SS}$-0.3～$V_{DD}$+0.3 | V |
| Storage temperature | $T_{STG}$ | -50～+125 | ℃ |
| Operating Temperature | $T_{OTG}$ | -40～+85 | ℃ |

## 10.2 DC Electrical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | |
|---|---|---|---|---|---|---|---|
| | | | | | | VDD | Conditions |
| Operating voltage | VDD | 2.4 | — | 5.2 | V | — | — |
| Operating current | $I_{DD1}$ | — | 150 | 300 | μA | 3V | No load/LCD ON On-chip RC oscillator |
| | | — | 300 | 600 | | 5V | |
| Standby Current | $I_{STB}$ | — | 0.1 | 5 | μA | 3V | No load, Power down mode |
| | | — | 0.3 | 10 | | 5V | |
| Low-level Input | $V_{IL}$ | 0 | — | 0.6 | V | 3V | DATA,/WR, /CS1,/CS2 |
| | | 0 | — | 1.0 | | 5V | |
| High-level Input | $V_{IH}$ | 2.4 | — | 3.0 | V | 3V | DATA,/WR, /CS1,/CS2 |
| | | 4.0 | — | 5.0 | | 5V | |
| DATA | $I_{OL}$ | 0.5 | 1.2 | — | mA | 3V | VOL=0.3V |
| | | 1.3 | 2.6 | — | | 5V | VOL=0.5V |
| DATA | $I_{OH}$ | -0.4 | -0.8 | — | mA | 3V | VOL=2.7V |
| | | -0.9 | -1.8 | — | | 5V | VOL=4.5V |
| LCD COM Sink Current | $I_{OL1}$ | 80 | 150 | — | μA | 3V | VOL=0.3V |
| | | 150 | 250 | — | | 5V | VOL=0.5V |
| LCD COM Source Current | $I_{OH1}$ | -80 | -120 | — | μA | 3V | VOH=2.7V |
| | | -120 | -200 | — | | 5V | VOH=4.5V |
| LCD SEG Sink Current | $I_{OL2}$ | 60 | 120 | — | μA | 3V | VOL=0.3V |
| | | -120 | 200 | — | | 5V | VOL=0.5V |
| LCD SEG Source Current | $I_{OH2}$ | -40 | -70 | — | μA | 3V | VOH=2.7V |
| | | -70 | -100 | — | | 5V | VOH=4.5V |
| Pull-UP Resistor RUP | $R_{PH}$ | 40 | 80 | 150 | KΩ | 3V | DATA,/WR, /CS1,/CS2 |
| | | 30 | 60 | 100 | | 5V | |

## 10.3 AC Electrical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | |
|---|---|---|---|---|---|---|---|
| | | | | | | VDD | Conditions |
| System Clock | $f_{SYS1}$ | 192 | 256 | 320 | kHz | 3V | On-chip RC oscillator |
| | | — | 256 | — | | 5V | |
| LCD Clock | $f_{LCD1}$ | — | $f_{SYS1}/1024$ | — | Hz | — | On-chip RC oscillator |
| LCD Common Period | $t_{COM}$ | — | $n/f_{LCD}$ | — | sec | — | N：Number of COM |
| Serial Data Clock （/WR，/RD ） | $F_{CLK1}$ | — | — | 150 | kHz | 3V | Duty cycle 50% |
| | | — | — | 300 | | 5V | |
| Serial Interface Reset PW | $t_{CS}$ | — | 250 | — | ns | — | /CS1,/CS2 |
| /WR，/RD Input pulse width | $t_{CLK}$ | 3.34 | — | — | μA | 3V | Write mode |
| | | 1.67 | — | — | μA | 5V | Write mode |
| Rise/fall time serial data time width | $t_r$，$t_f$ | — | 120 | — | ns | 3V | — |
| | | | | | | 5V | |
| Setup Time for DATA to /WR,/RD Clock Width | $t_{su}$ | — | 120 | — | ns | 3V | — |
| | | | | | | 5V | |
| Hold Time for DATA to /WR,/RD Clock Width | $t_h$ | — | 120 | — | ns | 3V | — |
| | | | | | | 5V | |
| Setup Time for /CS to /WR,/RD Clock Width | $t_{su1}$ | — | 100 | — | ns | 3V | — |
| | | | | | | 5V | |
| Hold Time for /CS to /WR,/RD Clock Width | $t_{h1}$ | — | 100 | — | ns | 3V | — |
| | | | | | | 5V | |

# 11 Package Information

## 11.1 LQFP128(14.0mm×14.0mm PP=0.4mm)



DETALL:F

BASE METAL    WITH PLATING

SECTION B-B
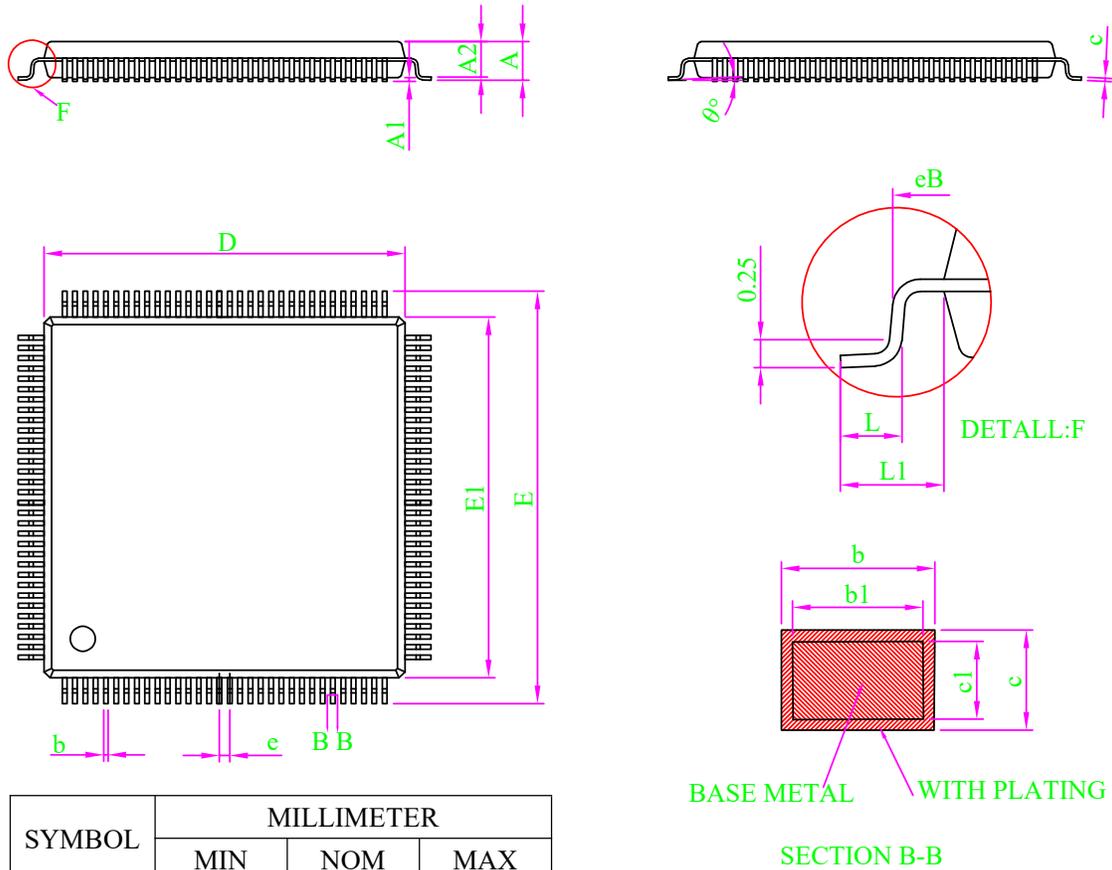
| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | - | - | 1.70 |
| A1 | 0.10 | 0.15 | 0.20 |
| A2 | 1.30 | 1.40 | 1.50 |
| b | 0.14 | - | 0.22 |
| b1 | 0.13 | 0.16 | 0.19 |
| c | 0.13 | - | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 13.90 | 14.00 | 14.10 |
| E | 15.80 | 16.00 | 16.20 |
| E1 | 13.90 | 14.00 | 14.10 |
| eB | 15.05 | - | 15.40 |
| e | 0.40 BSC | | |
| L | 0.42 | 0.57 | 0.72 |
| L1 | 0.95 | 1.00 | 1.15 |
| θ | 0 | - | 10° |

Note：

1. All dimension are in mm.

2. Dim D&El does not include plastic flash；
   Flash:Plastic residual around body edge after
   de junk/singulation.

3. Dim b does not include dambar protrusion/
   intrusion.

4. Plating thickness 0.007mm-0.015mm

## 12 Disclaimer

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## 13   Revision History

| No. | Version | Date | Modify the content | Check |
|-----|---------|------|--------------------|-------|
| 1 | 1.0 | 2018-08-10 | Initial release | YES |
| 2 | 1.1 | 2018-10-11 | Add reference circuit | YES |
| 3 | 1.2 | 2019-03-21 | Alignment correction | YES |
| 4 | 1.3 | 2025-09-02 | Change Description | YES |

[1] Please refer to the latest version of this document before starting or finalizing any design.

[2] Since the release of this document, the status or availability of this product may have changed. For the most up-to-date information, please visit: https://www.szvinka.com/