



VKS114 Datasheet

58×1/57×2/56×3/55×4

LCD DRIVER

Rev.1.1

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1 General Description

The VKS144 is a dot-matrix memory-mapped LCD driver that supports LCD screens with a maximum of 58 points (58SEG \times 1COM)/114 points (57SEG \times 2COM)/168 points (56SEG \times 3COM)/216 points (55SEG \times 4COM). The single-chip microcomputer can be configured with display parameters and read and write display data through the I2C interface, and can also enter power-saving mode through instructions. Its high anti-interference and low power consumption features make it suitable for water, electricity and gas meters as well as industrial control instrument products.

2 Key Features

- Operating voltage:2.4-5.5V
- Built-in RC oscillator (default)
- Selectable LCD bias:1/1、 1/2、 1/3、 1/4
- Selectable LCD duty:1/1、 1/2、 1/3、 1/4
- Built-in 55 \times 4-bit display RAM
- The frame rate can be configured as 80Hz or 160Hz
- Power-down mode via software command(LCD OFF, SYS DIS)
- I2C communication interface
- Display mode $58 \times 1/57 \times 2/56 \times 3/55 \times 4$
- Three display overall flicker frequencies
- Software-configurable of LCD parameters
- Auto-increment addressing for sequential read/write
- VLCD pin provides the LCD driving voltage source(2.4-5.5V)
- It is equipped with a built-in 16-stage LCD driver voltage adjustment circuit
- Built-in power-on reset circuit (POR)
- Low power consumption and high anti-interference
- Available Packages:
 - LQFP64(7.0mm \times 7.0mm PP=0.4mm)
 - DICE
 - COG

3 Product Selection

Part No.	SEG/COM	Bias	Duty	Packaging
VKS114	58×1/57×2/56×3/55×4	1/1, 1/2,1/3 1/4	1/1, 1/2,1/3 1/4	LQFP64
VKS118	118×1	1/1	1/1	LQFP128
VKS146	74×1/73×2/72×3/71×4	1/1, 1/2,1/3 1/4	1/1, 1/2,1/3 1/4	LQFP80
VKS232	116×1/116×2	1/1, 1/2	1/1, 1/2	LQFP128

4 Ordering Information

Part No.	Packaging	Tube Qty	Tray(reel)Qty	Box Qty	Total Qty	Notes
VKS114	LQFP64	-	250/tray	2500/box	15000 PCS	
VKS118	LQFP128	-	90/tray	900/box	5400 PCS	
VKS146	LQFP80	-	90/tray	900/box	54000 PCS	
VKS232	LQFP128	-	90/tray	900/box	5400 PCS	

When VLCD pad and VCCA2 pad are bound together, $VLCD \leq +5.5V$ (VLCD can be connected to an external voltage source to achieve $VLCD \geq VDD$)

Built-in voltage setting (IVA) command		VLCD	SEG71	Note
DE	VE			
0	0	Input	Null	• VLCD supports internal bias voltage
0	1	Input	Null	• The internal voltage is adjusted to Null • VLCD supports internal bias voltage
1	0	Input	Output	• VLCD supports internal bias voltage
1	1	Input	Output	• VLCD supports internal bias voltage

When VDD pad and VCCA2 pad are bound together, $VLCD \leq VDD$

Built-in voltage setting (IVA) command		VLCD	SEG71	Note
DE	VE			
0	0	Input	Null	• VLCD supports internal bias voltage
0	1	Output	Null	• Detect the internal bias voltage *1 • VDD supports internal bias voltage
1	0	NC	Output	• VDD supports internal bias voltage
1	1	NC	Output	• VDD supports internal bias voltage

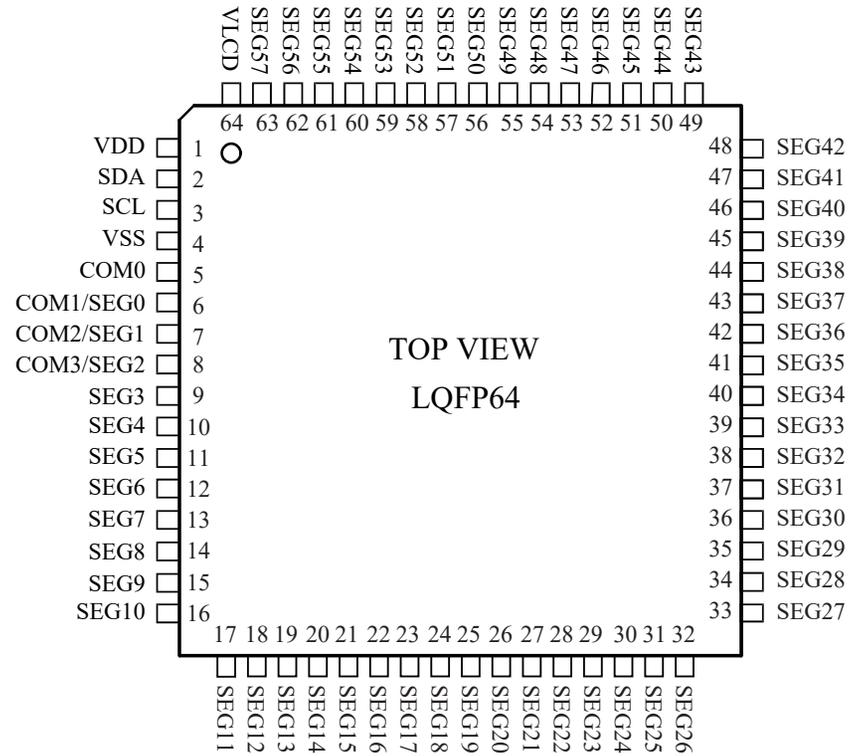
5.2 COB/PAD Coordina

No.	PAD NAME	PAD SIZE (um ²)	X (Center)um	Y (Center)um	NOTE
1	VDD	70*70	93.36	1990.42	
2	SDA	70*70	93.36	1905.92	
3	SCL	70*70	93.36	1807.42	
4	VSS	70*70	93.36	1722.92	
5	COM0	70*70	93.36	1638.42	
6	COM1_SEG0	70*70	93.36	1543.92	
7	COM2_SEG1	70*70	93.36	1459.42	
8	COM3_SEG2	70*70	93.36	1374.92	
9	SEG3	70*70	93.36	1290.42	
10	SEG4	70*70	93.36	1205.92	
11	SEG5	70*70	93.36	1121.42	
12	SEG6	70*70	93.36	1036.92	
13	SEG7	70*70	93.36	952.42	

14	SEG8	70*70	93.36	867.92	
15	SEG9	70*70	93.36	783.42	
16	SEG10	70*70	93.36	698.92	
17	SEG11	70*70	93.36	614.42	
18	SEG12	70*70	93.36	529.92	
19	SEG13	70*70	93.36	445.42	
20	SEG14	70*70	93.36	360.92	
21	SEG15	70*70	93.36	276.42	
22	SEG16	70*70	93.36	191.92	
23	SEG17	70*70	93.36	107.42	
24	SEG18	70*70	368.04	93.36	
25	SEG19	70*70	452.54	93.36	
26	SEG20	70*70	537.04	93.36	
27	SEG21	70*70	621.54	93.36	
28	SEG22	70*70	706.04	93.36	
29	SEG23	70*70	790.54	93.36	
30	SEG24	70*70	875.04	93.36	
31	SEG25	70*70	959.54	93.36	
32	SEG26	70*70	1044.04	93.36	
33	SEG27	70*70	1128.54	93.36	
34	SEG28	70*70	1213.04	93.36	
35	SEG29	70*70	1297.54	93.36	
36	SEG30	70*70	1382.04	93.36	
37	SEG31	70*70	1466.54	93.36	
38	SEG32	70*70	1551.04	93.36	
39	SEG33	70*70	1635.54	93.36	
40	SEG34	70*70	1906.64	107.42	
41	SEG35	70*70	1906.64	191.92	
42	SEG36	70*70	1906.64	276.42	
43	SEG37	70*70	1906.64	360.92	
44	SEG38	70*70	1906.64	445.42	
45	SEG39	70*70	1906.64	529.92	
46	SEG40	70*70	1906.64	614.42	
47	SEG41	70*70	1906.64	698.92	
48	SEG42	70*70	1906.64	783.42	

49	SEG43	70*70	1906.64	867.92	
50	SEG44	70*70	1906.64	952.42	
51	SEG45	70*70	1906.64	1036.92	
52	SEG46	70*70	1906.64	1121.42	
53	SEG47	70*70	1906.64	1205.92	
54	SEG48	70*70	1906.64	1290.42	
55	SEG49	70*70	1906.64	1374.92	
56	SEG50	70*70	1906.64	1459.42	
57	SEG51	70*70	1906.64	1543.92	
58	SEG52	70*70	1906.64	1628.42	
59	SEG53	70*70	1906.64	1712.92	
60	SEG54	70*70	1906.64	1797.42	
61	SEG55	70*70	1906.64	1881.92	
62	SEG56	70*70	1906.64	1966.42	
63	SEG57	70*70	1757.54	2206.64	
64	SEG58	70*70	1673.04	2206.64	
65	SEG59	70*70	1588.54	2206.64	
66	SEG60	70*70	1504.04	2206.64	
67	SEG61	70*70	1419.54	2206.64	
68	SEG62	70*70	1335.04	2206.64	
69	SEG63	70*70	1250.54	2206.64	
70	SEG64	70*70	1166.04	2206.64	
71	SEG65	70*70	1081.54	2206.64	
72	SEG66	70*70	997.04	2206.64	
73	SEG67	70*70	912.54	2206.64	
74	SEG68	70*70	828.04	2206.64	
75	SEG69	70*70	743.54	2206.64	
76	SEG70	70*70	659.04	2206.64	
77	SEG71	70*70	574.54	2206.64	
78	SEG72	70*70	490.04	2206.64	
79	SEG73	70*70	393.04	2206.64	
80	SEG74	70*70	303.04	2206.64	
81	VLCD	70*70	210.43	2206.64	
82	VCCA2	70*70	125.93	2206.64	
83	TEST	70*70	464.01	1521.21	test pad

6 Package Pinout Information(LQFP64)



说明：VCCA2 pad 内部与VLCD pad 连接

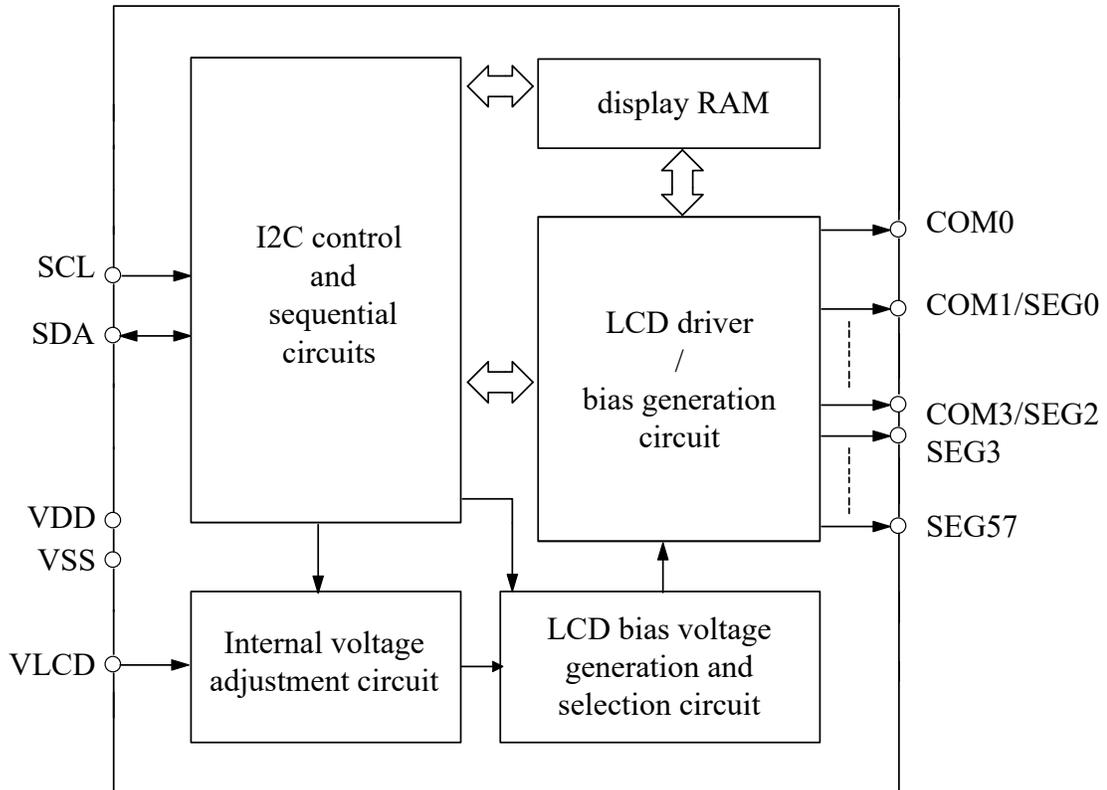
For more information: [Page 24](#)

6.1 VKS114/LQFP64 Pin Description

No.	Name	I/O	Function
1	VDD	VDD	Positive power supply
2	SDA	I/O	Serial Data Input/Output for I2C interface
3	SCL	I	Serial Clock Input for I2C interface
4	VSS	VSS	Negative power supply
5	COM0	O	LCD COM drive outputs
6-8	COM1/SEG0- COM3/SEG2	O	LCD COM/SEG drive outputs, software configuration: 1COM or 2/3/4COM
9-63	SEG3-SEG57	O	LCD SEG drive outputs
64	VLCD	I	When the VLCD pin and VDD pin are short-circuited and the internal voltage regulation function is enabled, the drive voltage is regulated by the internal voltage regulation function. When the VLCD pin is connected in series with the VDD pin and the internal voltage adjustment function is disabled, the LCD driving voltage is set by the series resistor.

7 Functional Description

7.1 Block Diagram



7.2 Display RAM

The static display memory (RAM) structure is 55×4 bits (58×1 bits for 1COM, 57×2 bits for 2COM, and 56×3 bits for 3COM), storing the displayed data. The content of the RAM is directly mapped to the display content of the LCD driver. Access the data in the display RAM via I2C commands.

The following is a mapping from the RAM to the LCD pattern:

1COM Output				COM0	1COM Output				COM0	Addr
2COM Output			COM1	COM0	2COM Output			COM1	COM0	Addr
3COM Output		COM2	COM1	COM0	3COM Output		COM2	COM1	COM0	Addr
4COM Output	COM3	COM2	COM1	COM0	4COM Output	COM3	COM2	COM1	COM0	Addr
SEG1					SEG0					00H
SEG3					SEG2					01H
SEG5					SEG4					02H
SEG7					SEG6					03H
SEG9					SEG8					04H
SEG11					SEG10					05H
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
					SEG74					25H
	D7	D6	D5	D4		D3	D2	D1	D0	Data

RAM Mapping of 55×4

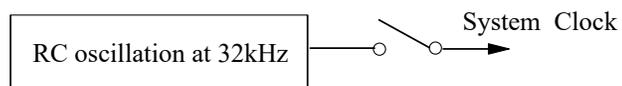
7.3 System Oscillator

The clock of VKS114 is used to generate LCD drive signals and internal logic timing. The system clock is derived from the internal RC oscillator (32kHz), and the system clock frequency (f_{SYS}) determines the LCD frame frequency.

The system setting command can start or stop the system oscillator. After the display shows off and the system oscillator stops, the system enters the power-saving mode.

When the system is powered on and working, the system oscillator is in a stopped state.

The Settings of the system oscillation are shown in the following figure:



7.4 LCD operating voltage

The LCD driver voltage can be obtained through the VLCD pin or selected as a 16-level voltage through the internal configuration.

When the VLCD pad is connected to the VCCA2 pad, the LCD driving voltage can be supplied from an external voltage source ($VLCD \leq 5.5V$), and VLCD may be higher than VDD.

When the VDD pad is connected to the VCCA2 pad, the LCD driving voltage can be obtained by connecting the VLCD pin to VDD through a series resistor ($VLCD \leq VDD$).

The internal 16-level voltage is set through a 4-bit programmable analog switch, as shown in the following table: When VCCA2 pad is connected to VDD pad

Bias DA3~DA0	1/1	1/2	1/3	1/4	1/5	Note
00H	1.000	1.000	1.000	1.000	1.000	Default
01H	0.849	0.918	0.944	0.957	0.966	
02H	0.738	0.849	0.894	0.918	0.934	
03H	0.652	0.789	0.849	0.882	0.904	
04H	0.584	0.738	0.808	0.849	0.875	
05H	0.529	0.692	0.771	0.818	0.849	
06H	0.484	0.652	0.738	0.789	0.824	
07H	0.446	0.616	0.707	0.763	0.801	
08H	0.413	0.584	0.678	0.738	0.779	
09H	0.385	0.556	0.652	0.714	0.758	
0AH	0.360	0.529	0.628	0.692	0.738	
0BH	0.338	0.506	0.605	0.672	0.719	
0CH	0.319	0.484	0.584	0.652	0.701	
0DH	0.302	0.464	0.565	0.634	0.684	
0EH	0.287	0.446	0.547	0.616	0.668	
0FH	0.273	0.429	0.529	0.600	0.652	

When the VCCA2 pad is connected to the VLCD pad

DA3~DA0 \ Bias	1/1	1/2	1/3	1/4	1/5
0x00(Default)	1.000×VLCD	1.000×VLCD	1.000×VLCD	1.000×VLCD	1.000×VLCD
0x01	0.849×VLCD	0.918×VLCD	0.944×VLCD	0.957×VLCD	0.966×VLCD
0x02	0.738×VLCD	0.849×VLCD	0.894×VLCD	0.918×VLCD	0.934×VLCD
0x03	0.652×VLCD	0.789×VLCD	0.849×VLCD	0.882×VLCD	0.904×VLCD
0x04	0.584×VLCD	0.738×VLCD	0.808×VLCD	0.849×VLCD	0.875×VLCD
0x05	0.529×VLCD	0.692×VLCD	0.771×VLCD	0.818×VLCD	0.849×VLCD
0x06	0.484×VLCD	0.652×VLCD	0.738×VLCD	0.789×VLCD	0.824×VLCD
0x07	0.446×VLCD	0.616×VLCD	0.707×VLCD	0.763×VLCD	0.801×VLCD
0x08	0.413×VLCD	0.584×VLCD	0.678×VLCD	0.738×VLCD	0.779×VLCD
0x09	0.385×VLCD	0.556×VLCD	0.652×VLCD	0.714×VLCD	0.758×VLCD
0x0A	0.360×VLCD	0.529×VLCD	0.628×VLCD	0.692×VLCD	0.738×VLCD
0x0B	0.338×VLCD	0.506×VLCD	0.605×VLCD	0.672×VLCD	0.719×VLCD
0x0C	0.319×VLCD	0.484×VLCD	0.584×VLCD	0.652×VLCD	0.701×VLCD
0x0D	0.302×VLCD	0.464×VLCD	0.565×VLCD	0.634×VLCD	0.684×VLCD
0x0E	0.287×VLCD	0.446×VLCD	0.547×VLCD	0.616×VLCD	0.668×VLCD
0x0F	0.273×VLCD	0.429×VLCD	0.529×VLCD	0.600×VLCD	0.652×VLCD

7.5 Power-On Reset

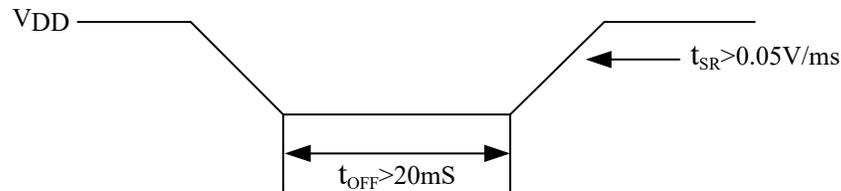
During the initialization of the power-on reset circuit(1ms),no I2C data transmission should occur.

The state of the internal circuit after initialization is as follows:

- When $V_{LCD} \leq V_{DD}$, all COM/SEG pins output VDD.
- When $V_{DD} \leq V_{LCD}$, all COM/SEG pins output VLCD.
- Configure 1/4 duty and 1/3 bias.
- The system oscillator and LCD bias generator are turned off.
- The LCD display is off.
- The internal voltage adjustment function is enabled.
- Set the shared pin of SEG/VLCD as the SEG pin.
- The VLCD pin detection function is prohibited.
- The frame rate is configured to 80Hz by default.
- Flashing function prohibited.

If,during operation, VDD falls below the specified minimum operating voltage, the power-on reset timing requirements must be met, that is, the VDD voltage must drop to 0V and remain at 0V for at least 20ms before rising to the normal operating voltage

Power-on Reset Timing:



7.6 LCD Communication Command

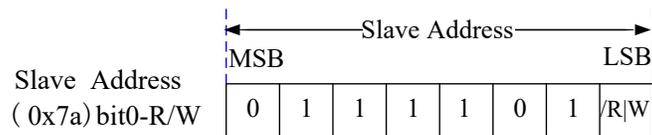
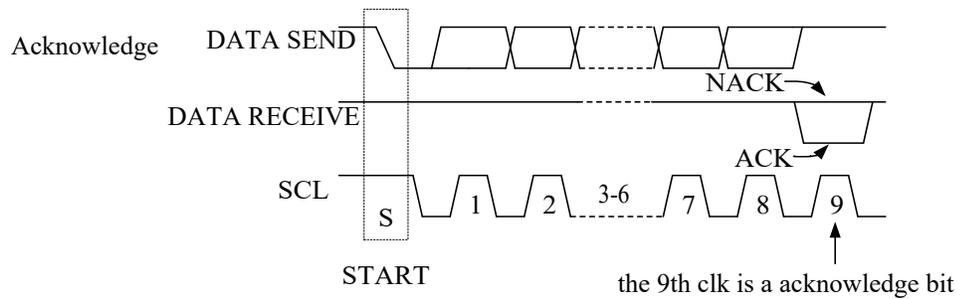
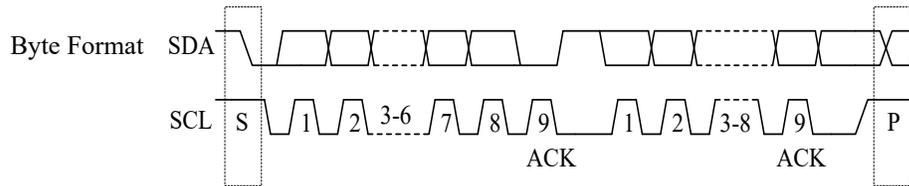
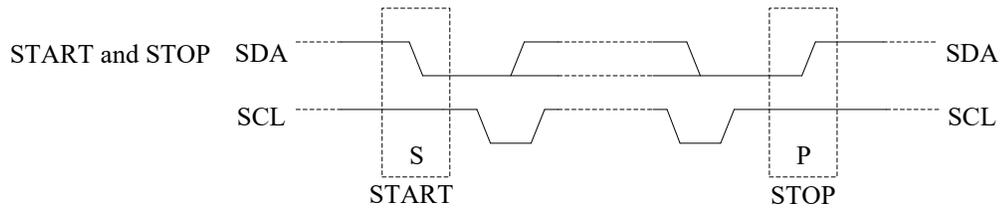
The LCD driver supports 58SEG×1COM、 57SEG×2COM、 56SEG×3COM、 55SEG×4COM modes, any unused SEG and COM pins should be left floating(NC).

Two frame frequencies are provided, and you can choose to set them to 80Hz or 160Hz through the frame frequency setting command.

8 I2C Serial Interface

The VKS114 features two communication pins compliant with the I2C protocol. open-drain outputs require external pull-up resistors.

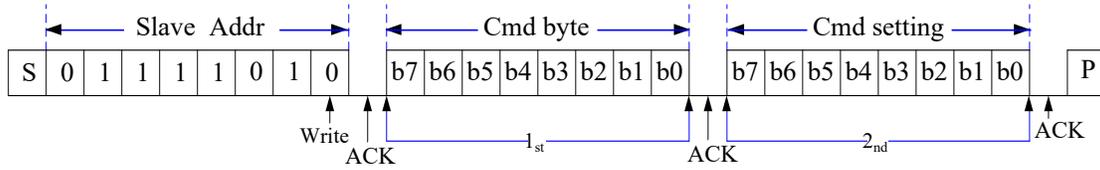
The SCL pin is the clock input pin, and the SDA pin is the serial data input/output pin. When the I2C bus is idle, both pins remain at a logic high level.



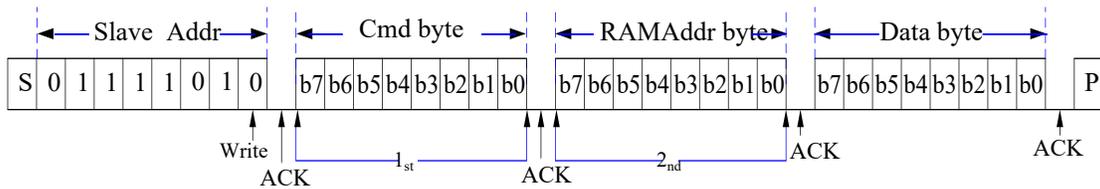
9 I2C Command Format

Write operation

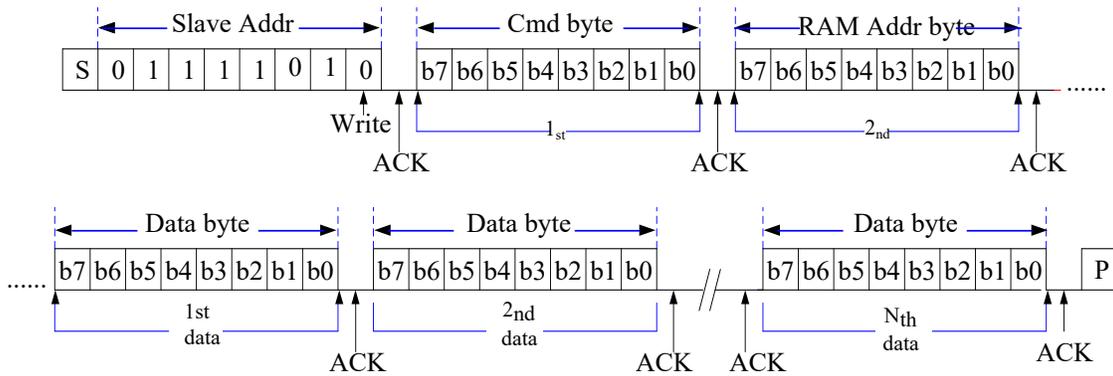
Write commands



Write a single byte to the display RAM

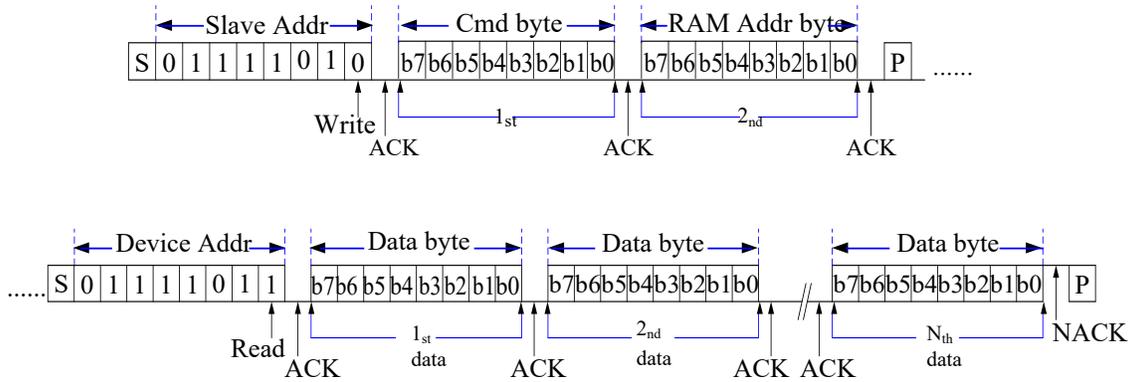


Write multiple bytes to the display RAM

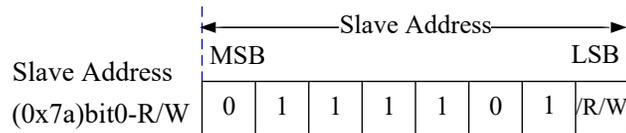


Read operation

Read multiple bytes from the display RAM



10 Command Summary



10.1 Display Data Command

Send display data to display RAM

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
Display data command	1st	1	0	0	0	0	0	0	0		W	
Address pointer	2nd	X	A6	A5	A4	A3	A2	A1	A0	Display data start address	W	00H

10.2 Mode Set Command

Set BIAS and DUTY

Function	Byte	(MSB)Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB)Bit0
Driver mode setting command	1st	1	0	0	0	0	0	1	0
Duty and Bias	2nd	X	X	Duty2	X	Duty1	Bias1	Duty0	Bias0

Bit 5	Bit 3	Bit 1	Duty
Duty2	Duty1	Duty0	
0	0	0	1/4 duty
1	0	0	1/1 duty
1	0	1	1/2 duty
1	1	0	1/3 duty

Bit 2	Bit0	Bias
Bias1	Bias0	
0	0	1/3 bias
0	1	1/4 bias
1	1	1/2 bias

10.3 System Settings Command

Enable/disable the internal system oscillator and LCD display

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
System Settings Command	1st	1	0	0	0	0	1	0	0		W	
System oscillator and Display the on/off Settings	2nd	X	X	X	X	X	X	S	E		W	00H

Bit 1	Bit 0	Internal system oscillator	LCD display
S	E		
0	X	off	off
1	0	on	off
1	1	on	on

10.4 Frame rate setting command

Select the frame frequency

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
Frame frequency command	1st	1	0	0	0	0	1	1	0		W	
Frame frequency setting	2nd	X	X	X	X	X	X	X	F		W	00H

Bit 0	Frame frequency
F	
0	80Hz
1	160Hz

10.5 Blinking Frequency Command

Set the blinking frequency

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
Blinking frequency command	1st	1	0	0	0	1	0	0	0		W	
Blinking frequency setting	2nd	X	X	X	X	X	X	BK1	BK0		W	00H

Bit 1	Bit 0	blinking freq
BK1	BK0	
0	0	blinking off(Def)
0	1	2Hz
1	0	1Hz
1	1	0.5Hz

10.6 Internal Voltage Adjustment(IVA) Command

The IVA command allows selection of 16 voltage levels to adjust the LCD driver voltage

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
IVA Com	1 st	1	0	0	0	1	0	1	0		W	
IVA set	2 nd	X	X	DE	VE	DA3	DA2	DA1	DA0	The SEG/VLCD pin function is set through the DE bit. The VE bit enables or disables the internal voltage adjustment function. DA3 to DA0 are used to adjust the output voltage of the VLCD.	W	30H

Note:

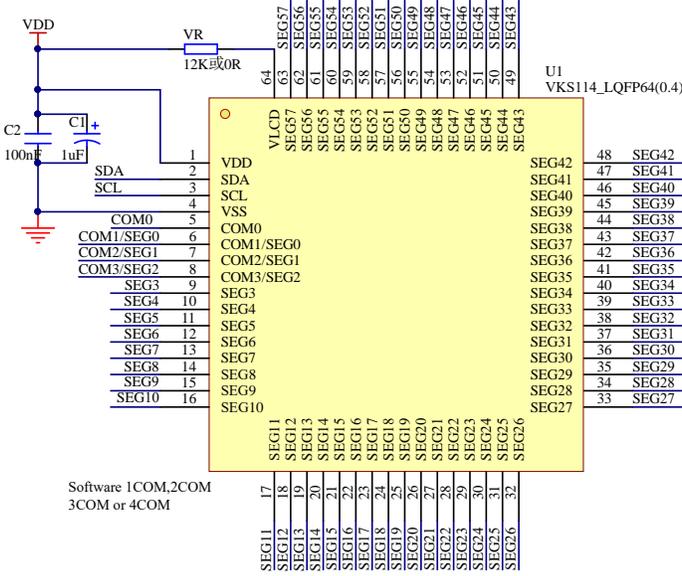
Bit 5 DE	Bit 4 VE	SEG71/VLCD shared pin sel	internal voltage adjustment	Note
0	0	VLCD pin	off	<ul style="list-style-type: none"> VCCA2→VLCD: bias voltage is provided by VLCD pin VCCA2→VDD: bias voltage is provided by VLCD pin. Note:VLCD→VDD: disable the internal voltage follower by setting DA3- DA0 to "0000".
0	1	VLCD pin	on	<ul style="list-style-type: none"> VCCA2→VLCD: Internal voltage adjustment disabled. (bias voltage is provided by VLCD pin) VCCA2→VDD: bias voltage is provided by VLCD pin, Internal adjustment disabled. (Not recommended.) VCCA2→VDD: VLCD floating, Internal adjustment enabled. (internal regulation adjusts bias)
1	0	SEG71 pin/COB	off	<ul style="list-style-type: none"> VCCA2→VLCD: bias voltage is provided by VLCD pin VCCA2→VDD: bias voltage is provided by VDD pin. Note: Internal voltage follower is automatically disabled, ignore DA3 to DA0 bits.
1	1	SEG71 pin/COB	on	<ul style="list-style-type: none"> VCCA2→VLCD: bias voltage is provided by VLCD, internal regulation adjusts bias. VCCA2→VDD: bias voltage is provided by VDD, internal regulation adjusts bias.

- Power-on status: The internal voltage adjustment function is enabled and the SEG/VLCD pin is selected as the SEG pin.
- When the DA0 to DA3 bits are set to "0000", the internal voltage follower is prohibited.
- When the DA0 to DA3 bits are set to values other than "0000", the internal voltage follower is enabled.

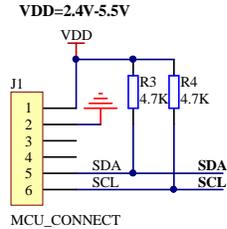
11 Application Circuits

1. The software configuration bias voltage is achieved through the internal voltage adjustment function:
When VLCD and VDD are short-circuited, VR=0R

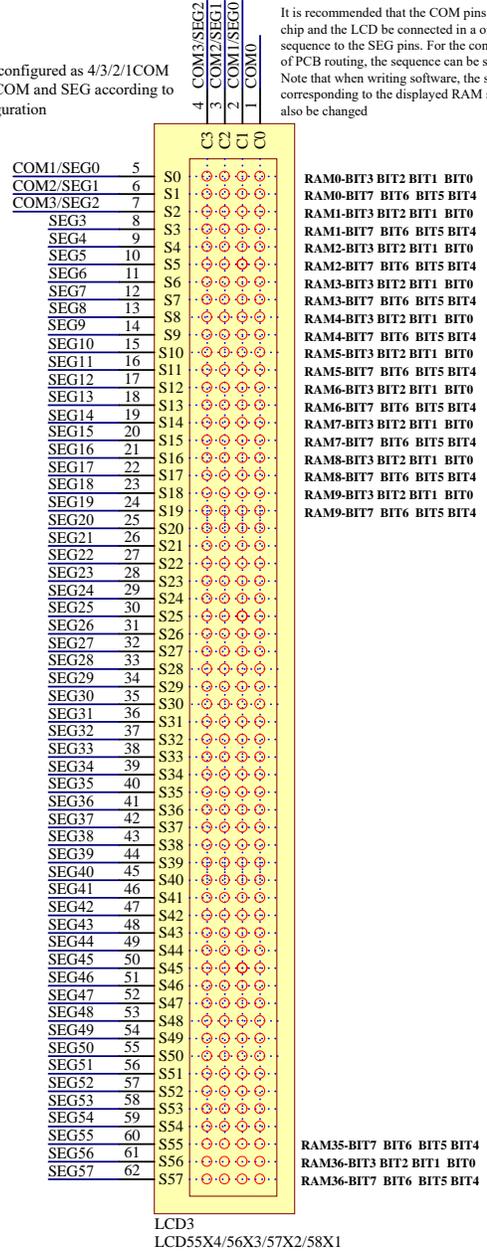
2. When the software configuration bias voltage is provided by the VLCD pin:
(VLCD can be connected to a power supply less than 5.5V through VR, and VLCD can be larger than VDD.
When VLCD is connected to VDD via VR, with VDD=5V and VR=12K:
The VLCD is approximately 4.2V
It is recommended to use a 20K adjustable resistor for VR to achieve the best display effect and take the resistance value at this time.



When the surrounding interference is relatively large, a 10R to 1k resistor and a PF-level small capacitor to ground can be connected in series on the communication pin. When the power supply of the single-chip microcomputer (3.3V) and the driver chip (5V) is inconsistent, it is recommended to add a level conversion circuit on the communication pin



The software is configured as 4/3/2/1COM
Please connect COM and SEG according to the actual configuration



It is recommended that the COM pins of the chip and the LCD be connected in a one-to-one sequence to the SEG pins. For the convenience of PCB routing, the sequence can be shuffled
Note that when writing software, the sequence corresponding to the displayed RAM should also be changed

12 Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3~6.5	V
Input Voltage	VIN	VSS-0.3~VDD+0.3	V
Storage Temperature	TSTG	-50~+125	°C
Operating Temperature	TOTG	-40~+85	°C

12.2 DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	2.4	—	5.5	V	—	—
Operating current	IDD1	—	25	40	μA	3V	No load, VLCD=VDD, 1/3 bias, fLCD=80Hz, LCD off, Internal osc on, DA0~DA3 = "0000"
		—	35	50		5V	
Operating current	IDD2	—	2	5	μA	3V	No load, VLCD=VDD, 1/3 bias, fLCD=80Hz, LCD off, Internal osc on, DA0~DA3 = "0000"
		—	4	10		5V	
Standby Current	ISTB	—	—	1	μA	3V	No load, VLCD=VDD, LCD off, Internal osc off
		—	—	2		5V	
Low-level Input	VIL	0	—	0.3	VDD	3V 5V	SCL, SDA
High-level Input	VIH	0.7	—	1.0	VDD	3V 5V	SCL, SDA
Low Level Output Current	IOL	3.0	—	—	mA	3V	VOL=0.4V, SDA
		6.0	—	—		5V	
LCD COM Sink Current	IOL1	250	400	—	μA	3V	VOL=0.3V
		500	800	—		5V	VOL=0.5V
LCD COM Source Current	IOH1	-140	-230	—	μA	3V	VOH=2.7V
		-300	-500	—		5V	VOH=4.5V
LCD SEG Sink Current	IOL2	250	400	—	μA	3V	VOL=0.3V
		500	800	—		5V	VOL=0.5V
LCD SEG Source Current	IOH2	-140	-230	—	μA	3V	VOH=2.7V
		-300	-500	—		5V	VOH=4.5V

12.3 AC Electrical Characteristics

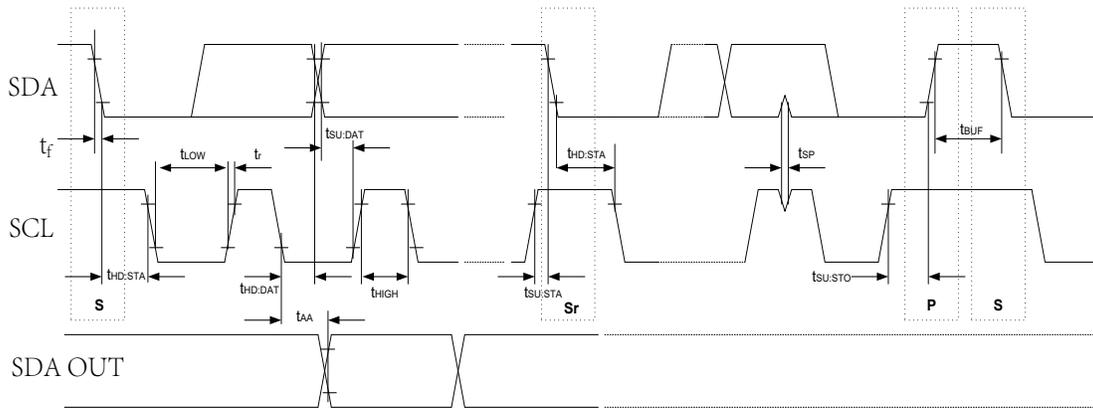
Frame Frequency

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
LCD Frame Frequency	f _{LCD1}	72	80	88	Hz	4.0V	1/4 duty, 25°C
LCD Frame Frequency	f _{LCD2}	144	160	176	Hz	4.0V	1/4 duty, 25°C
LCD Frame Frequency	f _{LCD3}	52	80	124	Hz	4.0V	1/4 duty, -40 ~ +85°C
LCD Frame Frequency	f _{LCD4}	104	160	248	Hz	4.0V	1/4 duty, -40 ~ +85°C

I2C parameter

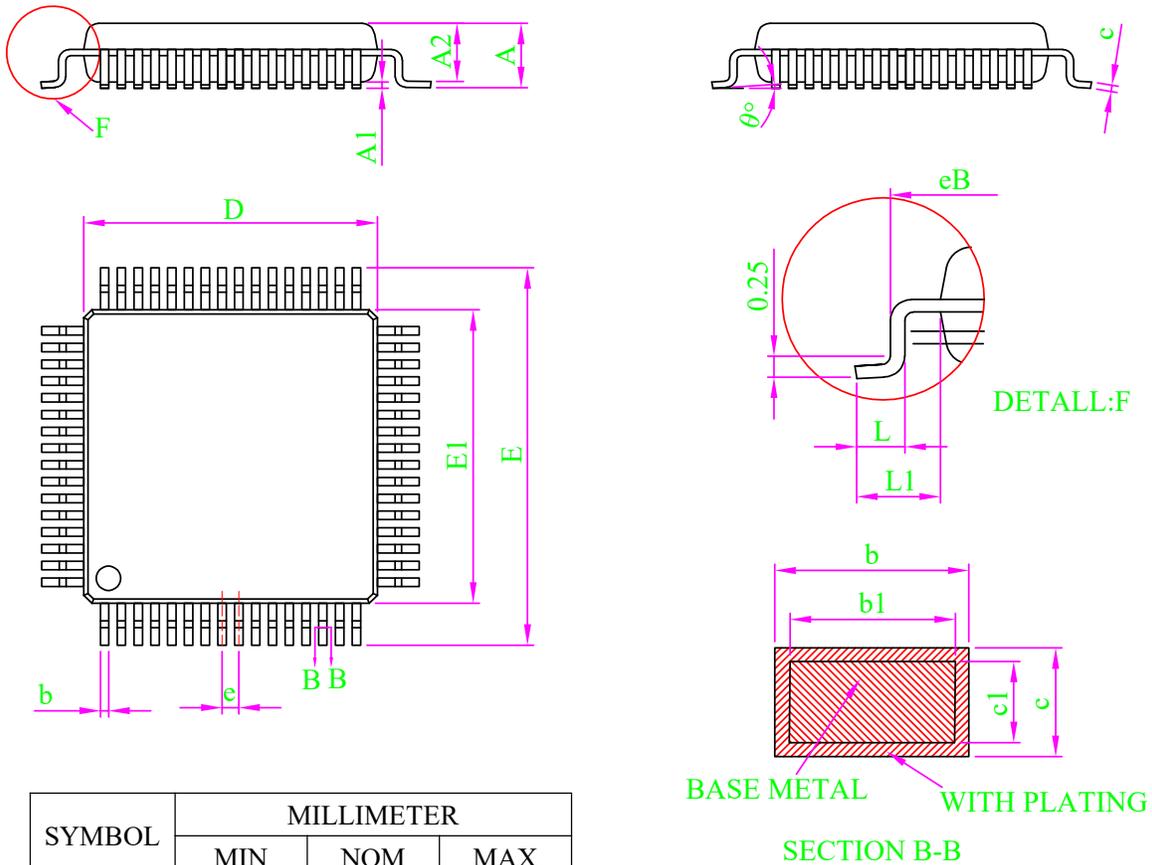
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Clock Frequency	f _{SCL}	—	—	400	kHz	3.0-5.5V	—
Bus Free Time	t _{BUF}	1.3	—	—	μs	3.0-5.5V	Time in which the bus must be free before a new transmission can start
Start Condition Hold Time	t _{HD:STA}	0.6	—	—	μs	3.0-5.5V	After this period, the first clock pulse is generated
SCL Low Time	t _{LOW}	1.3	—	—	μs	3.0-5.5V	—
SCL High Time	t _{HIGH}	0.6	—	—	μs	3.0-5.5V	—
Start Condition Setup Time	t _{SU:STA}	0.6	—	—	μs	3.0-5.5V	Only relevant for repeated START condition
Data Hold Time	t _{HD:DAT}	0	—	—	ns	3.0-5.5V	—
Data Setup Time	t _{SU:DAT}	100	—	—	ns	3.0-5.5V	—
SDA and SCL Rising Time	t _R	—	—	0.3	μs	3.0-5.5V	periodically sampled
SDA and SCL Falling Time	t _F	—	—	0.3	μs	3.0-5.5V	periodically sampled
Stop Condition Setup Time	t _{SU:STO}	0.6	—	—	μs	3.0-5.5V	—
Output Valid from Clock	t _{AA}	—	—	0.9	μs	3.0-5.5V	—
Input Filter Time Constant (SDA and SCL pin)	t _{SP}	—	—	50	ns	3.0-5.5V	Noise suppression time

I²C Timing



13 Package Information

13.1 LQFP64 (7.0mm × 7.0mm PP=0.4mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.70
A1	0.10	0.15	0.20
A2	1.30	1.40	1.50
b	0.16	-	0.24
b1	0.15	0.18	0.21
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.28
e	0.40 BSC		
L	0.42	0.57	0.72
L1	0.95	1.00	1.15
θ	0	-	10°

Note:

1. All dimension are in mm.
2. Dim D&E1 does not include plastic flash;
Flash:Plastic residual around body edge after de junk/singulation.
3. Dim b does not include dambar protrusion/
intrusion.
4. Plating thickness 0.007mm-0.015mm

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15 Revision History

No.	Version	Date	Modify the content	Check
1	1.0	2022-08-10	Initial release	YES
2	1.1	2025-09-02	Change Description	YES

[1] Please refer to the latest version of this document before starting or finalizing any design.

[2] Since the release of this document, the status or availability of this product may have changed. For the most up-to-date information, please visit:

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