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Vinka Microelectronics

VK2C22A Datasheet

44×4 LCD DRIVER

Rev.1.3

1 General Description

The VK2C22A is a dot-matrix memory-mapped LCD driver that supports LCD screens with a maximum of 176 dots (44SEG×4COM). The single-chip microcomputer can be configured with display parameters and read and write display data through the I2C interface, and can also enter power-saving mode through instructions. Its high anti-interference and low power consumption features make it suitable for water, electricity and gas meters as well as various industrial control instruments.

2 Key Features

- Operating voltage：2.4-5.5V
- Built-in RC oscillator (default)
- Selectable LCD bias: 1/2 or 1/3
- Selectable LCD duty: 1/4
- Built-in 44×4-bit display RAM
- The frame rate can be configured as 80Hz or 160Hz
- Power-down mode via software command(LCD OFF, SYS DIS)
- I2C communication interface
- Display mode 44×4
- Three display overall flicker frequencies
- Software-configurable of LCD parameters
- Auto-increment addressing for sequential read/write
- VLCD pin provides the LCD driving voltage source(2.4-5.5V)
- It is equipped with a built-in 16-stage LCD driver voltage adjustment circuit
- Built-in power-on reset circuit (POR)
- Low power consumption and high anti-interference
- Available Packages:
  LQFP52(14.0mm × 14.0mm PP=1.0mm)
  DICE
  COG

3 Product Selection

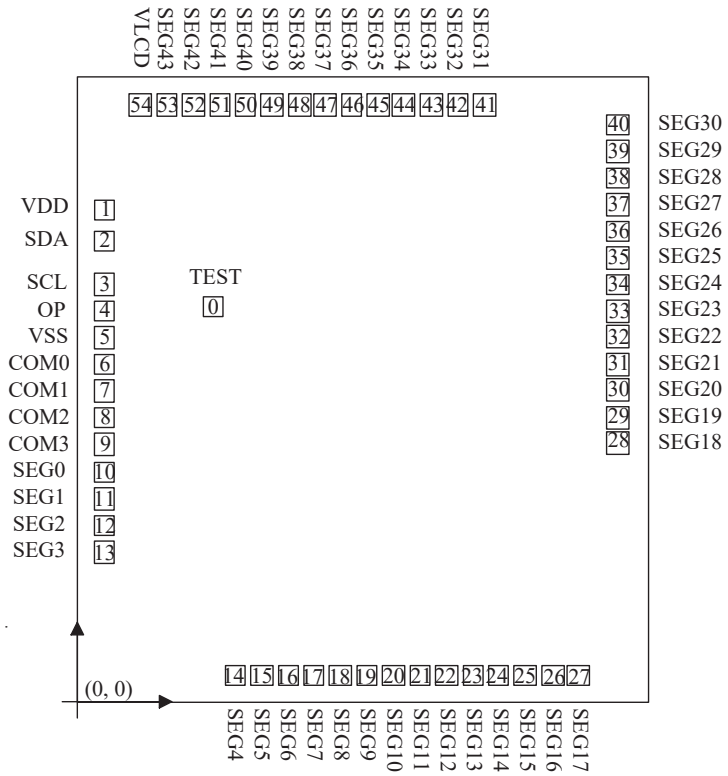
Part No.	SEG×COM	BIAS	DUTY	Packaging
VK2C21A	20×4,16×8	1/3,1/4	1/4,1/8	SOP28
VK2C21AA	20×4,16×8	1/3,1/4	1/4,1/8	SSOP28
VK2C21AQ	20×4,16×8	1/3,1/4	1/4,1/8	QFN28L
VK2C21B	16×4,12×8	1/3,1/4	1/4,1/8	SOP24
VK2C21BA	16×4,12×8	1/3,1/4	1/4,1/8	SSOP24
VK2C21BQ	16×4,12×8	1/3,1/4	1/4,1/8	QFN24L
VK2C21C	12×4,8×8	1/3,1/4	1/4,1/8	SOP20
VK2C21CQ	12×4,8×8	1/3,1/4	1/4,1/8	QFN20L
VK2C21D	8×4,4×8	1/3,1/4	1/4,1/8	SOP16
VK2C21DQ	8×4,4×8	1/3,1/4	1/4,1/8	QFN16L
VK2C22A	44×4	1/2,1/3	1/4	LQFP52
VK2C22B	40×4	1/2,1/3	1/4	LQFP48
VK2C22	44×4	1/2,1/3	1/4	DICE
VK2C23A	55×4,51×8	1/3,1/4	1/4, 1/8	LQFP64
VK2C23B	35×8	1/3,1/4	1/8	LQFP48
VK2C23	56×4,52×8	1/3,1/4	1/4,1/8	DICE
VK2C24A	71×4,67×8,59×16	1/2,1/3,1/4,1/5	1/4,1/8,1/16	LQFP80
VK2C24B	55×4,51×8,43×16	1/2,1/3,1/4,1/5	1/4,1/8,1/16	LQFP64
VK2C24	72×4,68×8,60×16	1/2,1/3,1/4,1/5	1/4,1/8,1/16	DICE

4 Ordering Information

Part No.	Packaging	Tube Qty	Tray(reel)Qty	Box Qty	Total Qty	Notes
VK2C21A	SOP28	26/tube	-	2080/box	20800 PCS	
VK2C21AA	SSOP28	50/tube	-	5000/box	50000 PCS	
VK2C21AQ	QFN28L	-	490/reel	4900/box	29400 PCS	
VK2C21B	SOP24	30/tube	-	2400/box	24000 PCS	
VK2C21BA	SSOP24	50/tube	-	10000/box	100000 PCS	
VK2C21BQ	QFN24L	-	490/reel	4900/box	29400 PCS	
VK2C21C	SOP20	36/tube	-	2880/box	28800 PCS	
VK2C21CQ	QFN20L	-	490/reel	4900/box	29400 PCS	
VK2C21D	SOP16	50/tube	-	10000/box	100000 PCS	
VK2C21DQ	QFN16L	-	3000/reel	3000/box	120000 PCS	
VK2C22A	LQFP52	-	90/tray	900/box	5400 PCS	
VK2C22B	LQFP48	-	250/tray	2500/box	15000 PCS	
VK2C22	DICE	-	400/tray	2000/box	4000 PCS	DICE
VK2C23A	LQFP64	-	250/tray	2500/box	15000 PCS	
VK2C23B	LQFP48	-	250/tray	2500/box	15000 PCS	
VK2C23	DICE	-	250/tray	1000/box	2000 PCS	DICE
VK2C24A	LQFP80	-	90/tray	900/box	5400 PCS	
VK2C24B	LQFP64	-	250/tray	2500/box	15000 PCS	
VK2C24	DICE	-	200/tray	1000/box	2000 PCS	DICE

5 COB Pad Information

5.1 COB Pad Assignment



Chip area: 1645×1610 um^2, substrate potential: VSS

OP pin: Suspended or grounded, PAD size: 80×80 um^2

（VLCD≤VDD）

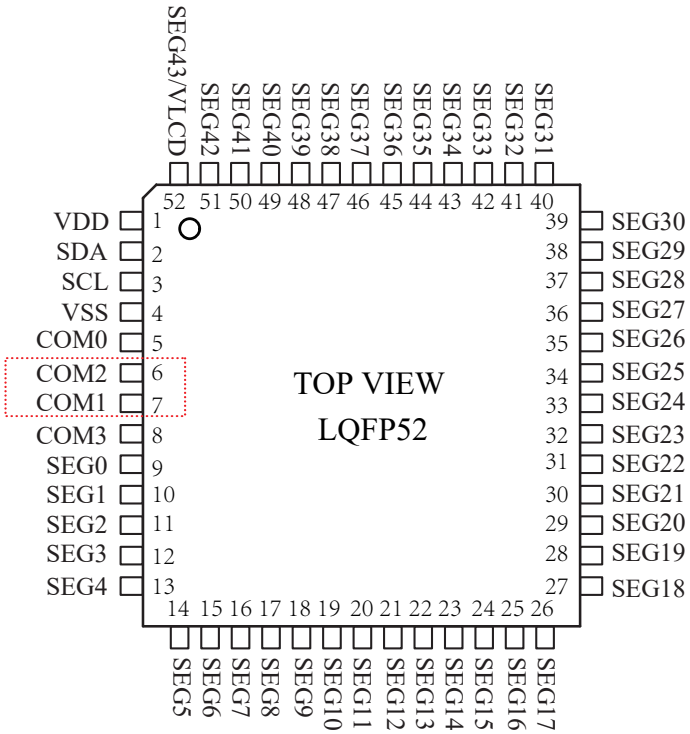
Built-in voltage setting (IVA) command		VLCD	SEG43	Notes
DE	VE			
0	0	Input	Null	• Connect a resistor in series with the VLCD to the VDD to adjust the bias voltage
0	1	Input	Null	• VLCD supports internal bias voltage • VLCD pin output bias voltage 1
1	0	-	-	• The bias voltage is provided by the internal VDD
1	1	-	-	• The bias voltage is provided by the internal adjustment circuit

5.2 COB PAD Coordinates

Unit: um

Pad No	Name	X	Y	Pad No	Name	X	Y
1	VDD	93.11	1158.4	29	SEG19	1551.89	571.86
2	SDA	93.11	1073.9	30	SEG20	1551.89	656.36
3	SCL	93.11	964.42	31	SEG21	1551.89	740.86
4	OP	93.11	879.92	32	SEG22	1551.89	825.36
5	VSS	93.11	795.42	33	SEG23	1551.89	909.86
6	COM0	93.11	710.92	34	SEG24	1551.89	994.36
7	COM1	93.11	626.42	35	SEG25	1551.89	1078.86
8	COM2	93.11	541.92	36	SEG26	1551.89	1163.36
9	COM3	93.11	457.42	37	SEG27	1551.89	1247.86
10	SEG0	93.11	362.42	38	SEG28	1551.89	1332.36
11	SEG1	93.11	277.92	39	SEG29	1551.89	1416.86
12	SEG2	93.11	193.42	40	SEG30	1551.89	1501.36
13	SEG3	93.11	108.92	41	SEG31	1260.87	1516.89
14	SEG4	437.83	93.11	42	SEG32	1176.37	1516.89
15	SEG5	522.33	93.11	43	SEG33	1091.87	1516.89
16	SEG6	606.83	93.11	44	SEG34	1007.37	1516.89
17	SEG7	691.33	93.11	45	SEG35	922.87	1516.89
18	SEG8	775.83	93.11	46	SEG36	838.37	1516.89
19	SEG9	860.33	93.11	47	SEG37	753.87	1516.89
20	SEG10	944.83	93.11	48	SEG38	669.37	1516.89
21	SEG11	1029.33	93.11	49	SEG39	584.87	1516.89
22	SEG12	1113.83	93.11	50	SEG40	500.37	1516.89
23	SEG13	1198.33	93.11	51	SEG41	415.87	1516.89
24	SEG14	1282.83	93.11	52	SEG42	318.87	1516.89
25	SEG15	1367.33	93.11	53	SEG43	228.87	1516.89
26	SEG16	1451.83	93.11	54	VLCD	136.26	1516.89
27	SEG17	1536.33	93.11				
28	SEG18	1551.89	487.36	0	TEST	443.31	1079.73

6 Package Pinout Information(LQFP52)



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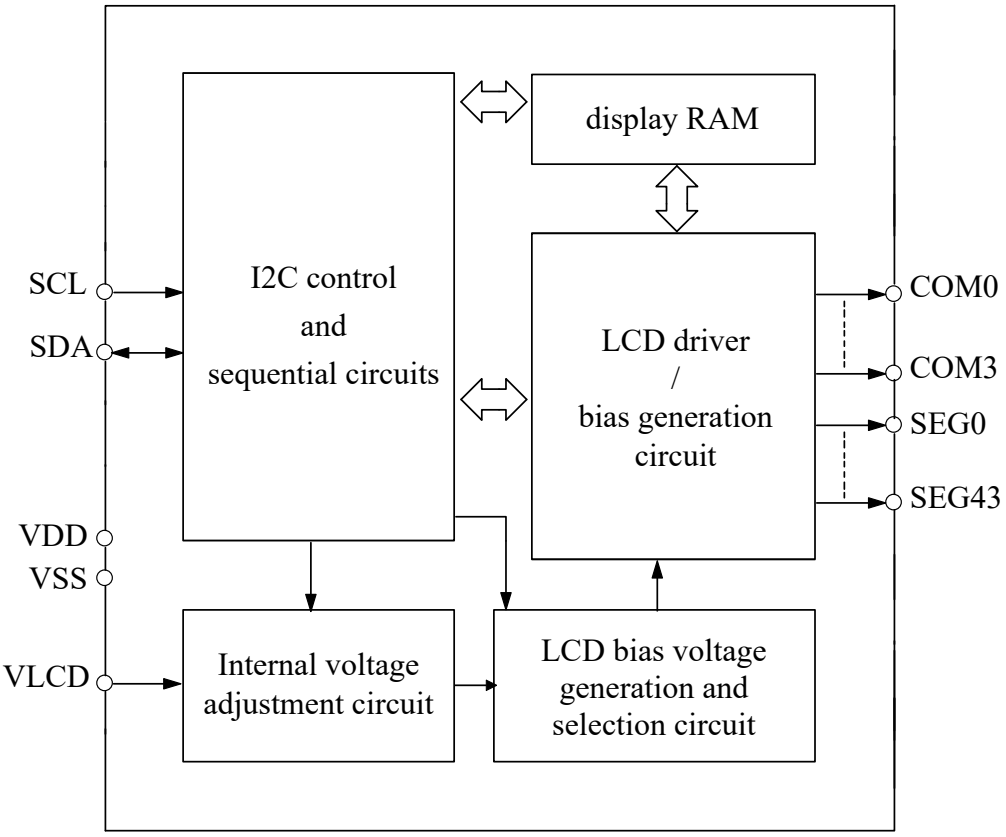
6.1 VK2C22A/LQFP52 Pin Description

No.	Name	I/O	Function
1	VDD	VDD	Positive power supply
2	SDA	I/OO	Serial Data Input/Output for I2C interface
3	SCL	I	Serial Clock Input for I2C interface
4	VSS	VSS	Negative power supply
5-8	COM0-COM3	OO	LCD drive outputs (the COM1 and COM2 pins are notarranged in sequence)
9-51	SEG4-SEG42	O	LCD SEG drive outputs
52	SEG43/VLCD	I/O	When the VLCD pin and VDD pin are short-circuited and the internal voltage regulation function is enabled, the drive voltage is regulated by the internal voltage regulation function. When the VLCD pin is connected in series with the VDD pin and the internal voltage adjustment function is disabled, the LCD driving voltage is set by the series resistor.

7 Functional Description

7.1 Block Diagram



7.2 Display RAM

The display RAM is organized as 44×4 bits (44×4 bits for 4-COM mode), storing the displayed data. The content of the display RAM is directly mapped to the display content of the LCD driver. Display RAM data is accessed via I2C commands.

The following is a mapping from the RAM to the LCD pattern:

Output	COM3	COM2	COM1	COM0	Output	COM3	COM2	COM1	COM0	Address
SEG1					SEG0					0x00
SEG3					SEG2					0x01
SEG5					SEG4					0x02
SEG7					SEG6					0x03
SEG9					SEG8					0x04
SEG11					SEG10					0x05
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
SEG43					SEG42					0x15
Data	bit7	bit6	bit5	bit4		bit3	bit2	bit1	bit0	

RAM Mapping of 44×4

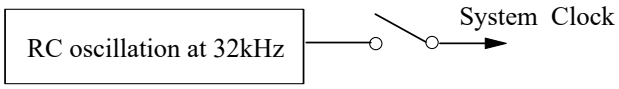
7.3 System Oscillator

The clock of VK2C22A is used to generate LCD drive signals and internal logic timing. The system clock is derived from the internal RC oscillator (32kHz), and the system clock frequency (f_{SYS}) determines the LCD frame frequency.

The system setting command can start or stop the system oscillator. After the display shows off and the system oscillator stops, the system enters the power-saving mode.

When the system is powered on and working, the system oscillator is in a stopped state.

The Settings of the system oscillation are shown in the following figure:



7.4 LCD operating voltage

The LCD drive voltage (VLCD≤VDD) can be obtained through the VLCD pin (by connecting a resistor in series to the VDD pin), or by selecting a 16-level voltage through internal configuration.

The internal 16-level voltage is set through a 4-bit programmable analog switch, as shown in the following table:

Bias / DA3~DA0	1/2	1/3	Note
0x00	1.000×VDD	1.000×VDD	Default
0x01	0.937×VDD	0.957×VDD	
0x02	0.882×VDD	0.918×VDD	
0x03	0.833×VDD	0.882×VDD	
0x04	0.789×VDD	0.849×VDD	
0x05	0.750×VDD	0.818×VDD	
0x06	0.714×VDD	0.789×VDD	
0x07	0.682×VDD	0.763×VDD	
0x08	0.652×VDD	0.738×VDD	
0x09	0.625×VDD	0.714×VDD	
0x0A	0.600×VDD	0.692×VDD	
0x0B	0.577×VDD	0.672×VDD	
0x0C	0.556×VDD	0.652×VDD	
0x0D	0.536×VDD	0.634×VDD	
0x0E	0.517×VDD	0.616×VDD	
0x0F	0.500×VDD	0.600×VDD	

7.5 Power-On Reset

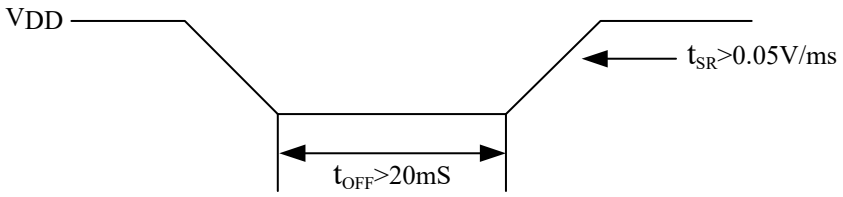
During the initialization of the power-on reset circuit(1ms),no I2C data transmission should occur.

The state of the internal circuit after initialization is as follows:

- When VLCD≤VDD, all COM/SEG pins output VDD.
- Display modes 1/4 duty and 1/3 bias.
- The system oscillator and LCD bias generator are turned off.
- LCD display off.
- The internal voltage adjustment function is enabled.
- The SEG/VLCD shared pin is set as the SEG pin.
- The VLCD foot detection function is disabled.
- The frame rate is set to 80Hz by default.
- The flashing function is disabled.

If,during operation, VDD falls below the specified minimum operating voltage, the power-on reset timing requirements must be met, that is, the VDD voltage must drop to 0V and remain at 0V for at least 20ms before rising to the normal operating voltage

Power-on Reset Timing:



7.6 LCD Communication Command

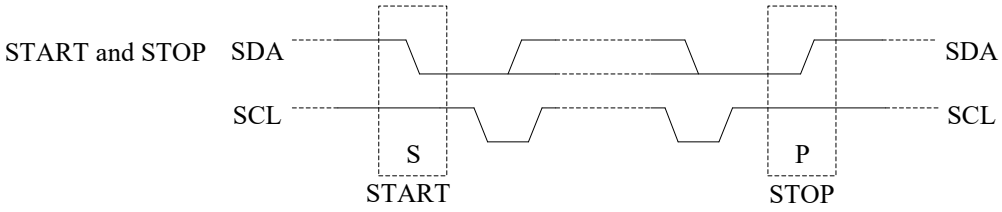
The LCD driver supports 44SEG × 4COMmodes, any unused SEG and COM pins should be left floating(NC).

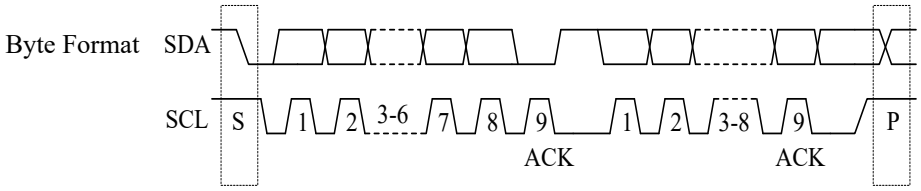
Two frame frequencies are provided, and you can choose to set them to 80Hz or 160Hz through the frame frequency setting command.

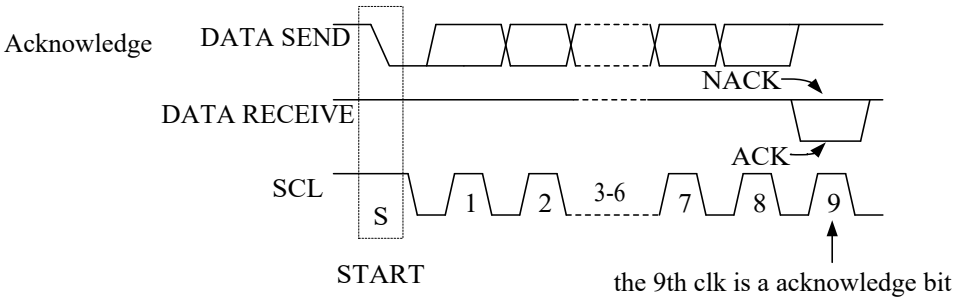
8 I2C Serial Interface

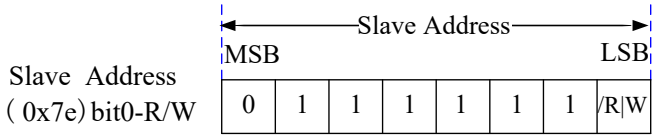
The VK2C22A features two communication pins compliant with the I2C protocol. open-drain outputs require external pull-up resistors.

The SCL pin is the clock input pin, and the SDA pin is the serial data input/output pin. When the I2C bus is idle, both pins remain at a logic high level.





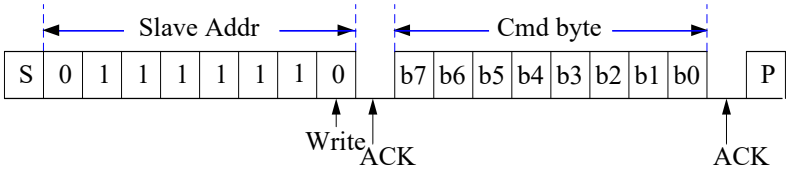




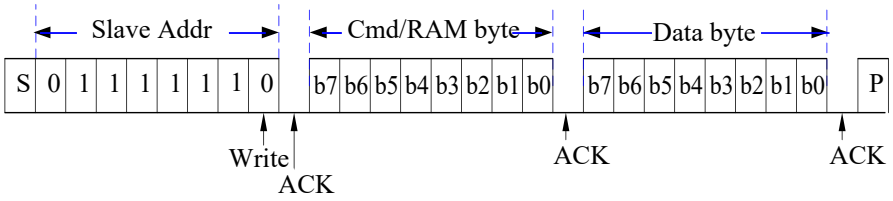
9 I2C Command Format

Write operation

Write commands

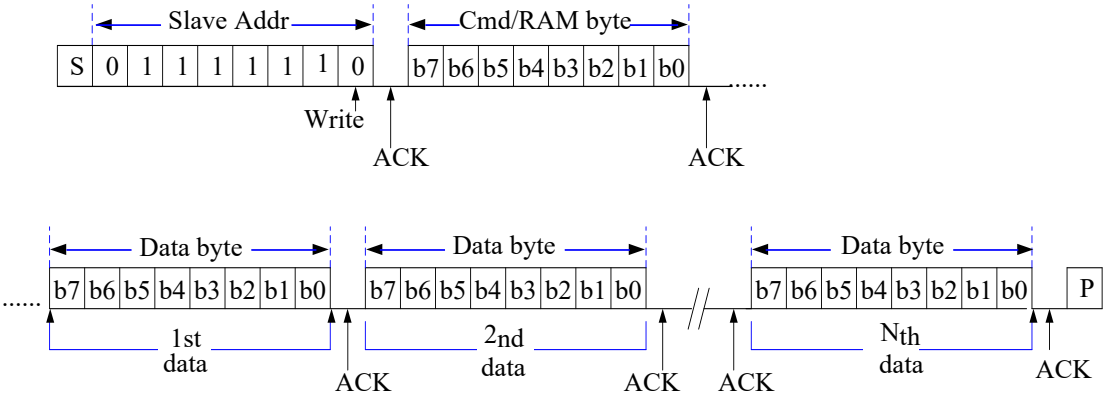


Write a single byte to the display RAM



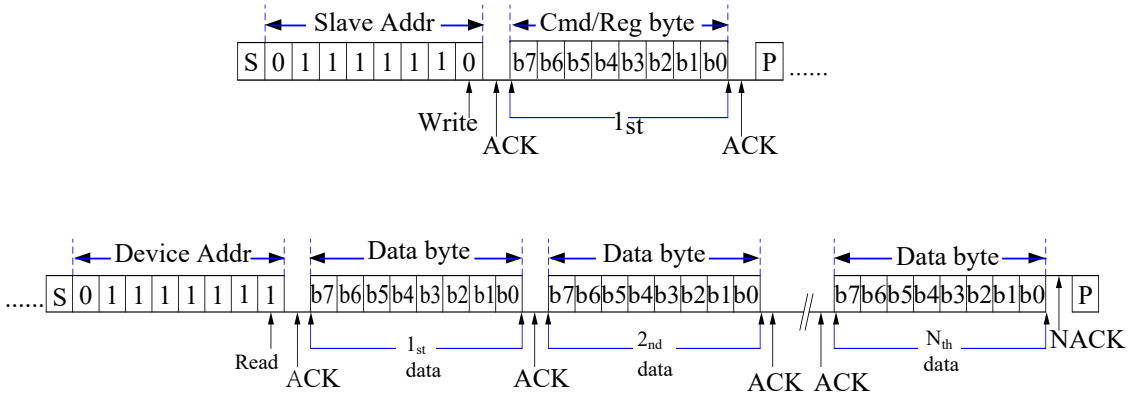
Note: If the byte after the Slave address is a command code, the byte after the command code is ignored.

Write multiple bytes to the display RAM

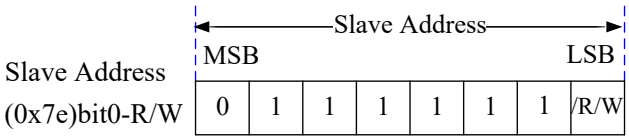


Read operation

Read multiple bytes from the display RAM



10 Command Summary



10.1 Display Data Command

Send display data to display RAM

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
Address pointer	1	0	0	0	A4	A3	A2	A1	A0	Display data start address	W	00H

10.2 Mode Set Command

Set BIAS and DUTY

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
Duty and Bias	1	1	0	0	F	S	E	0	M0		W	80H

Bit 4	Frame Frequency
F	
0	80Hz
1	160Hz

Bit 3	Bit 2	Internal RC oscillator	LCD display
S	E		
0	0	OFF	OFF
0	1	OFF	OFF
1	0	ON	OFF
1	1	ON	ON

Bit 0	Bias
M0	
0	1/3 bias
1	1/2 bias

10.3 Blinking Frequency Command

Set the blinking frequency

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
blinking freq set	1	1	1	0	0	0	0	BK1	BK0		W	C0H

Bit 1	Bit 0	blinking freq
BK1	BK0	
0	0	blinking off(Def)
0	1	2Hz
1	0	1Hz
1	1	0.5Hz

10.4 Internal Voltage Adjustment(IVA) Command

The IVA command allows selection of 16 voltage levels to adjust the LCD driver voltage

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
IVA set	1	0	1	DE	VE	DA3	DA2	DA1	DA0	SEG/VLCD pin can be set via the DE bit. internal voltage adjustment can be set via the VE bit. DA3~DA0 bits can be used to adjust the VLCD output voltage.	W	70H

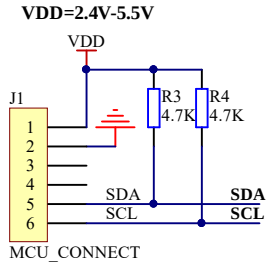
Note：

Bit 5 DE	Bit 4 VE	SEG /VLCD shared pin sel	internal voltage adjustment	Note
0	0	VLCD pin	off	• The SEG/VLCD shared pin is set to the VLCD pin. • The internal voltage adjustment function is prohibited. • A resistor is connected in series with the VLCD pin to the VDD pin to adjust the bias voltage. The DA3 to DA0 positions cannot be set to "0000". • The short-circuiting of pins DA3 to DA0 for VLCD and VDD must be set to "0000".
0	1	VLCD pin	on	• The SEG/VLCD shared pin is set to the VLCD pin. • Enable the internal voltage regulation function. • The VLCD pin outputs a bias voltage for external single-chip microcomputer detection.
1	0	SEG pin	off	• The SEG/VLCD shared pin is set to the SEG pin. • The internal voltage adjustment function is prohibited. • The bias voltage is provided by the internal VDD. • Regardless of the value of DA3 to DA0, the internal voltage follower is prohibited.
1	1	SEG pin	on	• Set the SEG/VLCD pin to the SEG pin. • Enable the internal voltage adjustment function.

- Power-on: Enable internal voltage Adjustment and the SEG/VLCD pin is set as the segment pin.
- When the DA0~DA3 bits are set to “0000”, the internal voltage is disabled.
- When the DA0~DA3 bits are set to other values except “0000”, internal voltage follower is enabled.

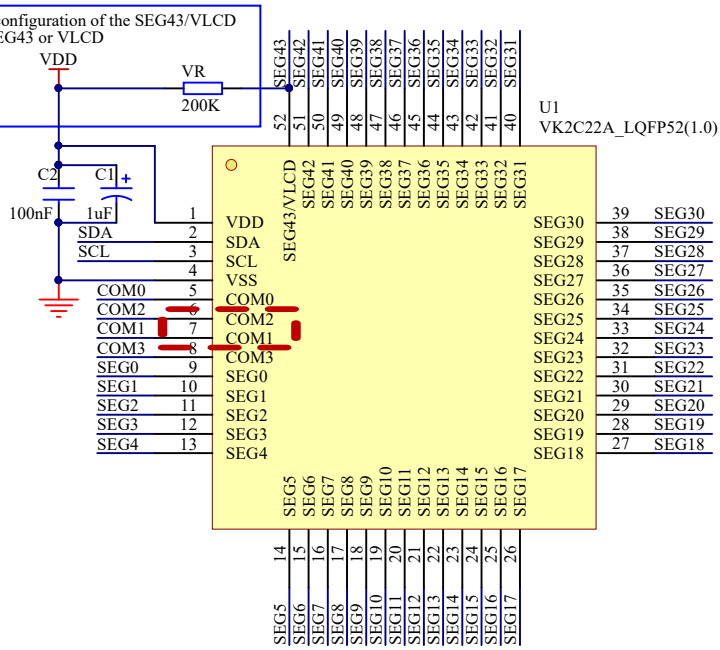
11 Application Circuits

When the surrounding interference is relatively large, a 10R to 1k resistor and a PF-level small capacitor to ground can be connected in series on the communication pin. When the power supply of the single-chip microcomputer (3.3V) and the driver chip (5V) is inconsistent, it is recommended to add a level conversion circuit on the communication pin



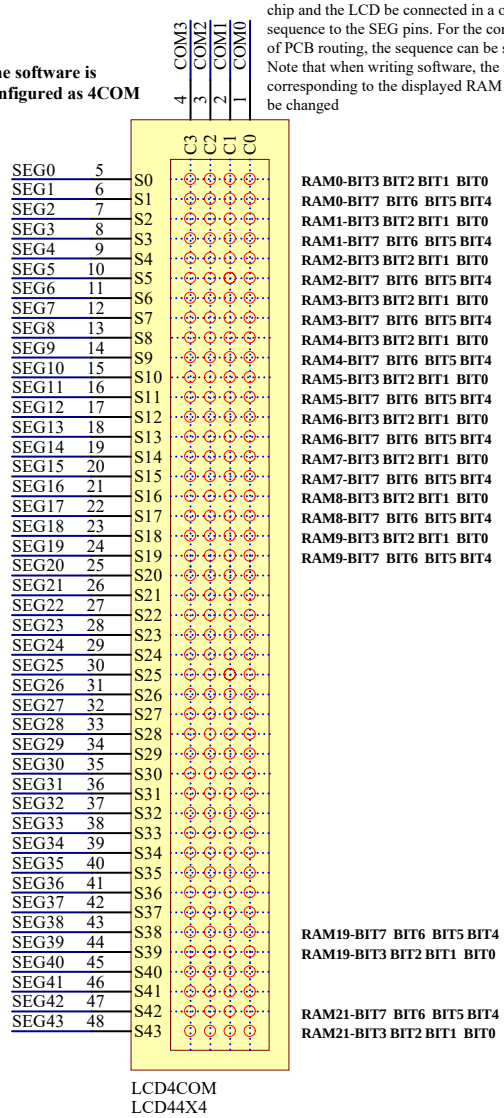
The software configuration of the SEG43/VLCD pin is VLCD
When VDD=5V and VR=200K:
The VLCD is approximately 4.2V
It is recommended to adjust the VR to the best display effect with a 510K adjustable resistor and take the resistance value at this time.

The software configuration of the SEG43/VLCD pin is either SEG43 or VLCD



It is recommended that the COM pins of the chip and the LCD be connected in a one-to-one sequence to the SEG pins. For the convenience of PCB routing, the sequence can be shuffled Note that when writing software, the sequence corresponding to the displayed RAM should also be changed

The software is configured as 4COM



RAM0-BIT3 BIT2 BIT1 BIT0
RAM0-BIT7 BIT6 BIT5 BIT4
RAM1-BIT3 BIT2 BIT1 BIT0
RAM1-BIT7 BIT6 BIT5 BIT4
RAM2-BIT3 BIT2 BIT1 BIT0
RAM2-BIT7 BIT6 BIT5 BIT4
RAM3-BIT3 BIT2 BIT1 BIT0
RAM3-BIT7 BIT6 BIT5 BIT4
RAM4-BIT3 BIT2 BIT1 BIT0
RAM4-BIT7 BIT6 BIT5 BIT4
RAM5-BIT3 BIT2 BIT1 BIT0
RAM5-BIT7 BIT6 BIT5 BIT4
RAM6-BIT3 BIT2 BIT1 BIT0
RAM6-BIT7 BIT6 BIT5 BIT4
RAM7-BIT3 BIT2 BIT1 BIT0
RAM7-BIT7 BIT6 BIT5 BIT4
RAM8-BIT3 BIT2 BIT1 BIT0
RAM8-BIT7 BIT6 BIT5 BIT4
RAM9-BIT3 BIT2 BIT1 BIT0
RAM9-BIT7 BIT6 BIT5 BIT4

RAM19-BIT7 BIT6 BIT5 BIT4
RAM19-BIT3 BIT2 BIT1 BIT0

RAM21-BIT7 BIT6 BIT5 BIT4
RAM21-BIT3 BIT2 BIT1 BIT0

12 Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3～6.5	V
Input Voltage	VIN	V_{SS}-0.3～V_{DD}+0.3	V
Storage Temperature	T_{STG}	-50～+125	℃
Operating Temperature	T_{OTG}	-40～+85	℃

12.2 DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	2.4	—	5.5	V	—	—
Operating current	I_{DD1}	—	18	27	μA	3V	No load,VLCD=VDD,1/3 bias, fLCD=80Hz,LCD off,Internal osc on,DA0~DA3 = "0000"
		—	25	40		5V	
Operating current	I_{DD2}	—	2	5	μA	3V	No load,VLCD=VDD,1/3 bias, fLCD=80Hz,LCD off,Internal osc on,DA0~DA3 = "0000"
		—	4	10		5V	
Standby Current	I_{STB}	—	0.1	1	μA	3V	No load, VLCD=VDD, LCD off, Internal osc off
		—	0.3	2		5V	
Low-level Input	V_{IL}	0	—	0.3	VDD	3V	SCL, SDA
						5V	
High-level Input	V_{IH}	0.7	—	1.0	VDD	3V	SCL, SDA
						5V	
Low Level Output Current	I_{OL}	3.0	—	—	mA	3V	V_{OL}=0.4V，SDA
		6.0	—	—		5V	
LCD COM Sink Current	I_{OL1}	250	400	—	μA	3V	V_{OL}=0.3V
		500	800	—		5V	V_{OL}=0.5V
LCD COM Source Current	I_{OH1}	-140	-230	—	μA	3V	V_{OH}=2.7V
		-300	-500	—		5V	V_{OH}=4.5V
LCD SEG Sink Current	I_{OL2}	250	400	—	μA	3V	V_{OL}=0.3V
		500	800	—		5V	V_{OL}=0.5V
LCD SEG Source Current	I_{OH2}	-140	-230	—	μA	3V	V_{OH}=2.7V
		-300	-500	—		5V	V_{OH}=4.5V

13 AC Electrical Characteristics

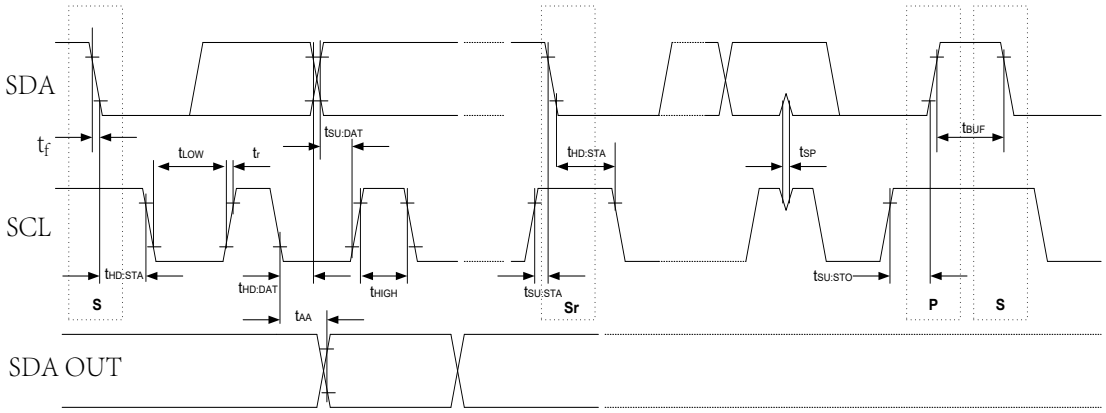
Frame Frequency

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
LCD Frame Frequency	fLCD1	72	80	88	Hz	4.0V	1/4 duty,25℃
LCD Frame Frequency	fLCD2	144	160	176	Hz	4.0V	1/4 duty,25℃
LCD Frame Frequency	fLCD3	52	80	124	Hz	4.0V	1/4 duty,-40 ~ +85℃
LCD Frame Frequency	fLCD4	104	160	248	Hz	4.0V	1/4 duty,-40 ~ +85℃

I2C parameter

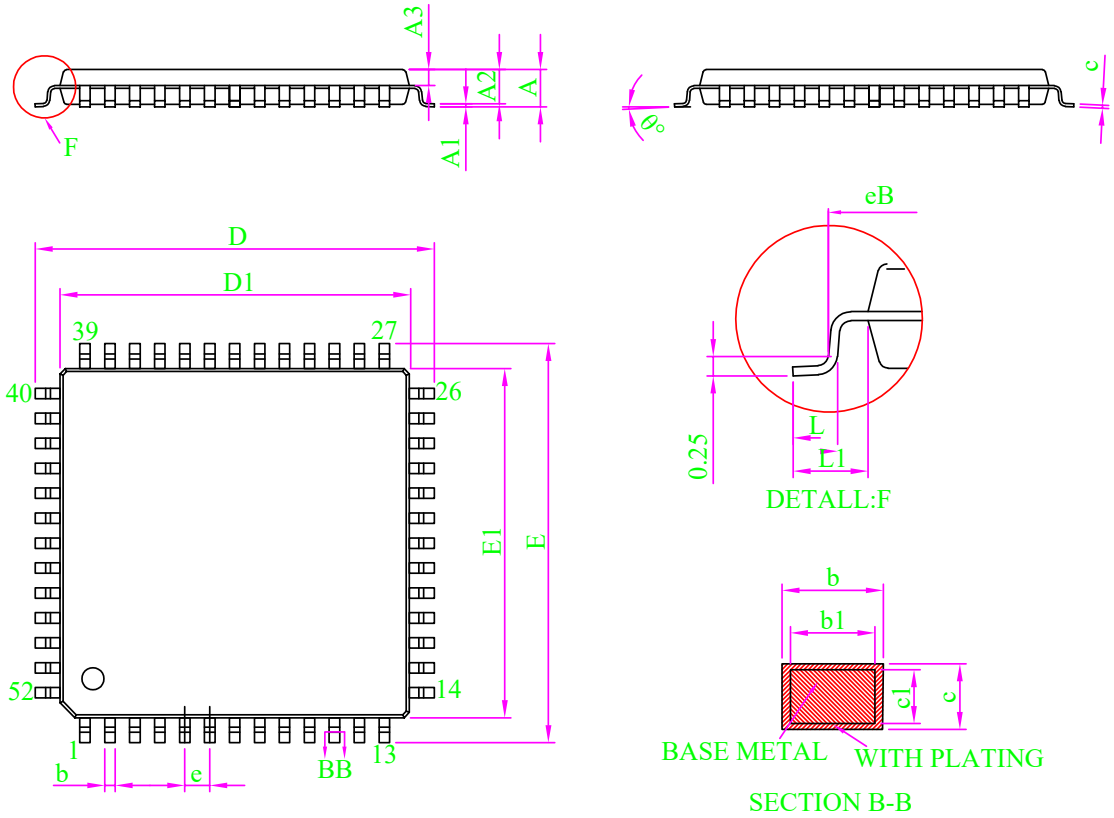
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Clock Frequency	f_{SCL}	—	—	400	kHz	3.0-5.5V	—
Bus Free Time	t_{BUF}	1.3	—	—	μs	3.0-5.5V	Time in which the bus must be free before a new transmission can start
Start Condition Hold Time	$t_{HD:STA}$	0.6	—	—	μs	3.0-5.5V	After this period, the first clock pulse is generated
SCL Low Time	t_{LOW}	1.3	—	—	μs	3.0-5.5V	—
SCL High Time	t_{HIGH}	0.6	—	—	μs	3.0-5.5V	—
Start Condition Setup Time	$t_{SU:STA}$	0.6	—	—	μs	3.0-5.5V	Only relevant for repeated START condition
Data Hold Time	$t_{HD:DAT}$	0	—	—	ns	3.0-5.5V	—
Data Setup Time	$t_{SU:DAT}$	100	—	—	ns	3.0-5.5V	—
SDA and SCL Rising Time	t_R	—	—	0.3	μs	3.0-5.5V	periodically sampled
SDA and SCL Falling Time	t_F	—	—	0.3	μs	3.0-5.5V	periodically sampled
Stop Condition Setup Time	$t_{SU:STO}$	0.6	—		μs	3.0-5.5V	—
Output Valid from Clock	t_{AA}	—	—	0.9	μs	3.0-5.5V	—
Input Filter Time Constant (SDA and SCL pin)	t_{SP}	—	—	50	ns	3.0-5.5V	Noise suppression time

I²C Timing


SDA
SCL
SDA OUT
tf
tLOW
tr
tSU:DAT
tHD:STA
tSP
tBUF
tHD:STA
tHD:DAT
tHIGH
tAA
tSU:STA
tSU:STO
S
Sr
P
S

14 Package Information

14.1 LQFP52（14.0mm × 14.0mm PP=1.0mm）



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.38	-	0.46
b1	0.37	0.40	0.43
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
eB	15.05	-	15.35
e	1.00 BSC		
L	0.45	-	0.75
L1	1.00 REF		
θ	0	-	7°

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16 Revision History

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Initial release	YES
2	1.1	2018-10-11	Add reference circuit	YES
3	1.2	2019-03-21	Alignment correction	YES
4	1.3	2025-06-19	Change Description	YES

[1] Please refer to the latest version of this document before starting or finalizing any design.

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