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VK2C21AQ Datasheet

20×4/16×8 LCD DRIVER

Rev.1.1

1 General Description

The VK2C21AQ is a dot-matrix memory-mapped LCD driver that supports LCD screens with a maximum of 80 dots (20SEG×4COM) or 128 dots (16SEG×8COM). The single-chip microcomputer can configure display parameters and read and write display data through the I2C interface, and can also enter power-saving mode through instructions. Its high anti-interference and low power consumption features make it suitable for water, electricity and gas meters as well as various industrial control instruments.

2 Key Features

- Operating voltage：2.4-5.5V
- Built-in RC oscillator (default)
- Selectable LCD bias: 1/3 or 1/4
- Selectable LCD duty: 1/4 or 1/8
- Built-in 20×4-bit、16×8-bit display RAM
- The frame rate can be configured as 80Hz or 160Hz
- Power-down mode via software command(LCD OFF, SYS DIS)
- I2C communication interface
- Display mode 20×4、16×8
- Three display overall flicker frequencies
- Software-configurable of LCD parameters
- Auto-increment addressing for sequential read/write
- VLCD pin provides the LCD driving voltage source(2.4-5.5V)
- It is equipped with a built-in 16-stage LCD driver voltage adjustment circuit
- Built-in power-on reset circuit (POR)
- Low power consumption and high anti-interference
- Available Packages:
  QFN28L(4.0mm × 4.0mm PP= 0.40mm)
  DICE
  COG

3 Product Selection

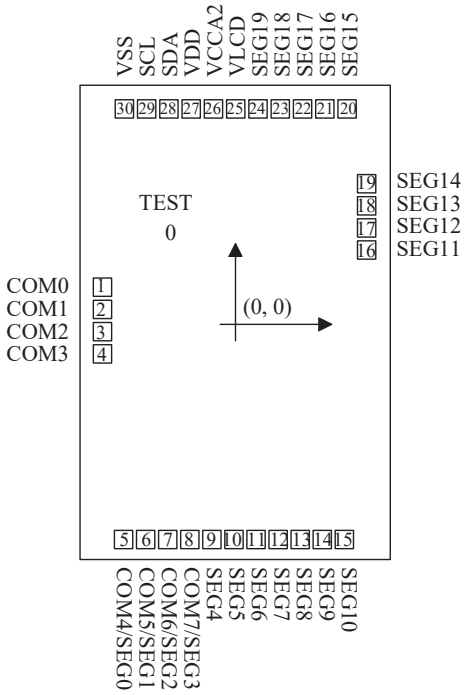
Part No.	SEG×COM	BIAS	DUTY	Packaging
VK2C21A	20×4,16×8	1/3,1/4	1/4,1/8	SOP28
VK2C21AA	20×4,16×8	1/3,1/4	1/4,1/8	SSOP28
VK2C21AQ	20×4,16×8	1/3,1/4	1/4,1/8	QFN28L
VK2C21B	16×4,12×8	1/3,1/4	1/4,1/8	SOP24
VK2C21BA	16×4,12×8	1/3,1/4	1/4,1/8	SSOP24
VK2C21BQ	16×4,12×8	1/3,1/4	1/4,1/8	QFN24L
VK2C21C	12×4,8×8	1/3,1/4	1/4,1/8	SOP20
VK2C21CQ	12×4,8×8	1/3,1/4	1/4,1/8	QFN20L
VK2C21D	8×4,4×8	1/3,1/4	1/4,1/8	SOP16
VK2C21DQ	8×4,4×8	1/3,1/4	1/4,1/8	QFN16L
VK2C22A	44×4	1/2,1/3	1/4	LQFP52
VK2C22B	40×4	1/2,1/3	1/4	LQFP48
VK2C22	44×4	1/2,1/3	1/4	DICE
VK2C23A	55×4,51×8	1/3,1/4	1/4, 1/8	LQFP64
VK2C23B	35×8	1/3,1/4	1/8	LQFP48
VK2C23	56×4,52×8	1/3,1/4	1/4,1/8	DICE
VK2C24A	71×4,67×8,59×16	1/2,1/3,1/4,1/5	1/4,1/8,1/16	LQFP80
VK2C24B	55×4,51×8,43×16	1/2,1/3,1/4,1/5	1/4,1/8,1/16	LQFP64
VK2C24	72×4,68×8,60×16	1/2,1/3,1/4,1/5	1/4,1/8,1/16	DICE

4 Ordering Information

Part No.	Packaging	Tube Qty	Tray(reel)Qty	Box Qty	Total Qty	Notes
VK2C21A	SOP28	26/tube	-	2080/box	20800 PCS	
VK2C21AA	SSOP28	50/tube	-	5000/box	50000 PCS	
VK2C21AQ	QFN28L	-	490/reel	4900/box	29400 PCS	
VK2C21B	SOP24	30/tube	-	2400/box	24000 PCS	
VK2C21BA	SSOP24	50/tube	-	10000/box	100000 PCS	
VK2C21BQ	QFN24L	-	490/reel	4900/box	29400 PCS	
VK2C21C	SOP20	36/tube	-	2880/box	28800 PCS	
VK2C21CQ	QFN20L	-	490/reel	4900/box	29400 PCS	
VK2C21D	SOP16	50/tube	-	10000/box	100000 PCS	
VK2C21DQ	QFN16L	-	3000/reel	3000/box	120000 PCS	
VK2C22A	LQFP52	-	90/tray	900/box	5400 PCS	
VK2C22B	LQFP48	-	250/tray	2500/box	15000 PCS	
VK2C22	DICE	-	400/tray	2000/box	4000 PCS	DICE
VK2C23A	LQFP64	-	250/tray	2500/box	15000 PCS	
VK2C23B	LQFP48	-	250/tray	2500/box	15000 PCS	
VK2C23	DICE	-	250/tray	1000/box	2000 PCS	DICE
VK2C24A	LQFP80	-	90/tray	900/box	5400 PCS	
VK2C24B	LQFP64	-	250/tray	2500/box	15000 PCS	
VK2C24	DICE	-	200/tray	1000/box	2000 PCS	DICE

5 COB Pad Information

5.1 COB Pad Assignment



Chip size: 1150×1715 um ², substrate potential: VSS
PAD size: 70×70 um
VDD (Pad27) and VCCA2 (Pad26) must be bound together.
The VLCD (Pad25) and SEG19 (Pad24) must be bound together.

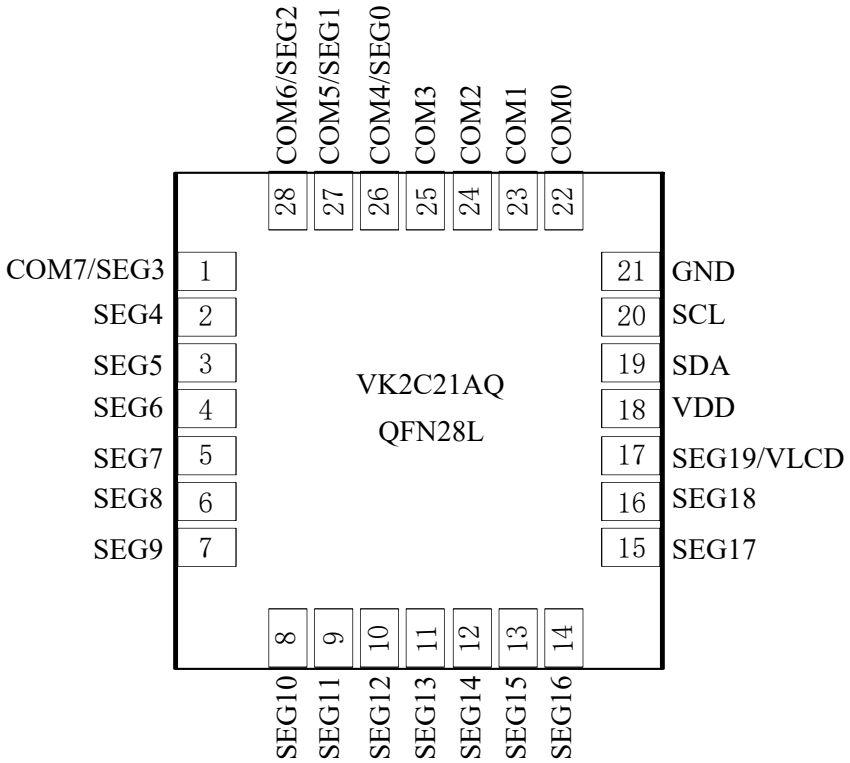
When the VLCD pins are configured to detect the internal bias voltage, the LCD drive voltage can be externally temperature-compensated through the voltage provided by the VLCD pins.

5.2 COB PAD Coordinates

Unit: um

Pad No	Name	X	Y	Pad No	Name	X	Y
1	COM0	93.11	1016.655	17	SEG12	1056.89	1621.89
2	COM1	93.11	932.155	18	SEG13	1056.89	1265.89
3	COM2	93.11	847.655	19	SEG14	1056.89	1350.39
4	COM3	93.11	763.155	20	SEG15	1040.39	1621.89
5	COM4/SEG0	130.97	93.11	21	SEG16	950.39	1621.89
6	COM5/SEG1	220.97	93.11	22	SEG17	860.39	1621.89
7	COM6/SEG2	310.9	93.11	23	SEG18	756.75	1621.89
8	COM7/SEG3	400.97	93.11	24	SEG19	666.75	1621.89
9	SEG4	490.97	93.11	25	VLCD	576.75	1621.89
10	SEG5	580.97	93.11	26	VCCA2	486.75	1621.89
11	SEG6	670.97	93.11	27	VDD	396.75	1621.89
12	SEG7	760.97	93.11	28	SDA	306.75	1621.89
13	SEG8	850.97	93.11	29	SCL	199.61	1621.89
14	SEG9	940.97	93.11	30	VSS	109.61	1621.89
15	SEG10	1030.97	93.11				
16	SEG11	1056.89	1096.89	0	TEST	295.57	1211.795

6 Package Pinout Information(QFN28L)



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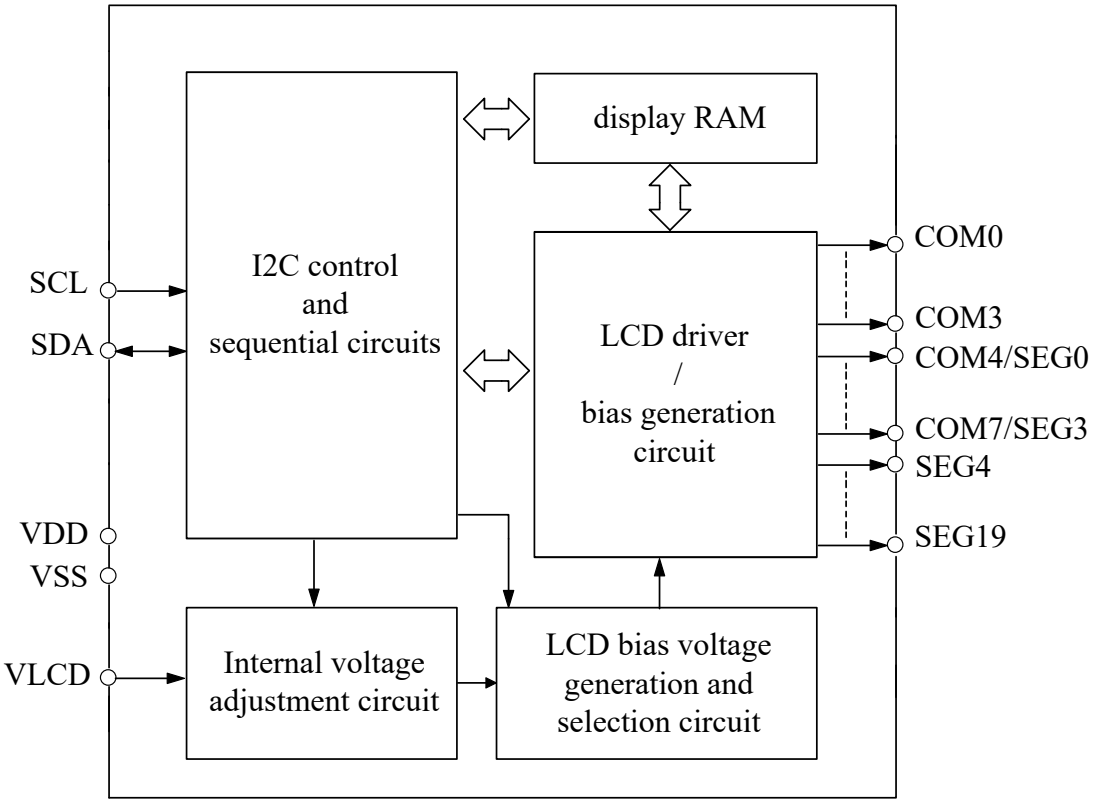
6.1 VK2C21AQ/QFN28L Pin Description

No.	Name	I/O	Function
18	VDD	VDD	Positive power supply
19	SDA	I/O	Serial Data Input/Output for I2C interface
20	SCL	I	Serial Clock Input for I2C interface
21	VSS	VSS	Negative power supply
22-25	COM0-COM3	O	LCD COM drive outputs
26-28, 1	COM4/SEG0-COM7/SEG3	O	LCD SEG/COM drive outputs， software configuration 4COM or 8COM
2-16	SEG4-SEG18	O	LCD SEG drive outputs
17	SEG19/VLCD	I/O	When the VLCD pin and VDD pin are short-circuited and the internal voltage regulation function is enabled, the drive voltage is regulated by the internal voltage regulation function. When the VLCD pin is connected in series with the VDD pin and the internal voltage adjustment function is disabled, the LCD driving voltage is set by the series resistor.

7 Functional Description

7.1 Block Diagram



7.2 Display RAM

The display RAM is organized as 16×8 bits (or 20×4 bits for 4-COM mode), which stores the displayed data. The content of the display RAM is directly mapped to the display content of the LCD driver. Display RAM data is accessed via I2C commands.

The following is a mapping from the RAM to the LCD pattern:

Output	COM3	COM2	COM1	COM0	Output	COM3	COM2	COM1	COM0	Address
SEG1					SEG0					0x00
SEG3					SEG2					0x01
SEG5					SEG4					0x02
SEG7					SEG6					0x03
SEG9					SEG8					0x04
SEG11					SEG10					0x05
SEG13					SEG12					0x06
SEG15					SEG14					0x07
SEG17					SEG16					0x08
SEG19					SEG18					0x09
Data	Bit7	Bit6	Bit5	Bit4		Bit3	Bit2	Bit1	Bit0	

RAM Mapping of 20×4

Output	COM7/ SEG3	COM6/ SEG2	COM5/ SEG1	COM4/ SEG0	COM3	COM2	COM1	COM0	Address
SEG4									0x00
SEG5									0x01
SEG6									0x02
SEG7									0x03
SEG8									0x04
SEG9									0x05
SEG10									0x06
SEG11									0x07
SEG12									0x08
SEG13									0x09
SEG14									0x0A
SEG15									0x0B
SEG16									0x0C
SEG17									0x0D
SEG18									0x0E
SEG19									0x0F
Data	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

RAM Mapping of 16×8

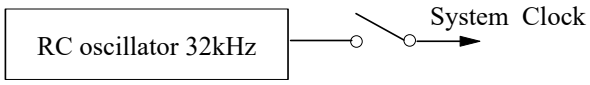
7.3 System Oscillator

The clock of VK2C21AQ is used to generate LCD drive signals and internal logic timing. The system clock is derived from the internal RC oscillator (32kHz), and the system clock frequency (fSYS) determines the LCD frame frequency.

The system setting command can start or stop the system oscillator. After the display shows off and the system oscillator stops, the system enters the power-saving mode.

When the system is powered on and working, the system oscillator is in a stopped state.

The Settings of the system oscillation are shown in the following figure:



7.4 LCD operating voltage

The LCD driving voltage can be obtained through the VLCD pins or by selecting 16 levels of voltage through the internal configuration.
When the VDD pad is connected to the VCCA2 pad, the LCD driving voltage can be obtained by connecting the VLCD pin to VDD through a series resistor (VLCD≤VDD).

The internal 16-level voltage is set through a 4-bit programmable analog switch, as shown in the following table:

Bias / DA3~DA0	1/3	1/4	Note
0x00	1.000×VDD	1.000×VDD	Default
0x01	0.944×VDD	0.957×VDD	
0x02	0.894×VDD	0.918×VDD	
0x03	0.849×VDD	0.882×VDD	
0x04	0.808×VDD	0.849×VDD	
0x05	0.771×VDD	0.818×VDD	
0x06	0.738×VDD	0.789×VDD	
0x07	0.707×VDD	0.763×VDD	
0x08	0.678×VDD	0.738×VDD	
0x09	0.652×VDD	0.714×VDD	
0x0A	0.628×VDD	0.692×VDD	
0x0B	0.605×VDD	0.672×VDD	
0x0C	0.584×VDD	0.652×VDD	
0x0D	0.565×VDD	0.634×VDD	
0x0E	0.547×VDD	0.616×VDD	
0x0F	0.529×VDD	0.600×VDD	

7.5 Power-On Reset

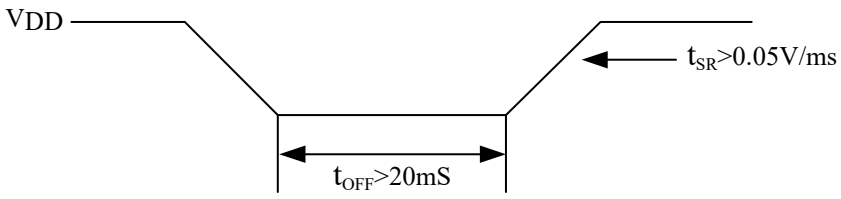
During the initialization of the power-on reset circuit(1ms),no I2C data transmission should occur.

The state of the internal circuit after initialization is as follows:

- When VDD≤VLCD, all COM/SEG pins output VLCD.
- Display modes 1/4 duty and 1/3 bias.
- The system oscillator and LCD bias generator are turned off.
- LCD display off.
- The internal voltage adjustment function is enabled.
- The SEG/VLCD shared pin is set as the SEG pin.
- The VLCD foot detection function is disabled.
- The frame rate is set to 80Hz by default.
- The flashing function is disabled.

If,during operation, VDD falls below the specified minimum operating voltage, the power-on reset timing requirements must be met, that is, the VDD voltage must drop to 0V and remain at 0V for at least 20ms before rising to the normal operating voltage

Power-on Reset Timing:



7.6 LCD Communication Command

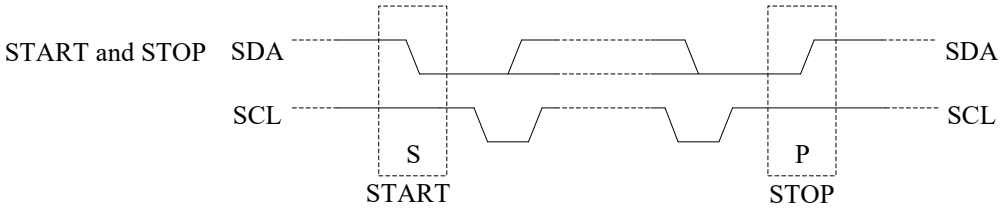
The LCD driver supports 20SEG×4COM and 16SEG×8COM modes, any unused SEG and COM pins should be left floating(NC).

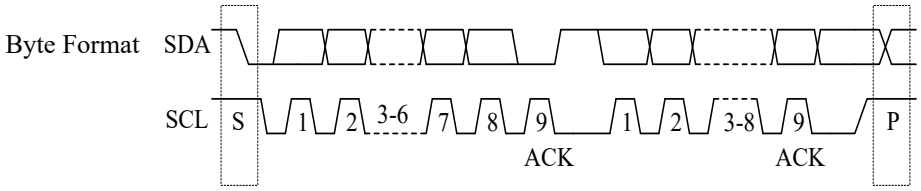
Two frame rates are provided. You can choose between 80Hz and 160Hz through the frame rate setting command.

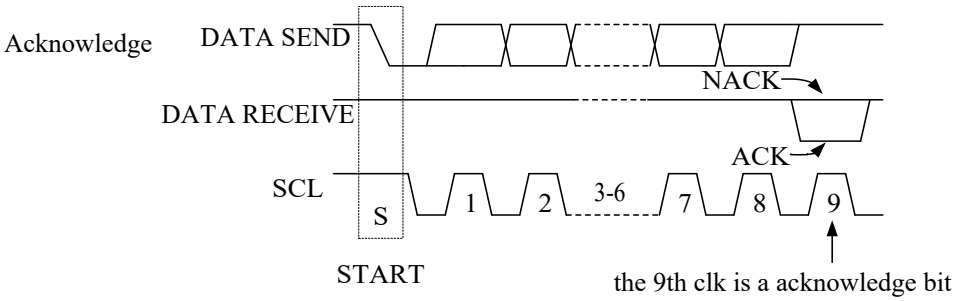
8 I2C Serial Interface

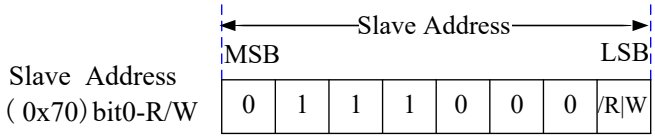
The VK2C21AQ features two communication pins compliant with the I2C protocol. open-drain outputs require external pull-up resistors.

The SCL pin is the clock input pin, and the SDA pin is the serial data input/output pin. When the I2C bus is idle, both pins remain at a logic high level.





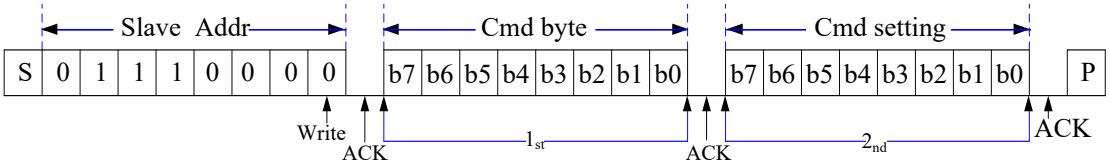




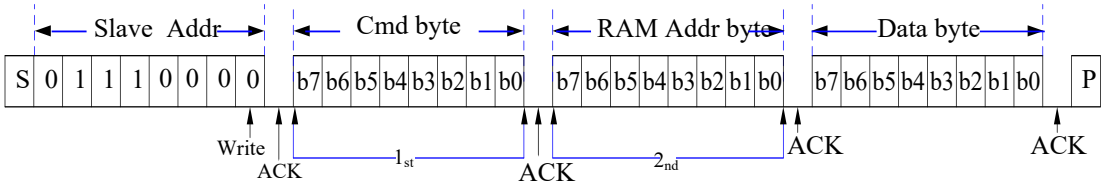
9 I2C Command Format

Write operation

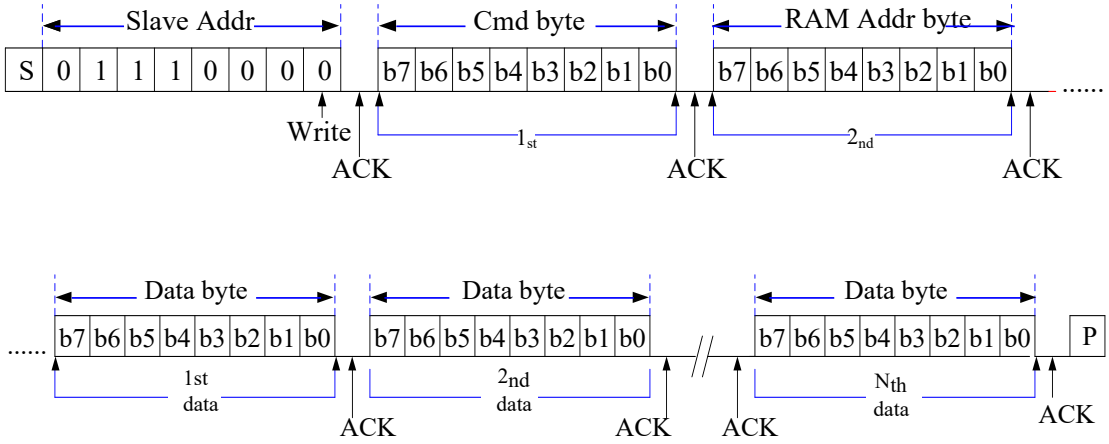
Write commands



Write a single byte to the display RAM

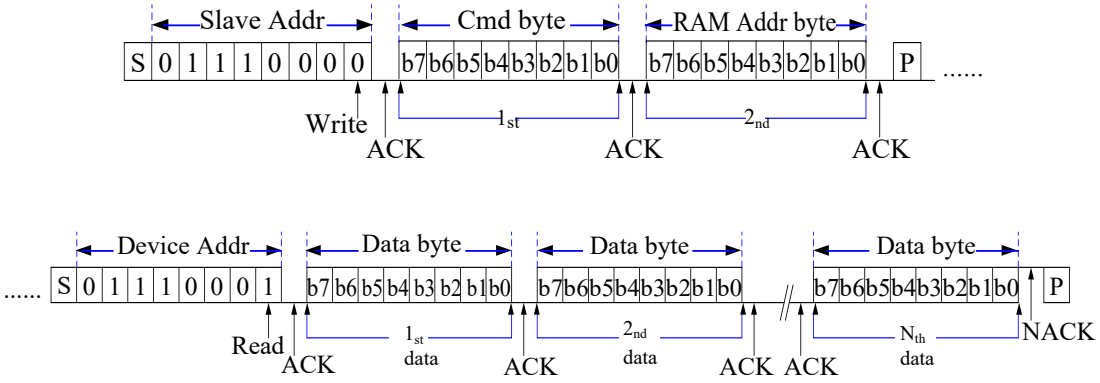


Write multiple bytes to the display RAM

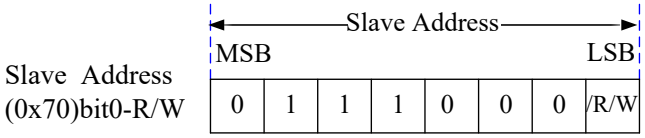


Read Operation

Read multiple bytes from the display RAM



10 Command Summary



10.1 Display Data Command

Send display data to display RAM

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
Display data command	1st	1	0	0	0	0	0	0	0		W	
Address pointer	2nd	X	X	A5	A4	A3	A2	A1	A0	Display data start address	W	00H

10.2 Mode Set Command

Set BIAS and DUTY

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
mode set cmd	1st	1	0	0	0	0	0	1	0		W	
Duty and Bias	2nd	X	X	X	X	X	X	Duty	Bias		W	00H

Bit 1	Bit 0	Duty	Bias
Duty	Bias		
0	0	1/4 duty	1/3 bias
0	1	1/4 duty	1/4 bias
1	0	1/8 duty	1/3 bias
1	1	1/8 duty	1/4 bias

10.3 System Set Command

Enable/disable the internal system oscillator and LCD display

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
system set cmd	1st	1	0	0	0	0	1	0	0		W	
System oscillator and Display on/ off set	2nd	X	X	X	X	X	X	S	E		W	00H

Bit 1	Bit 0	internal oscillator	LCD on/off
S	E		
0	X	off	off
1	0	on	off
1	1	on	on

10.4 Frame Frequency Command

Selects the frame frequency

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
frame freq cmd	1st	1	0	0	0	0	1	1	0		W	
frame freq set	2nd	X	X	X	X	X	X	X	F		W	00H

Bit 0	Frame Frequency
F	
0	80Hz
1	160Hz

10.5 Blinking Frequency Command

Set the blinking frequency

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
blinking freq cmd	1st	1	0	0	0	1	0	0	0		W	
blinking freq set	2nd	X	X	X	X	X	X	BK1	BK0		W	00H

Bit 1	Bit 0	blinking freq
BK1	BK0	
0	0	blinking off(Def)
0	1	2Hz
1	0	1Hz
1	1	0.5Hz

10.6 Internal Voltage Adjustment(IVA) Command

The IVA command allows selection of 16 voltage levels to adjust the LCD driver voltage

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
IVA cmd	1st	1	0	0	0	1	0	1	0		W	
IVA set	2nd	X	X	DE	VE	DA3	DA2	DA1	DA0	SEG/VLCD pin can be set via the DE bit. internal voltage adjustment can be set via the VE bit. DA3~DA0 bits can be used to adjust the VLCD output voltage.	W	30H

Note：

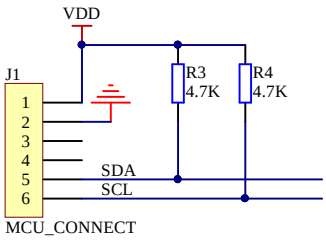
Bit 5	**Bit 4**	**SEG19/VLCD**	internal voltage	Note
DE	**VE**	shared pin sel	adjustment	
0	0	VLCD pin	off	● SEG/VLCD pin is set as the VLCD pin ● Disable internal voltage adjustment function ● An external resistor is connected in series between the VLCD pin and the VDD pin to adjust the bias voltage. At the same time, the DA3-DA0 bit must be set to a value other than "0000" to enable the internal voltage follower. ● VLCD pin is connected to the VDD pin, the internal voltage must be disabled by set DA3~DA0 as"0000".
0	1	VLCD pin	on	• SEG/VLCD pin is set as the VLCD pin • Enable internal voltage adjustment function • The VLCD pin is an output pin, and the voltage of the VLCD pin is detected by the MCU.
1	0	SEG19 pin	off	• SEG/VLCD pin is set as the segment pin • Disable internal voltage adjustment function. • The bias voltage is provided by internal VDD. • Regardless of the value of DA3-DA0, the internal voltage follower is prohibited.
1	1	SEG19 pin	on	• SEG/VLCD pin is set as the segment pin • Enable internal voltage adjustment function

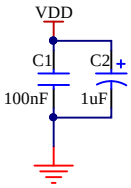
- Power-on: Enable internal voltage Adjustment and the SEG/VLCD pin is set as the segment pin.
- When the DA0~DA3 bits are set to “0000”, the internal voltage is disabled.
- When the DA0~DA3 bits are set to other values except “0000”, internal voltage follower is enabled.

11 Application Circuits

When the surrounding interference is relatively large, a 10R to 1k resistor and a PF-level small capacitor to ground can be connected in series on the communication pin. When the power supply of the single-chip microcomputer (3.3V) and the driver chip (5V) is inconsistent, it is recommended to add a level conversion circuit on the communication pin

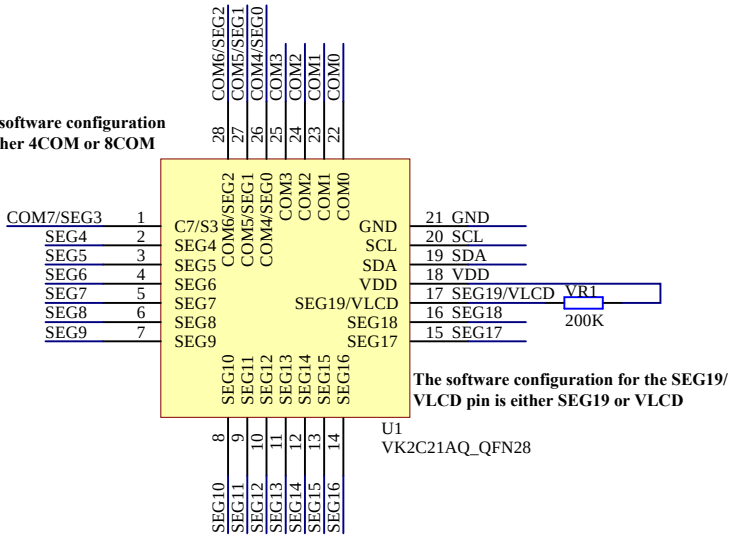
VDD=2.4V-5.5V





The software configuration of SEG19/VLCD pins is VLCD
When VDD=5V and VR=200K:
The VLCD is approximately 4.2V
It is recommended to use a 510K adjustable resistor for VR to adjust it to the best display effect and take the resistance value at this time.

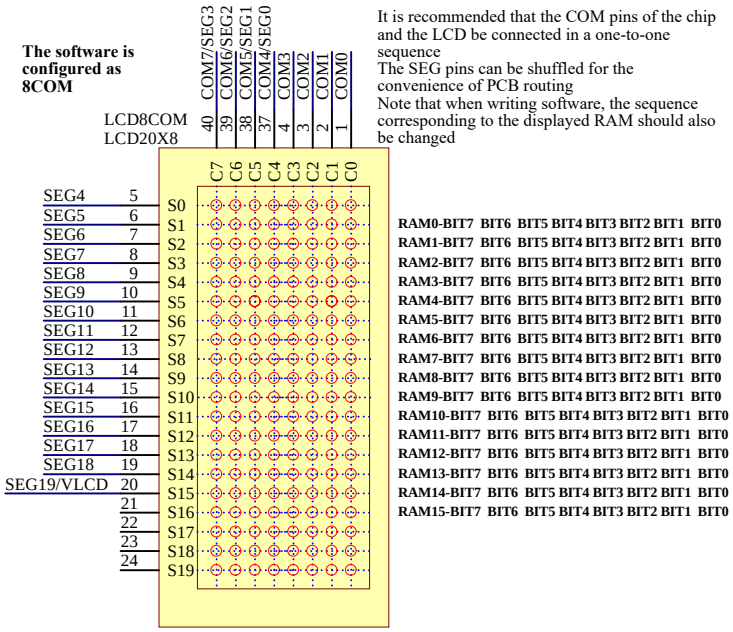
The software configuration is either 4COM or 8COM



The software configuration for the SEG19/ VLCD pin is either SEG19 or VLCD

The software is configured as 8COM

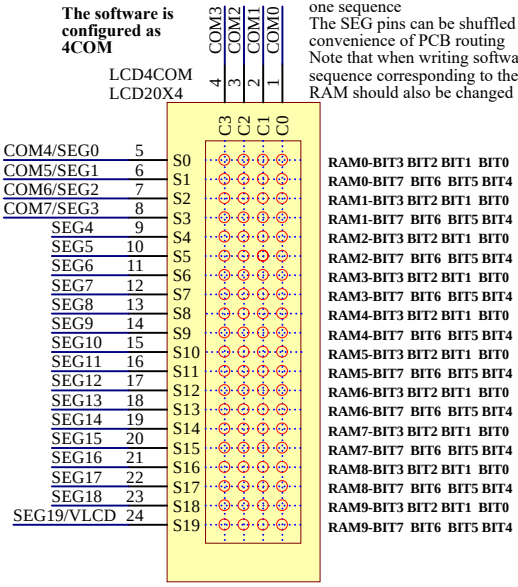
It is recommended that the COM pins of the chip and the LCD be connected in a one-to-one sequence
The SEG pins can be shuffled for the convenience of PCB routing
Note that when writing software, the sequence corresponding to the displayed RAM should also be changed



RAM0-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM1-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM2-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM3-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM4-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM5-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM6-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM7-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM8-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM9-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM10-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM11-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM12-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM13-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM14-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
RAM15-BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0

The software is configured as 4COM

It is recommended that the COM pins of the chip and the LCD be connected in a one-to-one sequence
The SEG pins can be shuffled for the convenience of PCB routing
Note that when writing software, the sequence corresponding to the displayed RAM should also be changed



RAM0-BIT3 BIT2 BIT1 BIT0
RAM0-BIT7 BIT6 BIT5 BIT4
RAM1-BIT3 BIT2 BIT1 BIT0
RAM1-BIT7 BIT6 BIT5 BIT4
RAM2-BIT3 BIT2 BIT1 BIT0
RAM2-BIT7 BIT6 BIT5 BIT4
RAM3-BIT3 BIT2 BIT1 BIT0
RAM3-BIT7 BIT6 BIT5 BIT4
RAM4-BIT3 BIT2 BIT1 BIT0
RAM4-BIT7 BIT6 BIT5 BIT4
RAM5-BIT3 BIT2 BIT1 BIT0
RAM5-BIT7 BIT6 BIT5 BIT4
RAM6-BIT3 BIT2 BIT1 BIT0
RAM6-BIT7 BIT6 BIT5 BIT4
RAM7-BIT3 BIT2 BIT1 BIT0
RAM7-BIT7 BIT6 BIT5 BIT4
RAM8-BIT3 BIT2 BIT1 BIT0
RAM8-BIT7 BIT6 BIT5 BIT4
RAM9-BIT3 BIT2 BIT1 BIT0
RAM9-BIT7 BIT6 BIT5 BIT4

12 Electrical Characteristics

12.1 Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power voltage	VDD	-0.3～6.5	V
Input Voltage	VIN	V_{SS}-0.3～V_{DD}+0.3	V
Storage Temperature	T_{STG}	-50～+125	℃
Operating Temperature	T_{OTG}	-40～+85	℃

12.2 DC Electrical Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	2.4	—	5.5	V	—	—
Operating current	I_{DD1}	—	18	27	μA	3V	No load,VLCD=VDD,1/3 bias, fLCD=80Hz,LCD off,Internal osc on,DA0~DA3 = "0000"
		—	25	40		5V	
Operating current	I_{DD2}	—	2	5	μA	3V	No load,VLCD=VDD,1/3 bias, fLCD=80Hz,LCD off,Internal osc on,DA0~DA3 = "0000"
		—	4	10		5V	
Standby Current	I_{STB}	—	0.1	1	μA	3V	No load, VLCD=VDD, LCD off, Internal osc off
		—	0.3	2		5V	
Low-level Input	V_{IL}	0	—	0.3	VDD	3V	SCL, SDA
						5V	
High-level Input	V_{IH}	0.7	—	1.0	VDD	3V	SCL, SDA
						5V	
Low Level Output Current	I_{OL}	3.0	—	—	mA	3V	V_{OL}=0.4V，SDA
		6.0	—	—		5V	
LCD COM Sink Current	I_{OL1}	250	400	—	μA	3V	V_{OL}=0.3V
		500	800	—		5V	V_{OL}=0.5V
LCD COM Source Current	I_{OH1}	-140	-230	—	μA	3V	V_{OH}=2.7V
		-300	-500	—		5V	V_{OH}=4.5V
LCD SEG Sink Current	I_{OL2}	250	400	—	μA	3V	V_{OL}=0.3V
		500	800	—		5V	V_{OL}=0.5V
LCD SEG Source Current	I_{OH2}	-140	-230	—	μA	3V	V_{OH}=2.7V
		-300	-500	—		5V	V_{OH}=4.5V

13 AC Electrical Characteristics

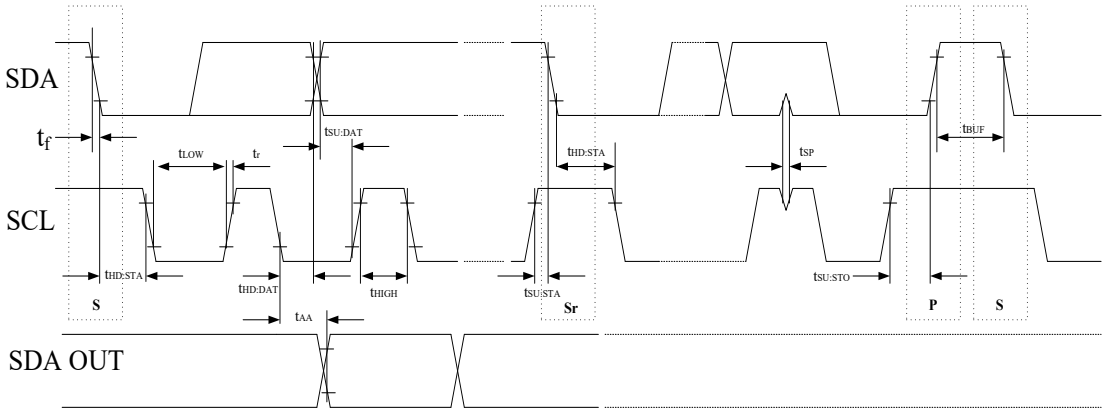
Frame Frequency

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
LCD Frame Frequency	fLCD1	72	80	88	Hz	4.0V	1/4 duty,25℃
LCD Frame Frequency	fLCD2	144	160	176	Hz	4.0V	1/4 duty,25℃
LCD Frame Frequency	fLCD3	52	80	124	Hz	4.0V	1/4 duty,-40 ~ +85℃
LCD Frame Frequency	fLCD4	104	160	248	Hz	4.0V	1/4 duty,-40 ~ +85℃

I2C parameter

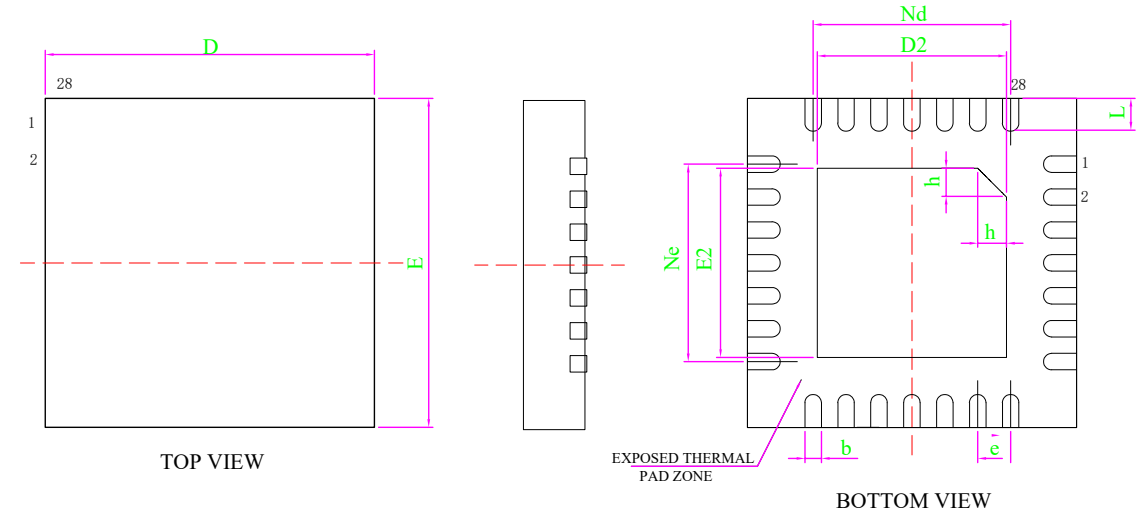
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Clock Frequency	f_{SCL}	—	—	400	kHz	3.0-5.5V	—
Bus Free Time	t_{BUF}	1.3	—	—	μs	3.0-5.5V	Time in which the bus must be free before a new transmission can start
Start Condition Hold Time	$t_{HD:STA}$	0.6	—	—	μs	3.0-5.5V	After this period, the first clock pulse is generated
SCL Low Time	t_{LOW}	1.3	—	—	μs	3.0-5.5V	—
SCL High Time	t_{HIGH}	0.6	—	—	μs	3.0-5.5V	—
Start Condition Setup Time	$t_{SU:STA}$	0.6	—	—	μs	3.0-5.5V	Only relevant for repeated START condition
Data Hold Time	$t_{HD:DAT}$	0	—	—	ns	3.0-5.5V	—
Data Setup Time	$t_{SU:DAT}$	100	—	—	ns	3.0-5.5V	—
SDA and SCL Rising Time	t_R	—	—	0.3	μs	3.0-5.5V	periodically sampled
SDA and SCL Falling Time	t_F	—	—	0.3	μs	3.0-5.5V	periodically sampled
Stop Condition Setup Time	$t_{SU:STO}$	0.6	—		μs	3.0-5.5V	—
Output Valid from Clock	t_{AA}	—	—	0.9	μs	3.0-5.5V	—
Input Filter Time Constant (SDA and SCL pin)	t_{SP}	—	—	50	ns	3.0-5.5V	Noise suppression time

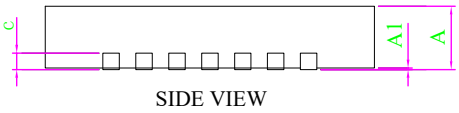
I²C Timing


SDA
SCL
SDA OUT
tf
tLOW
tr
tSU:DAT
tHD:STA
tSP
tBUF
tHD:STA
tHD:DAT
tHIGH
tAA
tSU:STA
tSU:STO
S
Sr
P
S

14 Package Information

14.1 QFN28L(4.0mm × 4.0mm PP= 0.40mm)





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.20	2.30	2.40
e	0.40BSC		
Ne	2.40BSC		
Nd	2.40BSC		
E	3.90	4.00	4.10
E2	2.20	2.30	2.40
L	0.35	0.40	0.45
h	0.30	0.35	0.40

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16 Revision History

No.	Version	Date	Modify the content	Check
1	1.0	2022-08-09	Initial release	YES
2	1.1	2025-06-23	Change Description	YES

[1] Please refer to the latest version of this document before starting or finalizing any design.

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