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Vinka Microelectronics

VK1626 Datasheet

48×16 LCD DRIVER

Rev.1.3

1 General Description

The VK1626 is a RAM-mapped LCD segment driver capable of supporting up to 768 segments (48 SEG × 16 COM).
The device communication via a 3-wire or 4-wire serial interface, which is used for display parameter configuration, data transmission, and Power-down control.

2 Key Features

- Operating voltage:2.4-5.2V
- Integrated RC oscillator (default)
- External crystal input: 32.768 kHz (OSCO, OSCI)
- Selectable LCD bias:1/5
- Selectable LCD duty:1/16
- Built-in 48 × 16-bit display RAM
- Configurable buzzer output: 2 kHz or 4 kHz
- Power-down mode via software command(LCD OFF, SYS DIS)
- Eight selectable clock sources for time base / WDT
- WDT or time base overflow flag output via /IRQ pin
- 3 wire or 4 wire serial communication interface
- Software-configurable of LCD parameters
- Dual command formats for configuration and access
- Auto-increment addressing for sequential read/write
- VLCD adjustable via external pin (≤ VDD)
- Available Packages:
  LQFP100(14.0mm × 14.0mm PP=0.5mm)
  QFP100(20.0mm × 14.0mm PP=0.65mm)
  DICE
  COG

3 Product Selection

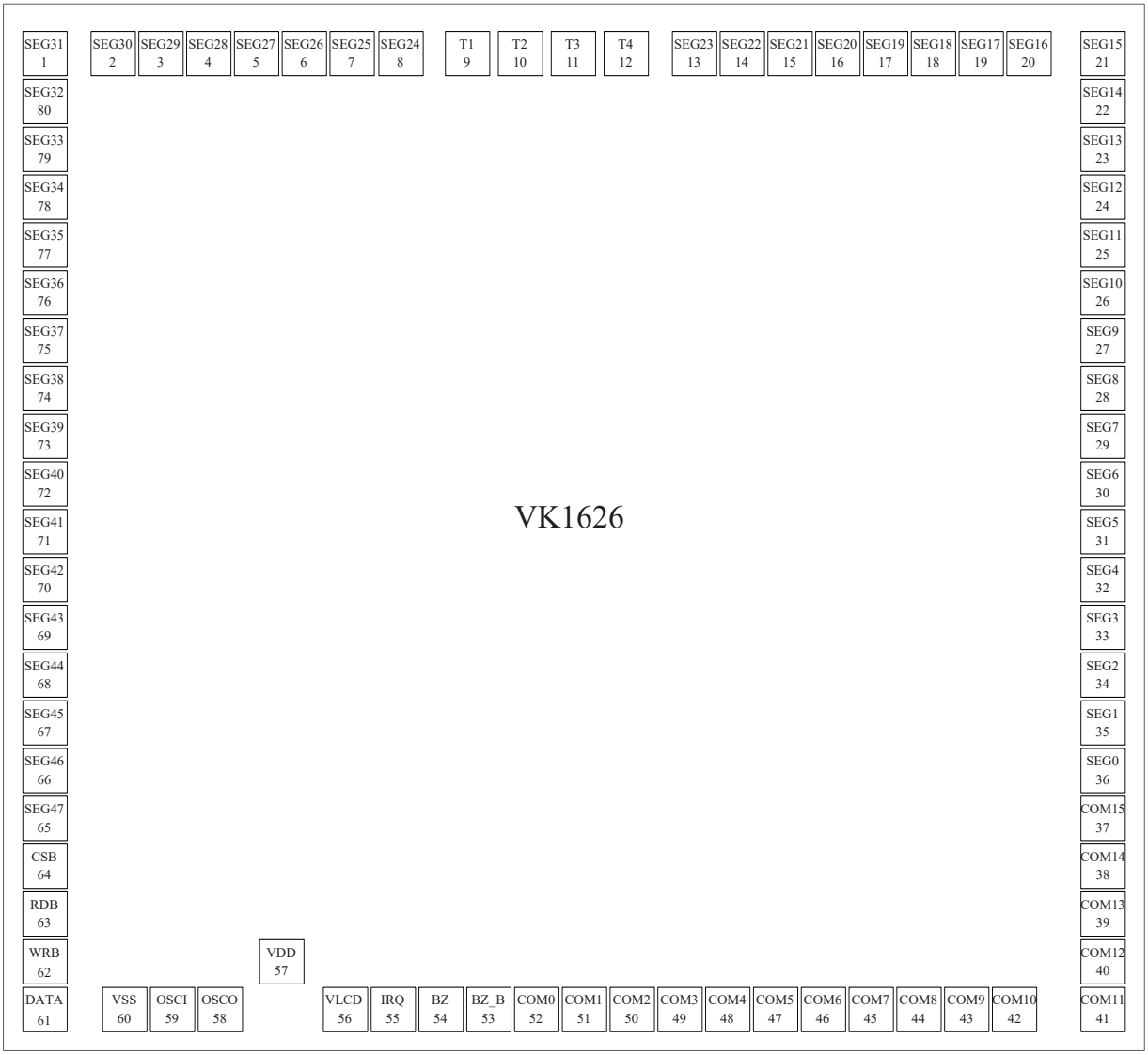
Part No.	VK1620	VK1621S-1	VK1622S-1	VK1623S	VK1625	VK1626
COM	4	4	8	8	8	16
SEG	32	32	32	48	64	48
On-chip Oscillator	-	√	√	√	√	√
Crystal Oscillator	√	√	-	√	√	√
External clock	√	√	√	√	√	√

4 Ordering Information

Part No.	Packaging	Tube Qty	Tray Qty	Box Qty	Total Qty	Notes
VK1620	LQFP64		250/tray	2500/box	15000 PCS	
	DICE		300/tray	1500/box	3000 PCS	DICE
VK1621S-1	LQFP44		160/tray	1600/box	9600 PCS	
	LQFP48		250/tray	2500/box	15000 PCS	
	SSPO48	30/tube		2400/box	24000 PCS	
	DICE		300/tray	1500/box	3000 PCS	DICE
VK1622S-1	LQFP44		160/tray	1600/box	5400 PCS	
	LQFP52		90/tray	900/box	5400 PCS	
	LQFP64		250/tray	2500/box	15000 PCS	
	QFP64		66/tray	660/box	3960 PCS	
	DICE		250/tray	1000/box	2000 PCS	DICE
VK1623S	LQFP100		90/tray	900/box	5400 PCS	
	QFP100		66/tray	660/box	3960 PCS	
	DICE		100/tray	500/box	1000 PCS	DICE
VK1625	LQFP100		90/tray	900/box	5400 PCS	
	QFP100		66/tray	660/box	3960 PCS	
	DICE		100/tray	500/box	1000 PCS	DICE
VK1626	LQFP100		90/tray	900/box	5400 PCS	
	QFP100		66/tray	660/box	3960 PCS	
	DICE		110/tray	550/box	1500 PCS	DICE

5 COB Pad Information

5.1 COB Pad Assignment



Chip Dimensions: 2550×2270 μm ²，Substrate potential: VDD，
Pad size: 80×80 μm，PAD SPACE: 28

5.2 COB PAD Coordinates

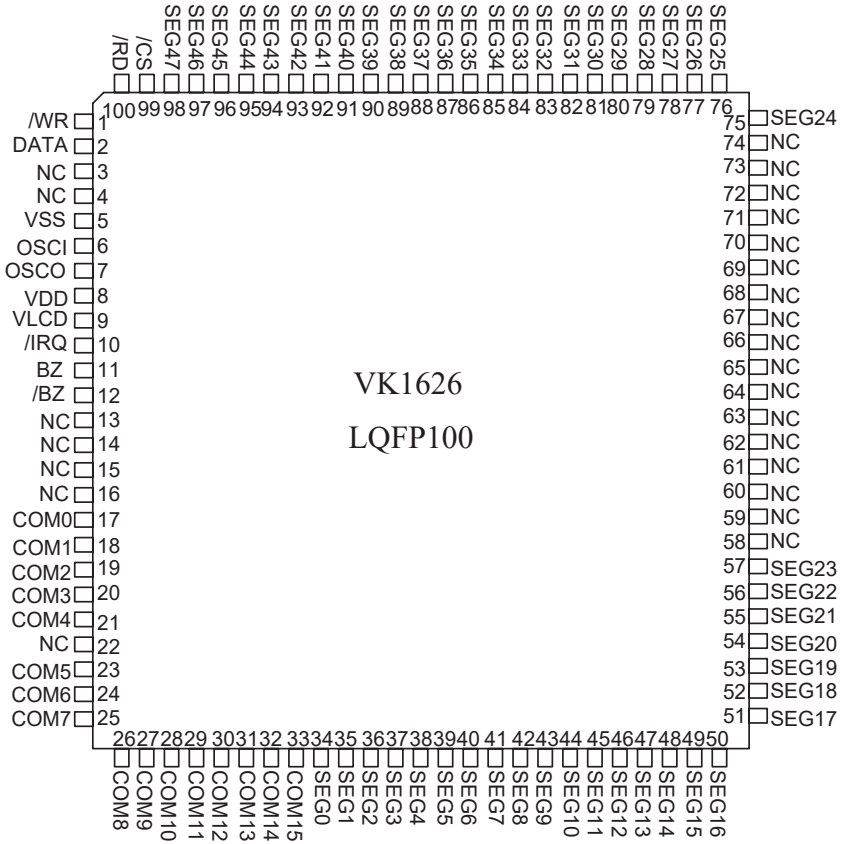
Unit: um

	PAD NAME	PAD SIZE(um^2)	X(Center)um	Y(Center)um	NOTE
1	SEG31	80*80	55	2215	
2	SEG30	80*80	268.3	2215	
3	SEG29	80*80	376.3	2215	
4	SEG28	80*80	484.3	2215	
5	SEG27	80*80	592.3	2215	
6	SEG26	80*80	700.3	2215	
7	SEG25	80*80	808.3	2215	
8	SEG24	80*80	916.3	2215	
9	T1	80*80	1059	2215	test pad
10	T2	80*80	1167	2215	test pad
11	T3	80*80	1275	2215	test pad
12	T4	80*80	1383	2215	test pad
13	SEG23	80*80	1525.7	2215	
14	SEG22	80*80	1633.7	2215	
15	SEG21	80*80	1741.7	2215	
16	SEG20	80*80	1849.7	2215	
17	SEG19	80*80	1957.7	2215	
18	SEG18	80*80	2065.7	2215	
19	SEG17	80*80	2173.7	2215	
20	SEG16	80*80	2281.7	2215	
21	SEG15	80*80	2495	2215	
22	SEG14	80*80	2495	2107	
23	SEG13	80*80	2495	1999	
24	SEG12	80*80	2495	1891	
25	SEG11	80*80	2495	1783	
26	SEG10	80*80	2495	1675	
27	SEG9	80*80	2495	1567	
28	SEG8	80*80	2495	1459	
29	SEG7	80*80	2495	1351	
30	SEG6	80*80	2495	1243	
31	SEG5	80*80	2495	1135	

32	SEG4	80*80	2495	1027	
33	SEG3	80*80	2495	919	
34	SEG2	80*80	2495	811	
35	SEG1	80*80	2495	703	
36	SEG0	80*80	2495	595	
37	COM15	80*80	2495	487	
38	COM14	80*80	2495	379	
39	COM13	80*80	2495	271	
40	COM12	80*80	2495	163	
41	COM11	80*80	2495	55	
42	COM10	80*80	2281.7	55	
43	COM9	80*80	2173.7	55	
44	COM8	80*80	2065.7	55	
45	COM7	80*80	1957.7	55	
46	COM6	80*80	1849.7	55	
47	COM5	80*80	1741.7	55	
48	COM4	80*80	1633.7	55	
49	COM3	80*80	1525.7	55	
50	COM2	80*80	1417.7	55	
51	COM1	80*80	1309.7	55	
52	COM0	80*80	1201.7	55	
53	BZ_B	80*80	1093.7	55	
54	BZ	80*80	985.7	55	
55	IRQ	80*80	877.7	55	
56	VLCD	80*80	769.7	55	
57	VDD	80*80	621.9	143	
58	OSCO	80*80	474.1	55	
59	OSCI	80*80	366.1	55	
60	VSS	80*80	258.1	55	
61	DATA	80*80	55	55	
62	WRB	80*80	55	163	
63	RDB	80*80	55	271	
64	CSB	80*80	55	379	

65	SEG47	80*80	55	487	
66	SEG46	80*80	55	595	
67	SEG45	80*80	55	703	
68	SEG44	80*80	55	811	
69	SEG43	80*80	55	919	
70	SEG42	80*80	55	1027	
71	SEG41	80*80	55	1135	
72	SEG40	80*80	55	1243	
73	SEG39	80*80	55	1351	
74	SEG38	80*80	55	1459	
75	SEG37	80*80	55	1567	
76	SEG36	80*80	55	1675	
77	SEG35	80*80	55	1783	
78	SEG34	80*80	55	1891	
79	SEG33	80*80	55	1999	
80	SEG32	80*80	55	2107	

6 Package Pinout Information(LQFP100)

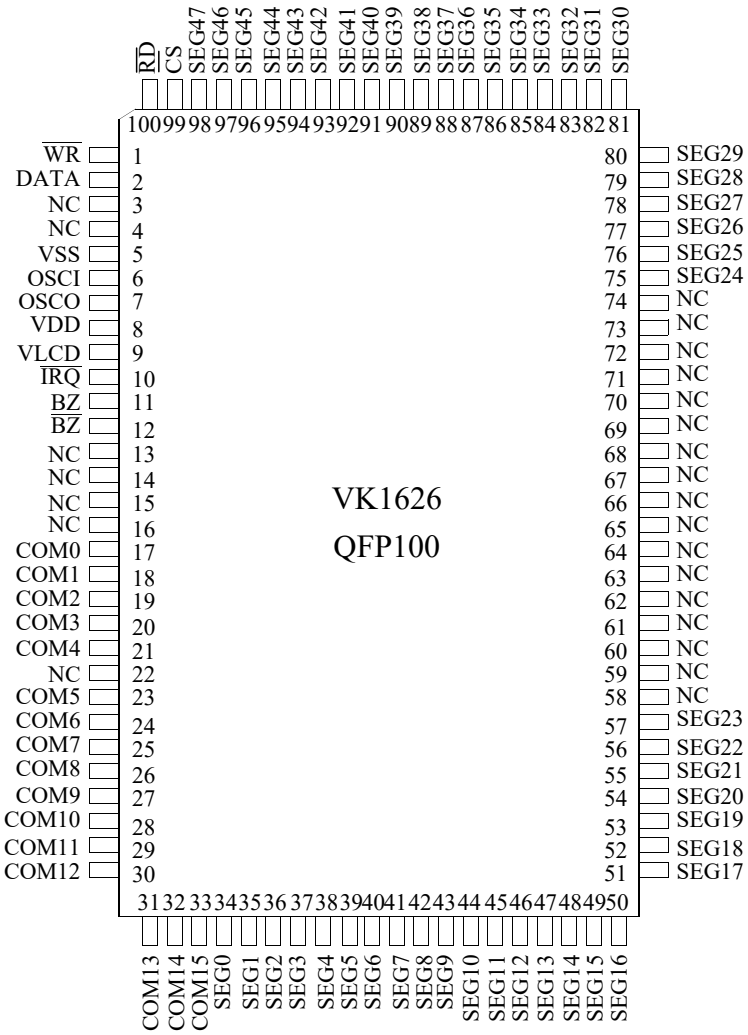


For more information: Page 25

6.1 VK1626/LQFP100 Pin Description

No.	Name	I/O	Function
99	/CS	I	Chip select signal with pull-up resistor ,active low.
100	/RD	I	Serial read signal with pull-up resistor, data out on the falling edge of the /RD signal.
1	/WR	I	Serial write signal with pull-up resistor, data latched on the rising edge of the /WR signal.
2	DATA	I/O	Serial data signal with pull-up resistor, input/output depending on access mode.
5	VSS	VSS	Negative power supply
6	OSCI	I	Crystal oscillator: OSCI and OSCO pins are connected to a 32.768kHz crystal External clock source: OSCI pin is connected to a, external clock source On-chip RC oscillator: the OSCI and OSCO pins can be left open.
7	OSCO	O	
8	VDD	VDD	Positive power supply
9	VLCD	I	LCD driving voltage input,must be ≤VDD
10	/IRQ	O	Time base or WDT overflow flag, NMOS open drain output.
11	BZ	O	2kHz or 4kHz tone frequency output， when TONE OFF the /BZ pin output low level.
12	/BZ	O	
13-16	NC	—	——
17-21 23-33	COM0-COM15	O	LCD COM drive outputs
34-57 75-98	SEG0-SEG47	O	LCD SEG drive outputs

7 Package Pinout Information(QFP100)



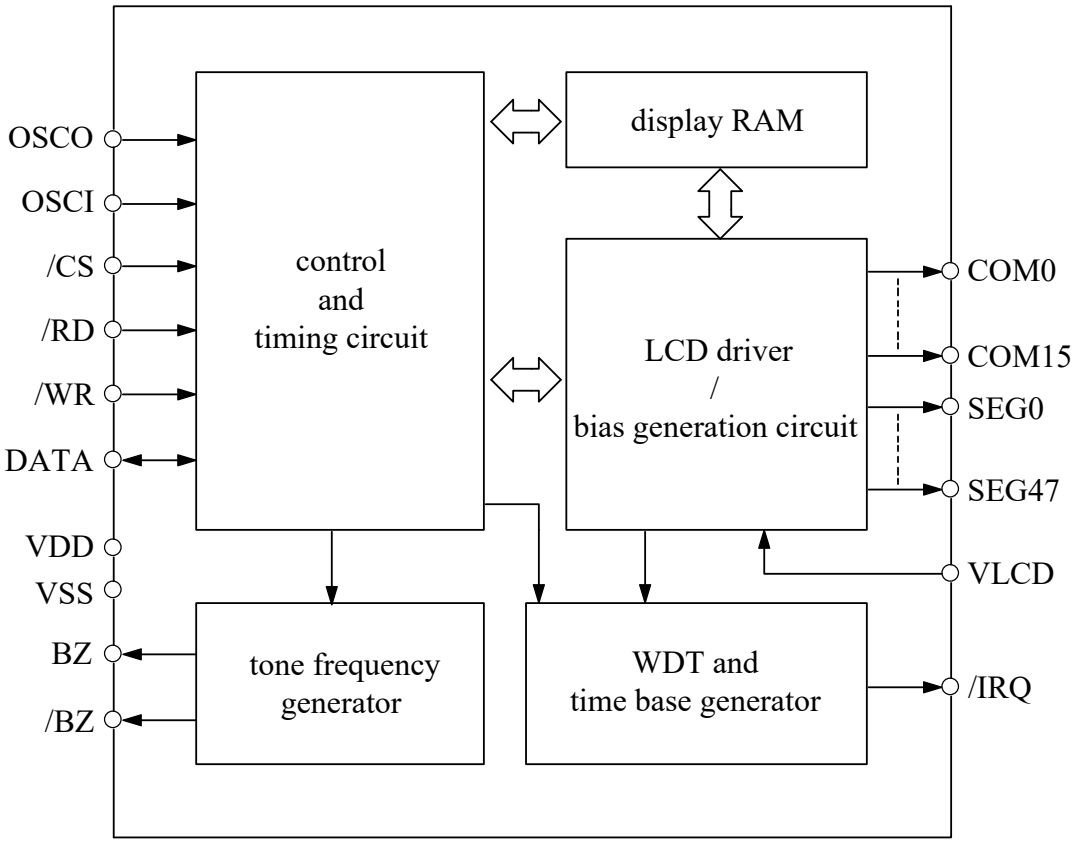
For more information: Page 26

7.1 VK1626/QFP100 Pin Description

No.	Name	I/O	Function
99	/CS	I	Chip select signal with pull-up resistor ,active low.
100	/RD	I	Serial read signal with pull-up resistor, data out on the falling edge of the /RD signal.
1	/WR	I	Serial write signal with pull-up resistor, data latched on the rising edge of the /WR signal.
2	DATA	I/O	Serial data signal with pull-up resistor, input/output depending on access mode.
5	VSS	VSS	Negative power supply
6	OSCI	I	Crystal oscillator: OSCI and OSCO pins are connected to a 32.768kHz crystal External clock source: OSCI pin is connected to a, external clock source On-chip RC oscillator: the OSCI and OSCO pins can be left open.
7	OSCO	O	
8	VDD	VDD	Positive power supply
9	VLCD	I	LCD driving voltage input,must be ≤VDD
10	/IRQ	O	Time base or WDT overflow flag, NMOS open drain output.
11	BZ	O	2kHz or 4kHz tone frequency output， when TONE OFF the /BZ pin output low level.
12	/BZ	O	
13-16	NC	—	——
17-21 23-33	COM0-COM15	O	LCD COM drive outputs
34-57 75-98	SEG0-SEG47	O	LCD SEG drive outputs

8 Functional Description

8.1 Block Diagram



8.2 Display RAM

The VK1626 integrates 48 × 16-bit RAM for LCD display. directly mapped to SEGx/COMx segments. Data is latched and updated on the LCD according to scan timing set by the system configuration. The display RAM can be accessed using three commands: READ, WRITE, and READ-MODIFY-WRITE. Each RAM address corresponds to a specific combination of SEG and COM lines.

The following is a mapping from the RAM to the LCD pattern:

	COM15	COM14	COM13	COM12			COM3	COM2	COM1	COM0		
SEG0					3						0	
SEG1					7						4	
SEG2					11						8	address 8 bits
SEG3					15	----					12	(A7----A0)
⋮					⋮						⋮	
SEG47					191						188	
	D3	D2	D1	D0	Data\Addr		D3	D2	D1	D0	Data\Addr	

4-bits data
（D3,D2,D1,D0）

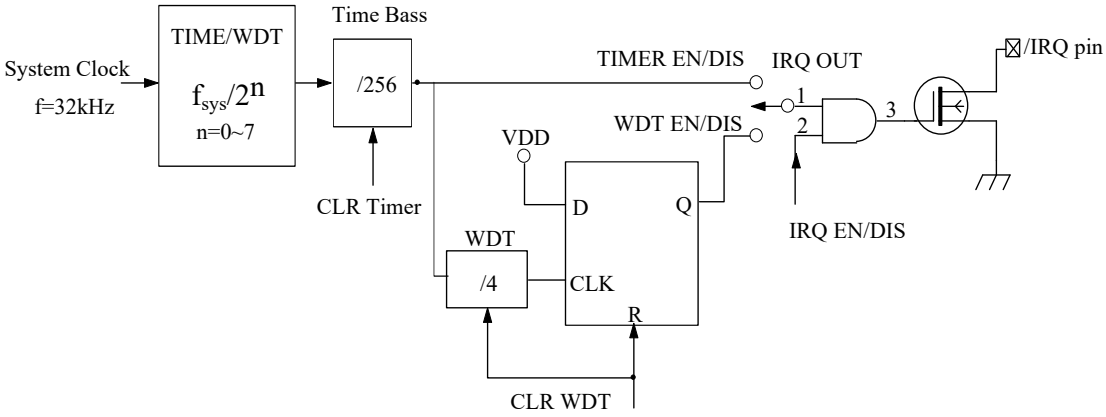
8.3 Time Base and WDT

The time base generator consists of an 8-stage ripple counter and provides accurate timing functionality. The Watchdog Timer (WDT) comprises the 8-stage time base plus an additional 2-stage counter. It helps reset or interrupt the host system in case of abnormal operation, such as unexpected jumps or execution errors. A WDT timeout sets an internal status flag. Both the time base overflow and WDT timeout flags can be routed to the /IRQ pin through software configuration. Eight frequency division options are available for the time base and WDT clock, derived using the formula:

$$f_{WDT}=fsys/2^{n} \quad (n=0\sim7) \quad fsys=32kHz$$

The time base generator and the Watchdog Timer (WDT) share the same 8-stage counter. The WDT is cleared by executing the CLR WDT command, while the time base generator can be cleared using either the CLR WDT or the CLR TIMER command. Executing the WDT EN command enables both the time base generator and the WDT timeout flag output, which can be routed to the /IRQ pin. Conversely, executing the WDT DIS command disables the time base generator. After the TIMER EN command is issued, the WDT is disconnected from the /IRQ pin, and the time base overflow signal is instead connected to it. The /IRQ output can be globally enabled or disabled using the IRQ EN and IRQ DIS commands, respectively.
By default, the /IRQ output is disabled upon system power-up.

Timer and WDT Configurations：



8.4 Tone Output

The VK1626 integrates a basic tone generator capable of producing 2 kHz or 4 kHz output signals. The output consists of a differential pair: BZ and /BZ, designed to drive a passive piezoelectric buzzer. Use the TONE 2K or TONE 4K commands to select the desired tone frequency. Tone output can be enabled or disabled via the TONE ON or TONE OFF commands. When the tone function is disabled or the system is powered down, both BZ and /BZ will remain at low level.

8.5 LCD Driver

The VK1626 is a 768-segment LCD driver (48 SEG × 16 COM). It supports software configurable bias settings of 1/5, and COM configurations of 16.

8.6 Communication Interfacing

The VK1626 communicates with the host via a 3-wire or 4-wire serial interface.

When used solely for display output, only 3 lines are required (/CS, /WR, and DATA); /RD is optional for reading.

- /CS: Chip select input. It enables the serial interface when low and terminates communication when high.
- /RD: Read clock input. On the falling edge, data is output from the device onto the DATA line.
- /WR: Write clock input. On the rising edge, data and commands from DATA are latched into the device.
- DATA: Bidirectional serial data line used to transfer both command and display data.
- /IRQ: Open-drain output pin for either WDT timeout or time base overflow flag, selectable via software.

8.7 Command Format

The VK1626 is configured via software commands that support two primary modes: command mode and data mode.

- Command mode is used to configure system-level parameters. It is identified by a command mode ID of 100.
- Data mode supports three types of memory operations: READ, WRITE, and READ-MODIFY-WRITE.

These commands allow the host controller to configure LCD behavior and access display RAM contents.

The following are the data mode IDs and the command mode ID:

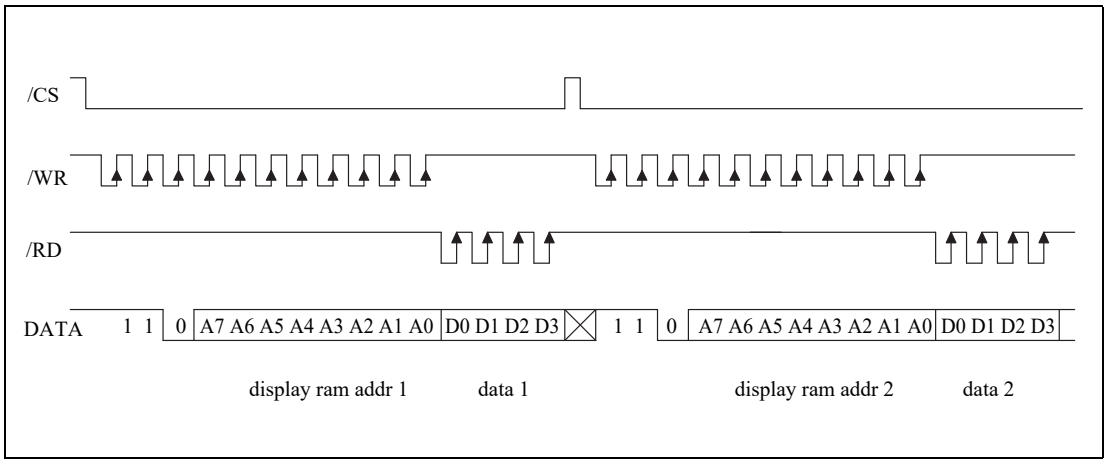
Command	MODE	ID
READ	DATA	110
WRITE	DATA	101
Read-Modify-Write	DATA	101
COMMAND	COMMAND	100

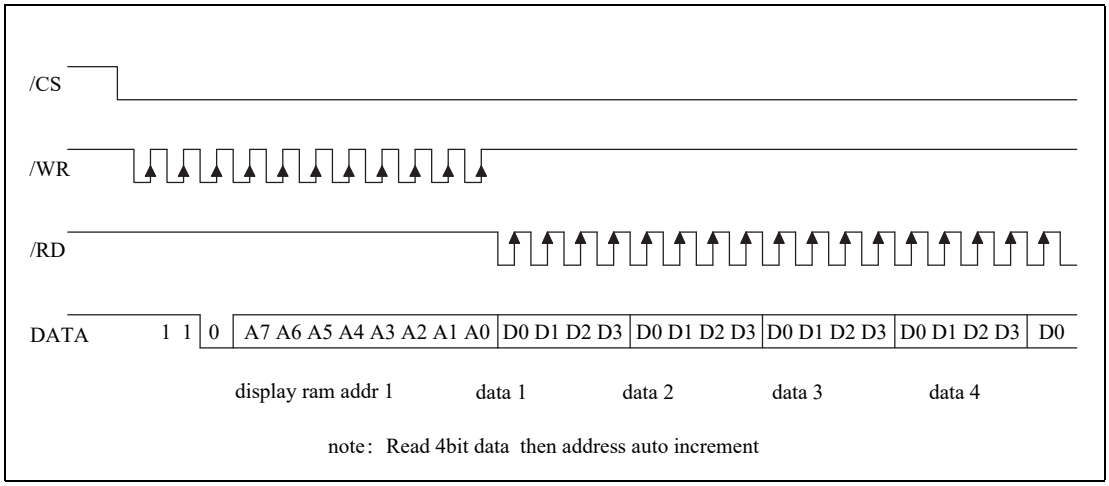
9 Cmd/Data Timing Diagram

The following are the data mode IDs and the command mode ID Timing Diagrams.

9.1 READ Mode

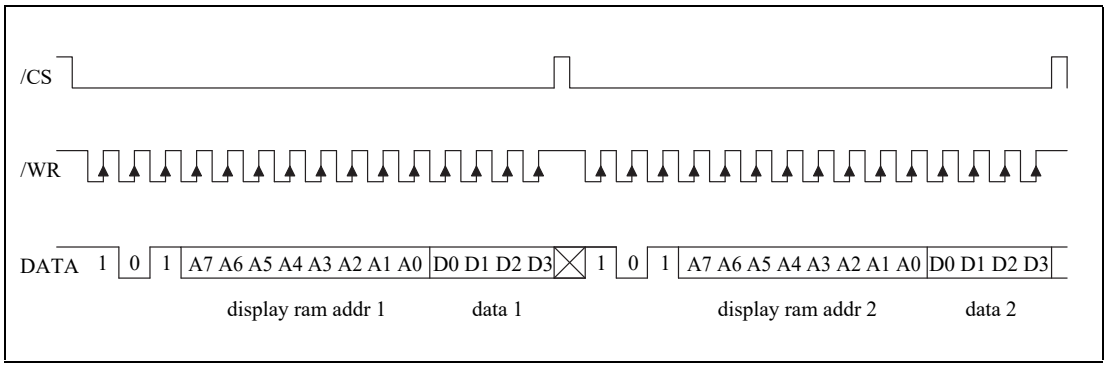
Command Code : 110



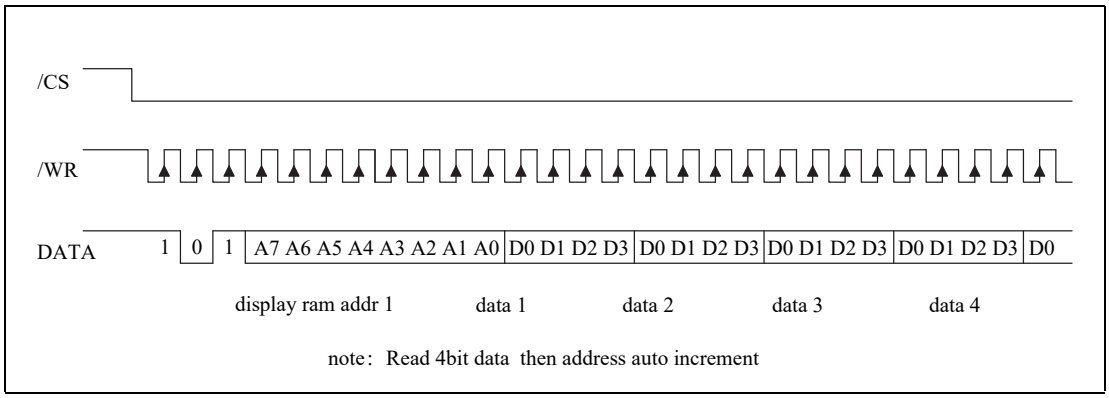


9.2 WRITE Mode

Command Code : 101

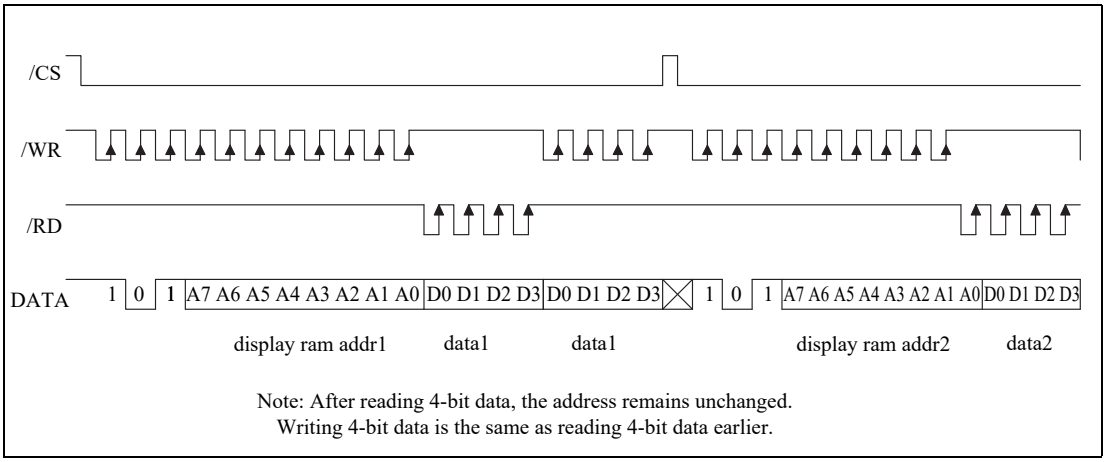


Successive Address Writing



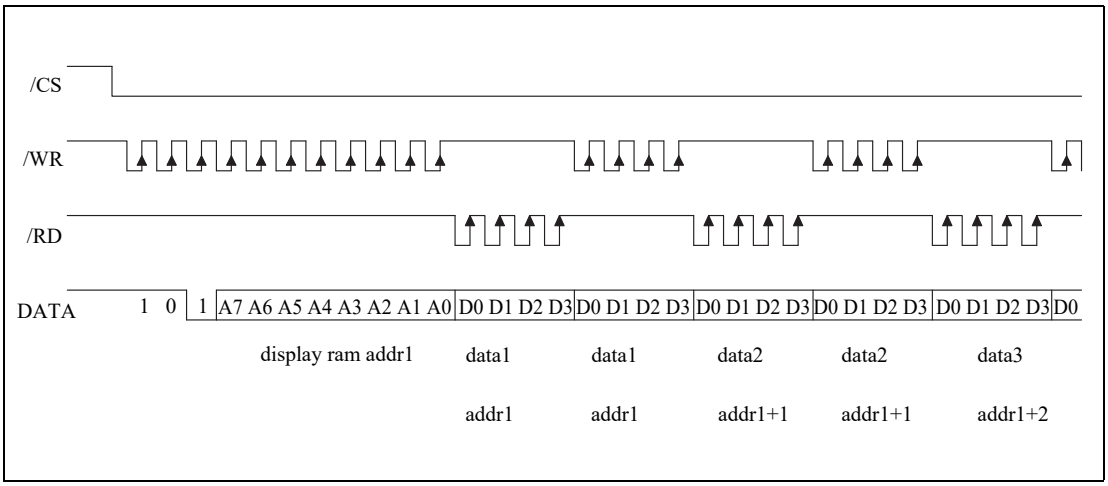
9.3 Read-Modify-Write Mode

Command Code : 101



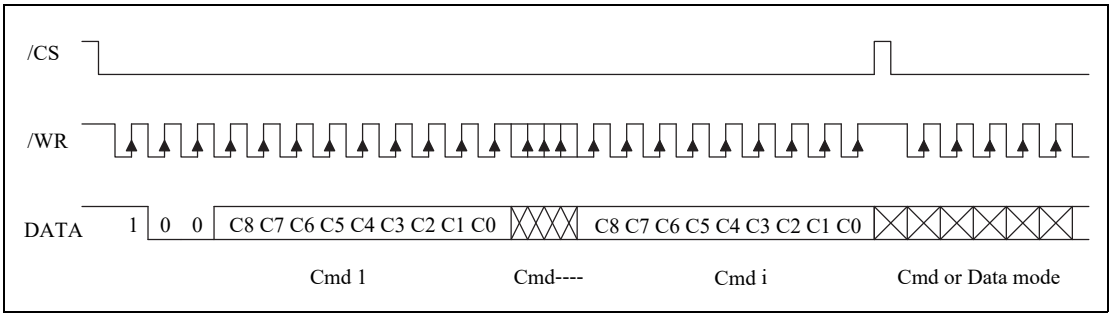
Note: After reading 4-bit data, the address remains unchanged.
Writing 4-bit data is the same as reading 4-bit data earlier.

Successive Address Accessing



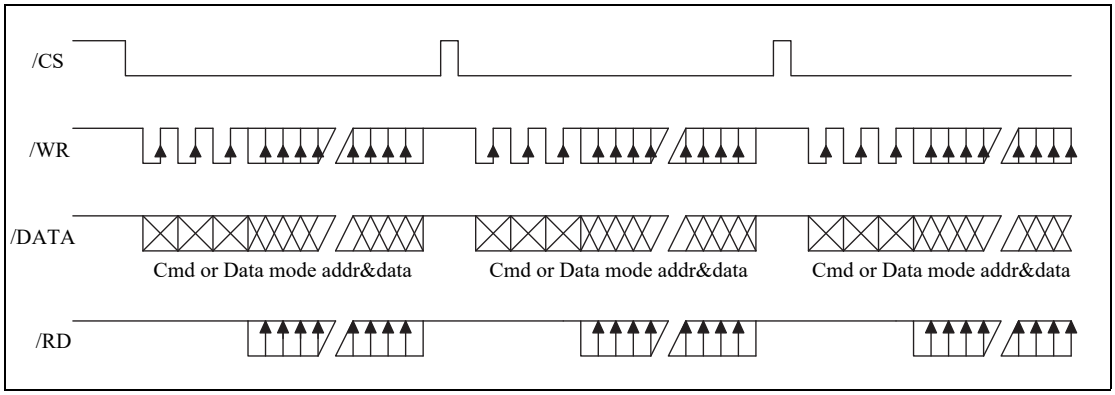
9.4 Command Mode

Command Code : 100



9.5 Data and Command Mode

Data and Command Mode



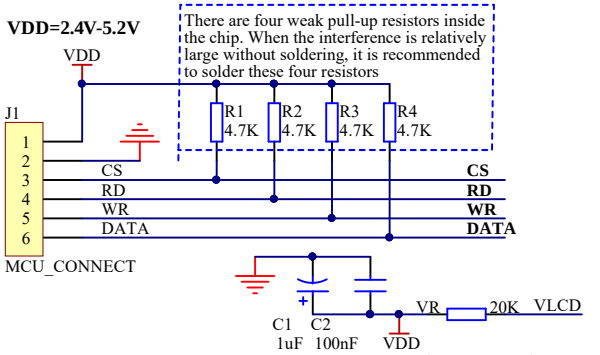
10 Command Summary

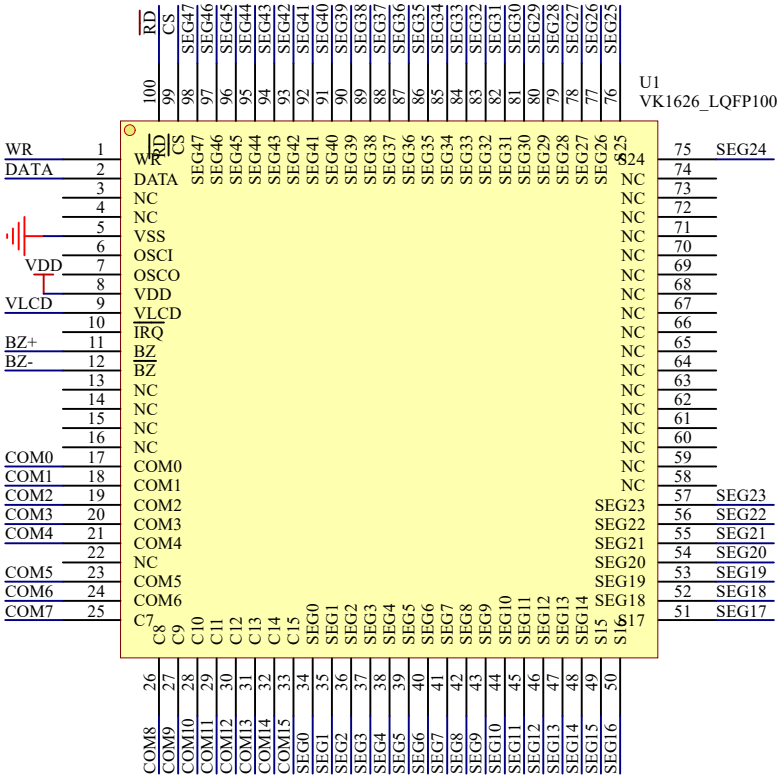
Name	ID	Command Code	D/C	Function	Def.
READ	110	A7A6A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	101	A7A6A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	101	A7A6A5A4A3A2A1A0D0D1D2D3	D	READ and WRITE to the RAM	
SYS DIS	100	0000-0000-X	C	Turn off both system oscillator	YES
SYS EN	100	0000-0001-X	C	Turn on system oscillator	
LCD OFF	100	0000-0010-X	C	Turn off LCD bias generator	YES
LCD ON	100	0000-0011-X	C	Turn on LCD bias generator	
TIMERS DIS	100	0000-0100-X	C	Disable time base output	
WDT DIS	100	0000-0101-X	C	Disable WDT time-out flag output	
TIMER EN	100	0000-0110-X	C	Enable time base output	
WDT EN	100	0000-0111-X	C	Enable WDT time-out flag output	
TONE OFF	100	0000-1000-X	C	Turn off tone outputs	YES
CLR TIMER	100	0000-11XX-X	C	Clear the contents of time base generator	
CLR WDT	100	0000-111X-X	C	Clear the contents of WDT stage	
RC32K	100	0001-10XX-X	C	on-chip RC oscillator	YES
EXT 32k	100	0001-11XX-X	C	external clock source	
TONE 4k	100	010X-XXXX-X	C	Tone frequency, 4kHz	
TONE 2k	100	011X-XXXX-X	C	Tone frequency, 2kHz	
IRQ DIS	100	100X-0XXX-X	C	Disable IRQ output	YES
IRQ EN	100	100X-1XXX-X	C	Enable IRQ output	
F1	100	101X-X000-X	C	Time base/WDT clock output:1Hz The WDT time-out flag after: 4s	
F2	100	101X-X001-X	C	Time base/WDT clock output:2Hz The WDT time-out flag after: 2s	
F4	100	101X-X010-X	C	Time base/WDT clock output:4Hz The WDT time-out flag after: 1s	
F8	100	101X-X011-X	C	Time base/WDT clock output:8Hz The WDT time-out flag after: 1/2s	
F16	100	101X-X100-X	C	Time base/WDT clock output:16Hz The WDT time-out flag after: 1/4s	
F32	100	101X-X101-X	C	Time base/WDT clock output:16Hz The WDT time-out flag after: 1/4s	
F64	100	101X-X110-X	C	Time base/WDT clock output:64Hz The WDT time-out flag after: 1/16s	
F128	100	101X-X111-X	C	Time base/WDT clock output:128Hz The WDT time-out flag after: 1/32s	YES
TEST	100	1110-0000- X	C	Test mode	
NORMAL	100	1110-0011- X	C	Normal mode	YES

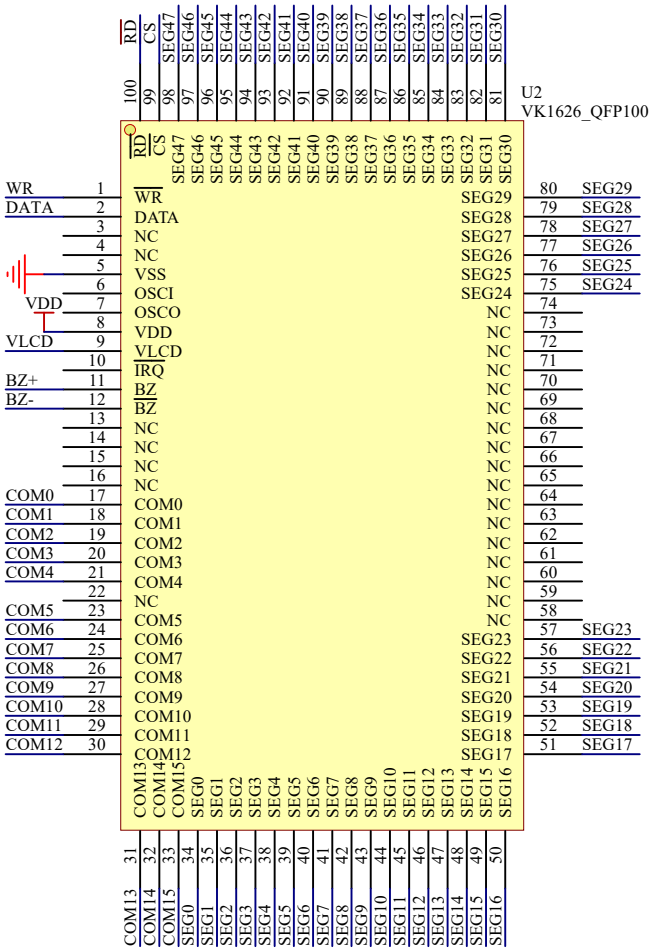
note: X: 0 or 1 D/C:Data/Command mode
A7-A0: Display RAM addresses Def.:Power on reset default
D3-D0:4bit Display RAM data 110,101and 100 is Command ID

11 Application Circuits

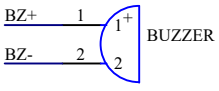
When the LCD only displays, the RD pin can be left floating and not connected
When the surrounding interference is relatively large, a 10R to 1k resistor and a small PF-level capacitor to ground can be connected in series on the communication pin
When the power supply of the chip machine (3.3V) and the driver chip (5V) is inconsistent, it is recommended to add a level conversion circuit to the communication pin



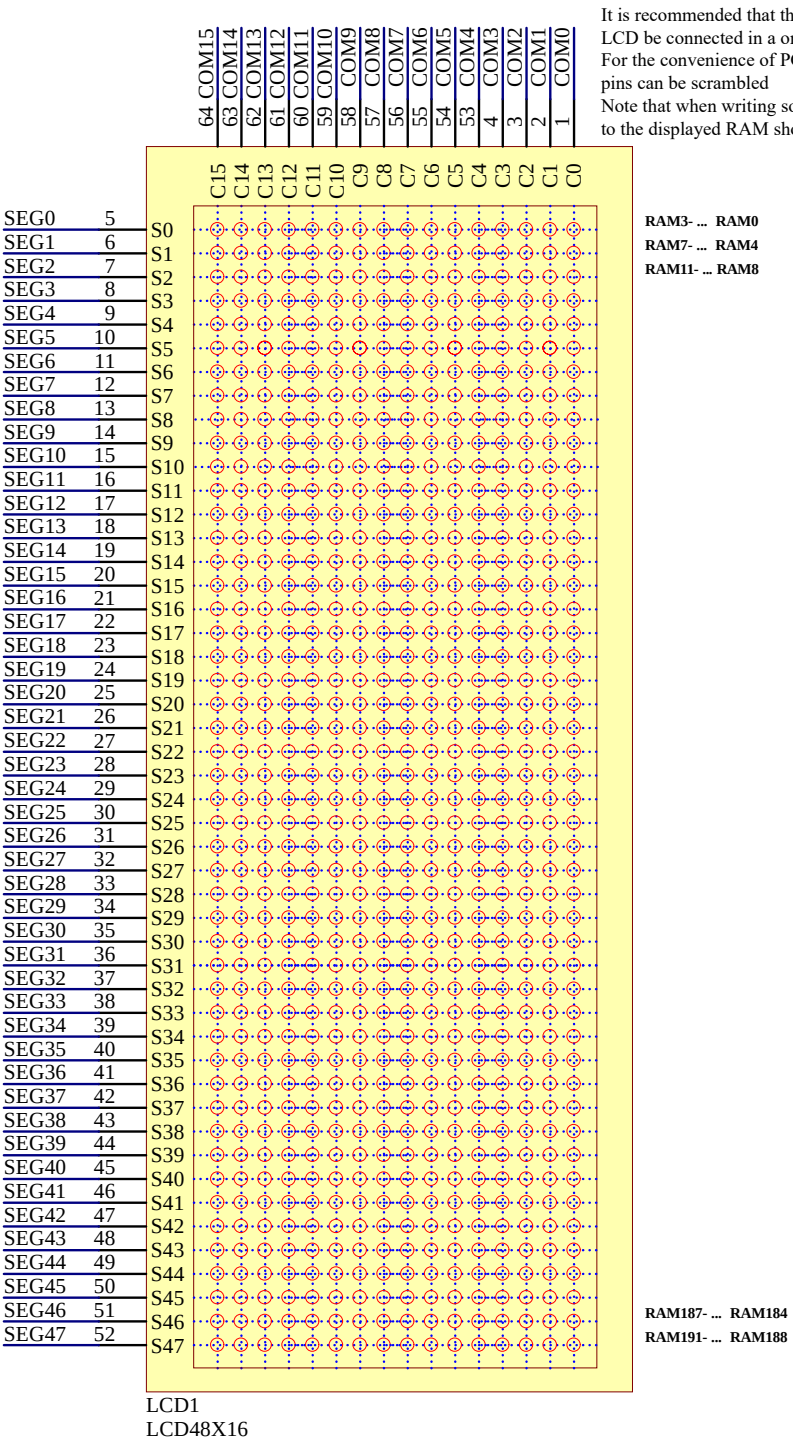




Passive buzzer drive current <1mA circuit LCD



The buzzer frequency is 2kHz or 4kHz, and the buzzer voltage is no more than 5V



It is recommended that the COM pins of the chip and the LCD be connected in a one-to-one sequence
For the convenience of PCB routing, the order of the SEG pins can be scrambled
Note that when writing software, the sequence corresponding to the displayed RAM should also be changed

12 Electrical Characteristics

12.1 Absolute Maximum Ratings

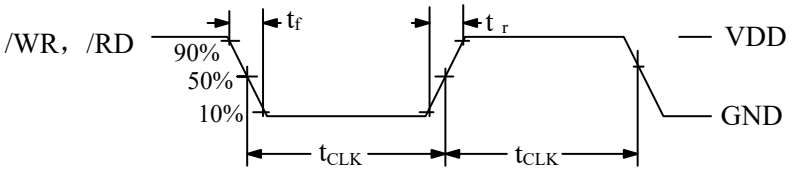
Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3～5.5	V
Input Voltage	VIN	V_{SS}-0.3～V_{DD}+0.3	V
Storage Temperature	T_{STG}	-50～+125	℃
Operating Temperature	T_{OTG}	-40～+85	℃

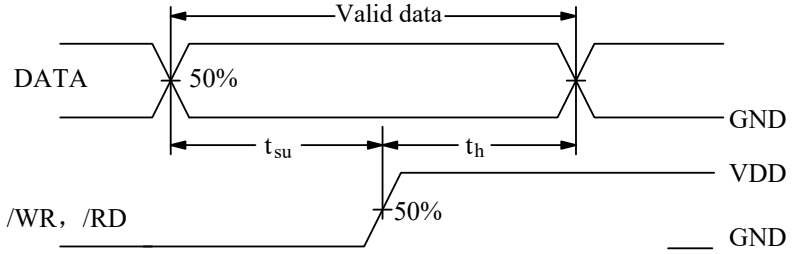
12.2 DC Electrical Characteristics

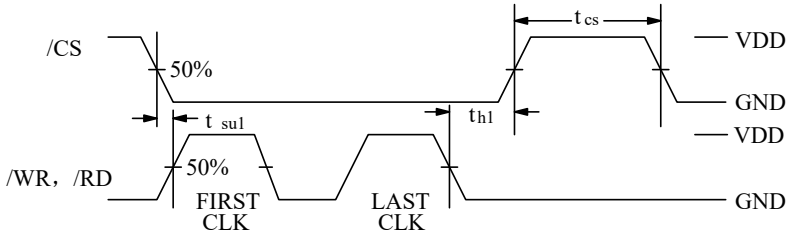
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	2.4	—	5.2	V	—	—
Operating current	I_{DD1}	—	155	310	μA	3V	No load/LCD ON On-chip RC oscillator
		—	260	420		5V	
Operating current	I_{DD2}	—	150	310	μA	3V	No load/LCD ON External crystal
		—	250	420		5V	
Operating current	I_{DD11}	—	8	30	μA	3V	No load/LCD OFF On-chip RC oscillator
		—	20	60		5V	
Operating current	I_{DD22}	—	—	20	μA	3V	No load/LCD OFF External crystal
		—	—	35		5V	
Standby Current	I_{STB}	—	1	10	μA	3V	No load, Power down mode
		—	2	20		5V	
Low-level Input	V_{IL}	0	—	0.6	V	3V	DATA, /WR, /CS,/RD
		0	—	1.0		5V	
High-level Input	V_{IH}	2.4	—	3.0	V	3V	DATA, /WR, /CS,/RD
		4.0	—	5.0		5V	
BZ, /BZ, /IRQ	I_{OL1}	0.9	1.8	—	mA	3V	V_{OL}=0.3V
		1.7	3.0	—		5V	V_{OL}=0.5V
BZ, /BZ	I_{OH1}	-0.9	-1.8	—	mA	3V	V_{OH}=2.7V
		-1.7	-3.0	—		5V	V_{OH}=4.5V
DATA	I_{OH1}	0.9	1.8	—	mA	3V	V_{OL}=0.3V
		1.7	3.0	—		5V	V_{OL}=0.5V
DATA	I_{OH1}	-0.9	-1.8	—	mA	3V	V_{OH}=2.7V
		-1.7	-3.0	—		5V	V_{OH}=4.5V
LCD COM Sink Current	I_{OL2}	80	160	—	μA	3V	V_{OL}=0.3V
		180	360	—		5V	V_{OL}=0.5V
LCD COM Source Current	I_{OH2}	-40	-80	—	μA	3V	V_{OH}=2.7V
		-90	-180	—		5V	V_{OH}=4.5V
LCD SEG Sink Current	I_{OL3}	50	100	—	μA	3V	V_{OL}=0.3V
		120	240	—		5V	V_{OL}=0.5V
LCD SEG Source Current	I_{OH3}	-30	-60	—	μA	3V	V_{OH}=2.7V
		-70	-140	—		5V	V_{OH}=4.5V
Pull-UP Resistor	R_{UP}	100	200	300	kΩ	3V	DATA, /WR, /CS,/RD
		50	100	150		5V	

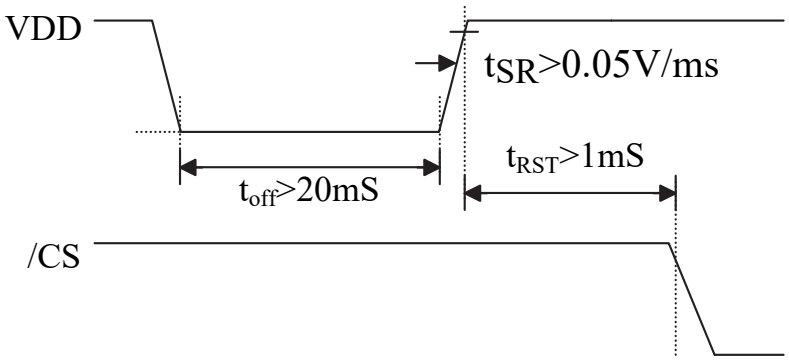
12.3 AC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
System Clock	f_{SYS1}	22	32	40	kHz	3V	On-chip
		24	32	40		5V	RC oscillator
System Clock	f_{SYS2}	—	32	—	kHz	3V	External
		—	32	—		5V	clock source
LCD Clock	f_{LCD1}	44	64	80	Hz	3V	On-chip
		48	64	80	Hz	5V	RC oscillator
	f_{LCD2}	—	64	—	Hz	3V	External clock (32kHz)
		—	64	—	Hz	5V	
LCD Common Period	t_{COM}	—	n/ f_{LCD}	—	sec	—	N：Number of COM
Serial Data Clock(/WR)	F_{CLK1}	—	—	150	kHz	3V	Duty cycle 50%
		—	—	300		5V	
Serial Data Clock(/RD)	F_{CLK2}	—	—	75	kHz	3V	Duty cycle 50%
		—	—	150		5V	
Serial Interface Reset PW	t_{CS}	—	250	—	ns	—	/CS
/WR, /RD Input Pulse Width	t_{CLK}	3.34	—	—	µS	3V	Write mode
		6.67	—	—			Read mode
		1.67	—	—	µS	5V	Write mode
		3.34	—	—			Read mode
Rise/Fall Time Serial Data Clock Width	t_r，t_f	—	120	—	ns	3V	—
						5V	
Setup Time for DATA to /WR, /RD Clock Width	t_{su}	—	120	—	ns	3V	—
						5V	
Hold Time for DATA to /WR, /RD Clock Width	t_h	—	120	—	ns	3V	—
						5V	
Setup Time for /CS to /WR, /RD Clock Width	t_{su1}	—	100	—	ns	3V	—
						5V	
Hold Time for /CS to /WR, /RD Clock Width	t_{h1}	—	100	—	ns	3V	—
						5V	


/WR，/RD
90%
50%
10%
tf
t r
VDD
GND
tCLK
tCLK

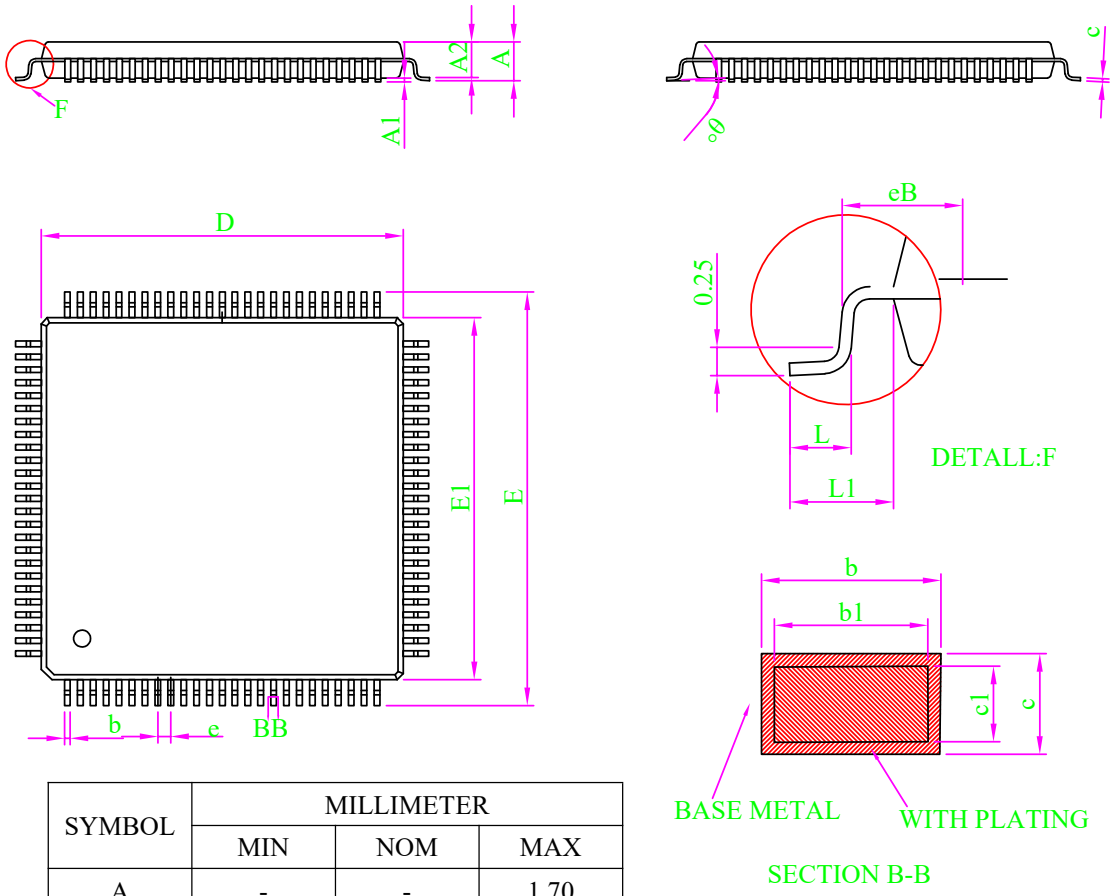

Valid data
DATA
50%
GND
tsu
th
VDD
/WR，/RD
50%
GND


/CS
50%
t cs
VDD
GND
t su1
th1
VDD
/WR，/RD
50%
FIRST CLK
LAST CLK
GND


VDD
tSR>0.05V/ms
tRST>1mS
toff>20mS
/CS

13 Package Information

13.1 LQFP100(14.0mm × 14.0mm PP=0.5mm)

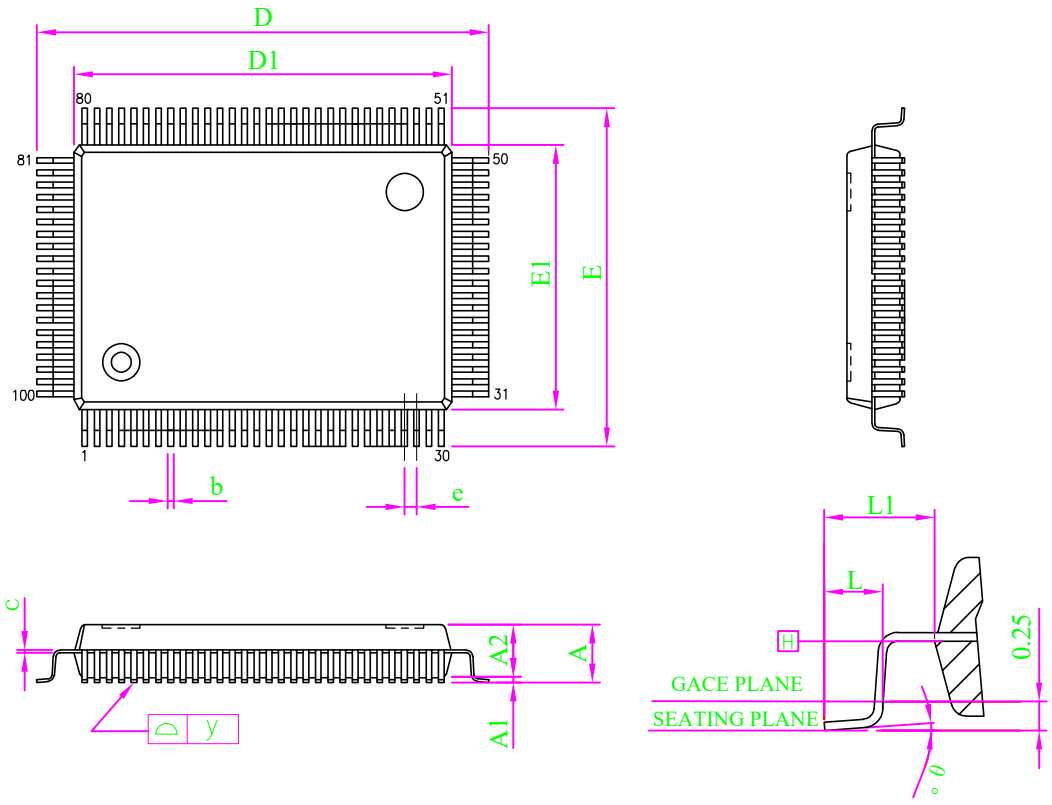


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.70
A1	0.10	0.15	0.20
A2	1.30	1.40	1.50
b	0.17	-	0.27
b1	0.16	0.20	0.24
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
eB	15.05	-	15.40
e	0.50BSC		
L	0.42	0.57	0.72
L1	0.95	1.00	1.15
θ	0	-	10°

Note:

1. All dimension are in mm.
2. Dim D&El does not include plastic flash; Flash: Plastic residual around body edge after de junk/singulation.
3. Dim b does not include dambar protrusion/intrusion.
4. Plating thickness 0.007mm-0.015mm

13.2 QFP100(20.0mm × 14.0mm PP=0.65mm)



SYMBOL	MIN	NOMINAL	MAX
A	—	—	3.40
A1	0.25	—	0.50
A2	2.57	2.72	2.87
b	—	0.30	—
c	0.10	0.15	0.20
D	23.65	23.90	24.15
D1	19.90	20.00	20.10
e	—	0.65	—
E	17.65	17.90	18.15
E1	13.90	14.00	14.10
L	0.65	0.80	0.95
L1	—	1.95	—
y	—	—	0.10
θ°	0	—	7

UNIT:mm

NOTES:

1.JEDEC OUTLINE:MO-112 CC-1

2.DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THW BODY.

3.DIMENSIONS D1 AND E1 D0 NOT INCLUDE MOLD PROTRUSION, ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 D0 NOT INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

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15 Revision History

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	initial release	YES
2	1.1	2018-10-11	Add reference circuit	YES
3	1.2	2019-03-21	Alignment correction	YES
4	1.3	2025-06-12	Change Description	YES

[1] Please refer to the latest version of this document before starting or finalizing any design.

[2] Since the release of this document, the status or availability of this product may have changed. For the most up-to-date information, please visit: https://www.szvinka.com/