永嘉微电
Vinka Microelectronics

VK1623S Datasheet

48×8 LCD DRIVER

Rev.1.3

1 General Description

The VK1623S is a RAM-mapped LCD segment driver capable of supporting up to 384 segments (48 SEG × 8 COM).
The device communication via a 3-wire or 4-wire serial interface, which is used for display parameter configuration, data transmission, and Power-down control.

2 Key Features

- Operating voltage:2.4-5.2V
- Integrated RC oscillator (default)
- External crystal input: 32.768 kHz (OSCO, OSCI)
- Selectable LCD bias:1/4
- Selectable LCD duty:1/8
- Built-in 48 × 8-bit display RAM
- Configurable buzzer output: 2 kHz or 4 kHz
- Power-down mode via software command(LCD OFF, SYS DIS)
- Eight selectable clock sources for time base / WDT
- WDT or time base overflow flag output via /IRQ pin
- 3 wire or 4 wire serial communication interface
- Software-configurable of LCD parameters
- Dual command formats for configuration and access
- Auto-increment addressing for sequential read/write
- Three RAM accessing modes
- VLCD adjustable via external pin (≤ VDD)
- Available Packages:
  LQFP100(14.0mm × 14.0mm PP=0.5mm)
  QFP100(20.0mm × 14.0mm PP=0.65mm)
  DICE
  COG

3 Product Selection

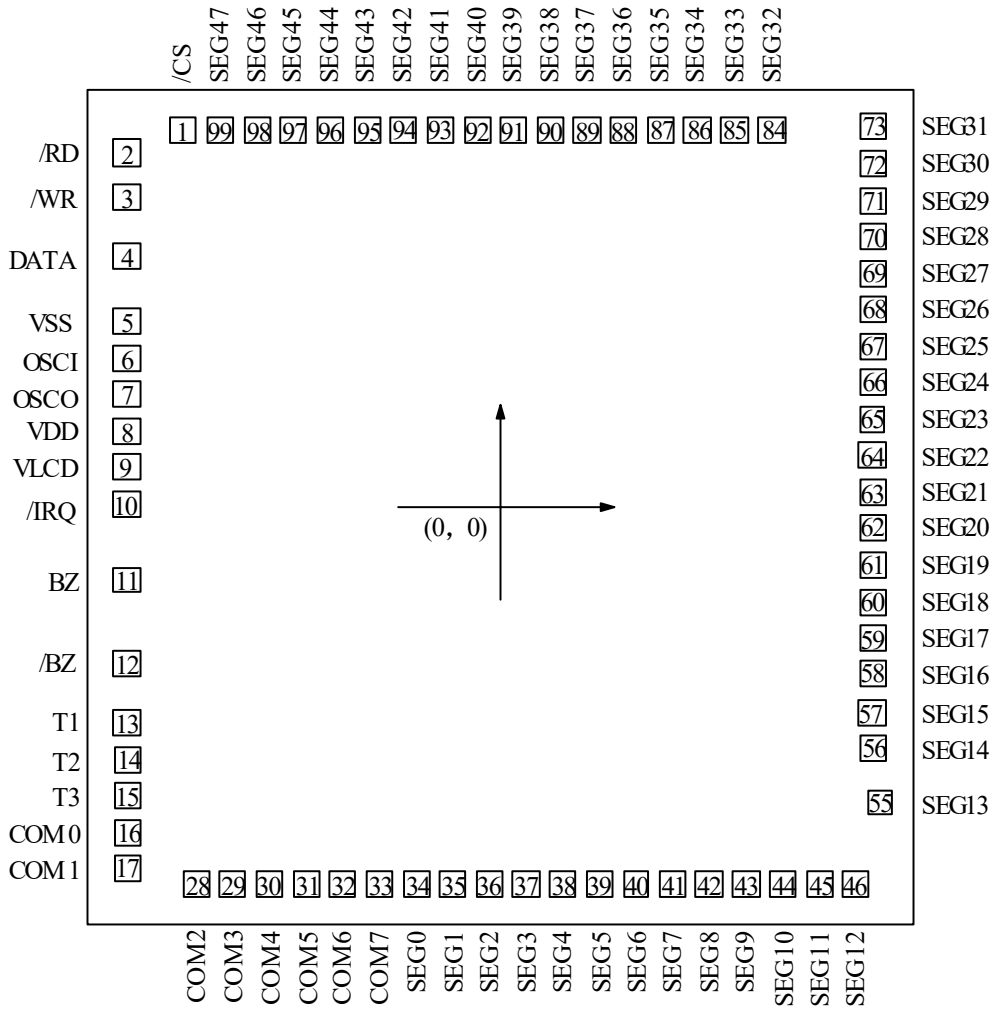
Part No.	VK1620	VK1621S-1	VK1622S-1	VK1623S	VK1625	VK1626
COM	4	4	8	8	8	16
SEG	32	32	32	48	64	48
On-chip Oscillator	-	√	√	√	√	√
Crystal Oscillator	√	√	-	√	√	√
External clock	√	√	√	√	√	√

4 Ordering Information

Part No.	Packaging	Tube Qty	Tray Qty	Box Qty	Total Qty	Notes
VK1620	LQFP64		250/tray	2500/box	15000 PCS	
	DICE		300/tray	1500/box	3000 PCS	DICE
VK1621S-1	LQFP44		160/tray	1600/box	9600 PCS	
	LQFP48		250/tray	2500/box	15000 PCS	
	SSPO48	30/tube		2400/box	24000 PCS	
	DICE		300/tray	1500/box	3000 PCS	DICE
VK1622S-1	LQFP44		160/tray	1600/box	5400 PCS	
	LQFP52		90/tray	900/box	5400 PCS	
	LQFP64		250/tray	2500/box	15000 PCS	
	QFP64		66/tray	660/box	3960 PCS	
	DICE		250/tray	1000/box	2000 PCS	DICE
VK1623S	LQFP100		90/tray	900/box	5400 PCS	
	QFP100		66/tray	660/box	3960 PCS	
	DICE		100/tray	500/box	1000 PCS	DICE
VK1625	LQFP100		90/tray	900/box	5400 PCS	
	QFP100		66/tray	660/box	3960 PCS	
	DICE		100/tray	500/box	1000 PCS	DICE
VK1626	LQFP100		90/tray	900/box	5400 PCS	
	QFP100		66/tray	660/box	3960 PCS	
	DICE		110/tray	550/box	1500 PCS	DICE

5 COB Pad Information

5.1 COB Pad Assignment



Chip Dimensions: 2730×2730 μm², substrate potential: VDD

Pad size: 90×90 μm, Pad spacing: 112 μm,

Al Pad size: 100×100μm, Al pad thickness: 1μm,

5.2 COB PAD Coordinates

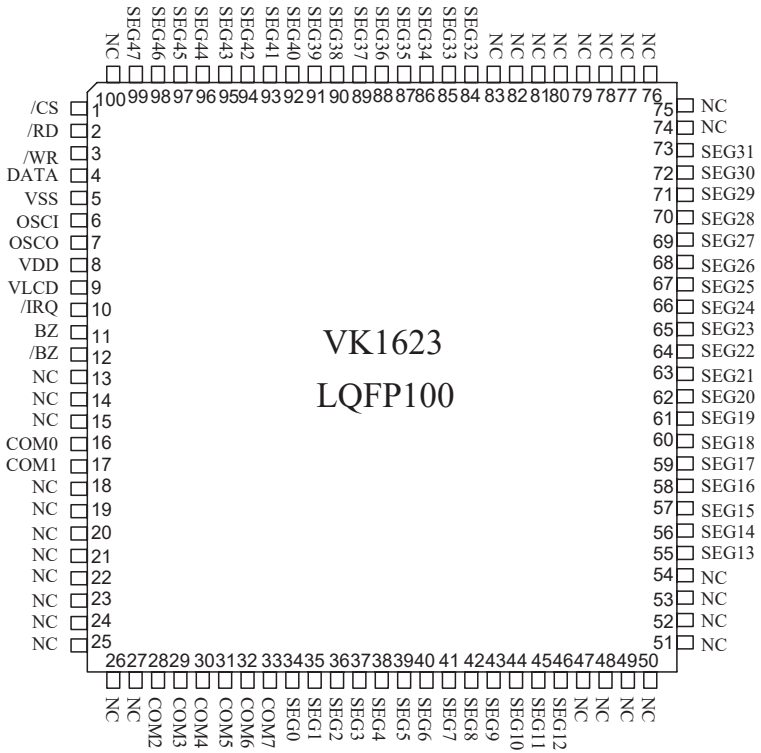
Unit: um

Pad No	Name	X	Y	Pad No	Name	X	Y
1	/CS	-1076	1288	51	NC	—	—
2	/RD	-1270	1212	52	NC	—	—
3	/WR	-1270	1062	53	NC	—	—
4	DATA	-1270	860	54	NC	—	—
5	VSS	-1270	638	55	SEG13	1293	-1008
6	OSCI	-1270	513	56	SEG14	1270	-823
7	OSCO	-1270	388	57	SEG15	1270	-698
8	VDD	-1270	263	58	SEG16	1270	-573
9	VLCD	-1270	138	59	SEG17	1270	-448
10	/IRQ	-1270	13	60	SEG18	1270	-323
11	BZ	-1270	-249	61	SEG19	1270	-198
12	/BZ	-1270	-534	62	SEG20	1270	-73
13	T1	-1270	-738	63	SEG21	1270	51
14	T2	-1270	-863	64	SEG22	1270	176
15	T3	-1270	-988	65	SEG23	1270	301
16	COM0	-1270	-1113	66	SEG24	1270	426
17	COM1	-1270	-1238	67	SEG25	1270	551
18	NC	—	—	68	SEG26	1270	676
19	NC	—	—	69	SEG27	1270	801
20	NC	—	—	70	SEG28	1270	926
21	NC	—	—	71	SEG29	1270	1051
22	NC	—	—	72	SEG30	1270	1176
23	NC	—	—	73	SEG31	1270	1301
24	NC	—	—	74	NC	—	—
25	NC	—	—	75	NC	—	—
26	NC	—	—	76	NC	—	—
27	NC	—	—	77	NC	—	—

Unit: um

Pad No	Name	X	Y	Pad No	Name	X	Y
28	COM2	-1035	-1288	78	NC	—	—
29	COM3	-910	-1288	79	NC	—	—
30	COM4	-785	-1288	80	NC	—	—
31	COM5	-660	-1288	81	NC	—	—
32	COM6	-535	-1288	82	NC	—	—
33	COM7	-410	-1288	83	NC	—	—
34	SEG0	-285	-1288	84	SEG32	923	1289
35	SEG1	-160	-1288	85	SEG33	798	1289
36	SEG2	-35	-1288	86	SEG34	673	1289
37	SEG3	90	-1288	87	SEG35	548	1289
38	SEG4	215	-1288	88	SEG36	423	1289
39	SEG5	340	-1288	89	SEG37	298	1289
40	SEG6	465	-1288	90	SEG38	173	1289
41	SEG7	590	-1288	91	SEG39	48	1289
42	SEG8	715	-1288	92	SEG40	-76	1289
43	SEG9	840	-1288	93	SEG41	-201	1289
44	SEG10	965	-1288	94	SEG42	-326	1289
45	SEG11	1090	-1288	95	SEG43	-451	1289
46	SEG12	1215	-1288	96	SEG44	-576	1289
47	NC	—	—	97	SEG45	-701	1289
48	NC	—	—	93	SEG46	-826	1289
49	NC	—	—	99	SEG47	-951	1289
50	NC	—	—	100	NC	—	—

6 Package Pinout Information (LQFP100)

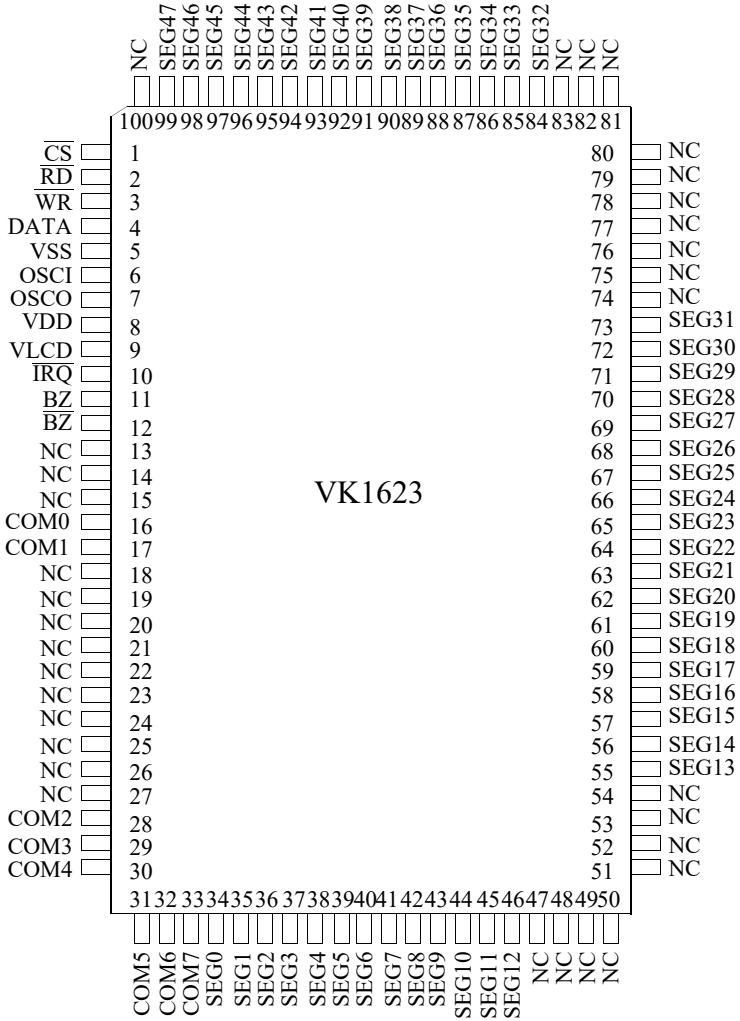


For more information: Page 24

6.1 VK1623/LQFP100 Pin Description

No.	Name	I/O	Function
1	/CS	I	Chip select signal with pull-up resistor ,active low.
2	/RD	I	Serial read signal with pull-up resistor, data out on the falling edge of the /RD signal.
3	/WR	I	Serial write signal with pull-up resistor, data latched on the rising edge of the /WR signal.
4	DATA	I/O	Serial data signal with pull-up resistor, input/output depending on access mode.
5	VSS	VSS	Negative power supply
6	OSCI	I	Crystal oscillator: OSCI and OSCO pins are connected to a 32.768kHz crystal External clock source: OSCI pin is connected to a, external clock source On-chip RC oscillator: the OSCI and OSCO pins can be left open.
7	OSCO	I	
8	VDD	VDD	Positive power supply
9	VLCD	I	LCD driving voltage input,must be ≤VDD
10	/IRQ	O	Time base or WDT overflow flag, NMOS open drain output.
11	BZ	O	2kHz or 4kHz tone frequency output， when TONE OFF the /BZ pin output low level.
12	/BZ	O	
13-15	NC	—	——
16,17 28-33	COM0-COM7	O	LCD COM drive outputs
34-46 55-73 84-99	SEG0-SEG47	O	LCD SEG drive outputs

7 Package Pinout Information (QFP100)



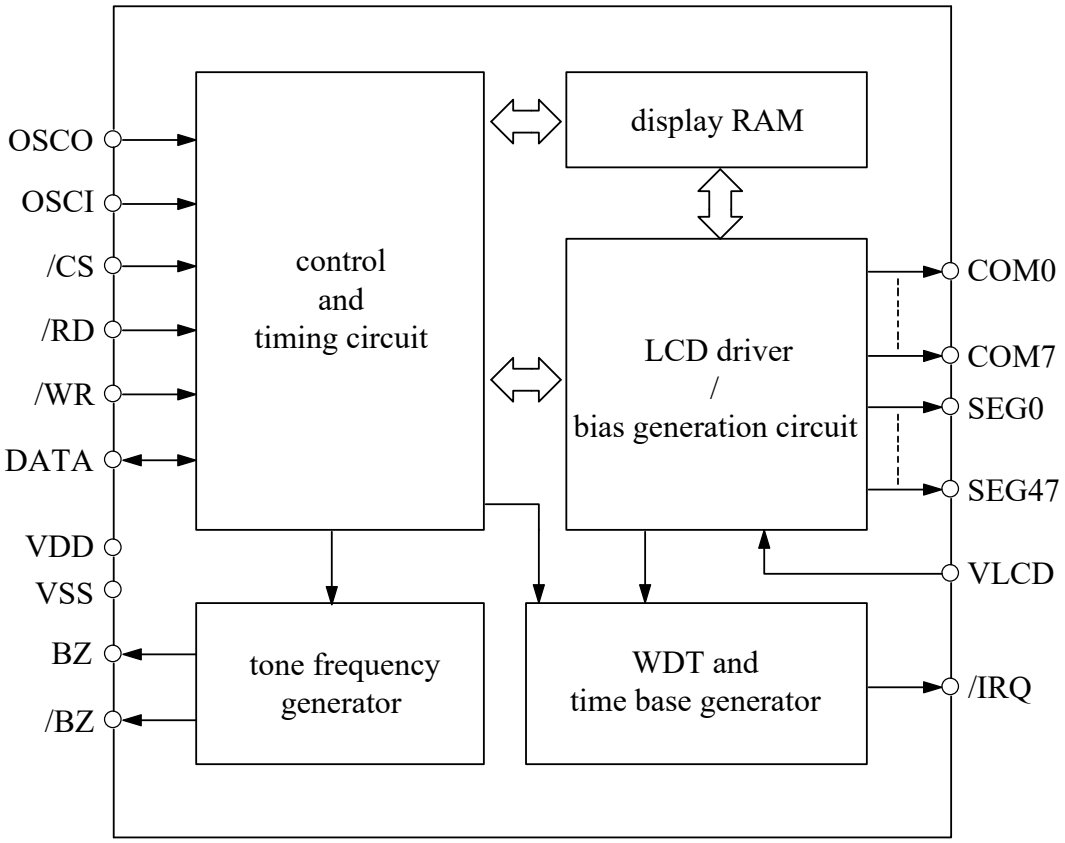
For more information: Page 25

7.1 VK1623/QFP100 Pin Description

No.	Name	I/O	Function
1	/CS	I	Chip select signal with pull-up resistor ,active low.
2	/RD	I	Serial read signal with pull-up resistor, data out on the falling edge of the /RD signal.
3	/WR	I	Serial write signal with pull-up resistor, data latched on the rising edge of the /WR signal.
4	DATA	I/O	Serial data signal with pull-up resistor, input/output depending on access mode.
5	VSS	VSS	Negative power supply
6	OSCI	I	Crystal oscillator: OSCI and OSCO pins are connected to a 32.768kHz crystal External clock source: OSCI pin is connected to a, external clock source On-chip RC oscillator: the OSCI and OSCO pins can be left open.
7	OSCO	I	
8	VDD	VDD	Positive power supply
9	VLCD	I	LCD driving voltage input,must be ≤VDD
10	/IRQ	O	Time base or WDT overflow flag, NMOS open drain output.
11	BZ	O	2kHz or 4kHz tone frequency output， when TONE OFF the /BZ pin output low level.
12	/BZ	O	
13-15	NC	—	——
16,17 28-33	COM0-COM7	O	LCD COM drive outputs
34-46 55-73 84-99	SEG0-SEG47	O	LCD SEG drive outputs

8 Functional Description

8.1 Block Diagram



8.2 Display RAM

The VK1623S integrates 48 × 8-bit RAM for LCD display. directly mapped to SEGx/COMx segments. Data is latched and updated on the LCD according to scan timing set by the system configuration. The display RAM can be accessed using three commands: READ, WRITE, and READ-MODIFY-WRITE. Each RAM address corresponds to a specific combination of SEG and COM lines.

The following is a mapping from the RAM to the LCD pattern:

	COM7	COM6	COM5	COM4		COM3	COM2	COM1	COM0		
SEG0					1					0	address 7 bit （A6----A0）
SEG1					3					2	
SEG2					5					4	
SEG3					7					6	
⋮					⋮					⋮	
SEG47					95					94	
	D3	D2	D1	D0	Data\Addr	D3	D2	D1	D0	Data\Addr	

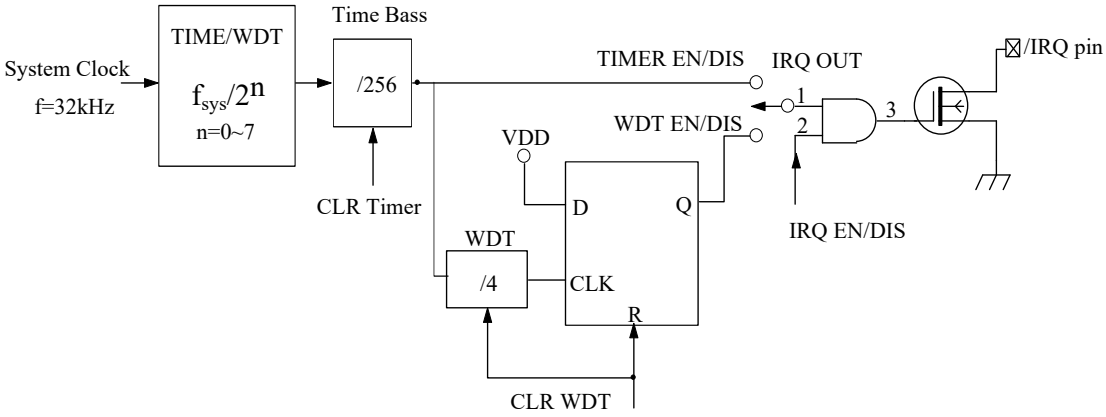
8.3 Time Base and WDT

The time base generator consists of an 8-stage ripple counter and provides accurate timing functionality. The Watchdog Timer (WDT) comprises the 8-stage time base plus an additional 2-stage counter. It helps reset or interrupt the host system in case of abnormal operation, such as unexpected jumps or execution errors. A WDT timeout sets an internal status flag. Both the time base overflow and WDT timeout flags can be routed to the /IRQ pin through software configuration. Eight frequency division options are available for the time base and WDT clock, derived using the formula:

$$f_{WDT}=fsys/2^{n} \quad (n=0\sim7) \quad fsys=32kHz$$

The time base generator and the Watchdog Timer (WDT) share the same 8-stage counter. The WDT is cleared by executing the CLR WDT command, while the time base generator can be cleared using either the CLR WDT or the CLR TIMER command. Executing the WDT EN command enables both the time base generator and the WDT timeout flag output, which can be routed to the /IRQ pin. Conversely, executing the WDT DIS command disables the time base generator. After the TIMER EN command is issued, the WDT is disconnected from the /IRQ pin, and the time base overflow signal is instead connected to it. The /IRQ output can be globally enabled or disabled using the IRQ EN and IRQ DIS commands, respectively.By default, the /IRQ output is disabled upon system power-up

Timer and WDT Configurations：



8.4 Tone Output

The VK1623S integrates a basic tone generator capable of producing 2 kHz or 4 kHz output signals. The output consists of a differential pair: BZ and /BZ, designed to drive a passive piezoelectric buzzer. Use the TONE 2K or TONE 4K commands to select the desired tone frequency. Tone output can be enabled or disabled via the TONE ON or TONE OFF commands. When the tone function is disabled or the system is powered down, both BZ and /BZ will remain at low level.

8.5 LCD Driver

The VK1622S is a 384-segment LCD driver (48 SEG × 8 COM). It supports software configurable bias settings of 1/4, and COM configurations of 8.

8.6 Communication Interfacing

The VK1623S communicates with the host via a 3-wire or 4-wire serial interface.

When used solely for display output, only 3 lines are required (/CS, /WR, and DATA); /RD is optional for reading.

- /CS: Chip select input. It enables the serial interface when low and terminates communication when high.
- /RD: Read clock input. On the falling edge, data is output from the device onto the DATA line.
- /WR: Write clock input. On the rising edge, data and commands from DATA are latched into the device.
- DATA: Bidirectional serial data line used to transfer both command and display data.
- /IRQ: Open-drain output pin for either WDT timeout or time base overflow flag, selectable via software.

8.7 Command Format

The VK1623S is configured via software commands that support two primary modes: command mode and data mode.

- Command mode is used to configure system-level parameters. It is identified by a command mode ID of 100.
- Data mode supports three types of memory operations: READ, WRITE, and READ-MODIFY-WRITE.

These commands allow the host controller to configure LCD behavior and access display RAM contents.

The following are the data mode IDs and the command mode ID:

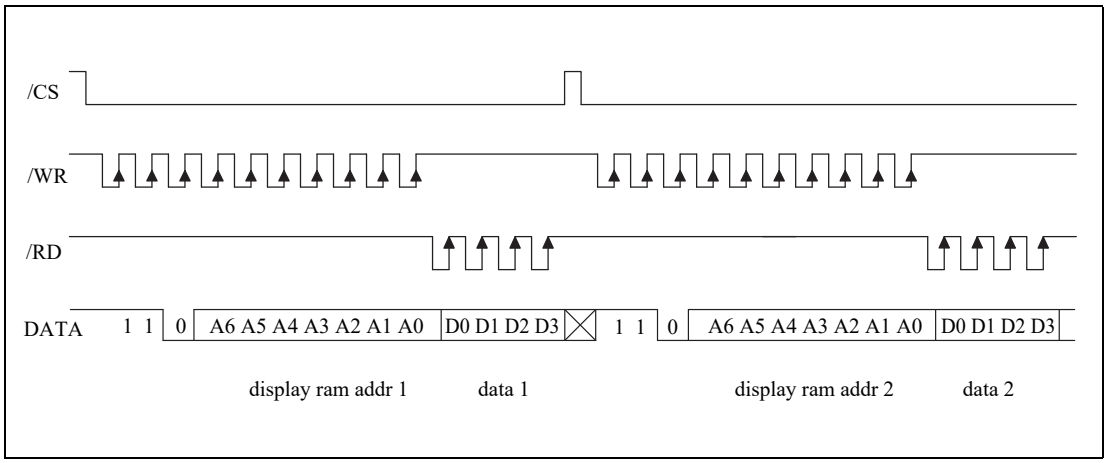
Command	MODE	ID
READ	DATA	110
WRITE	DATA	101
Read-Modify-Write	DATA	101
COMMAND	COMMAND	100

9 Cmd/Data Timing Diagram

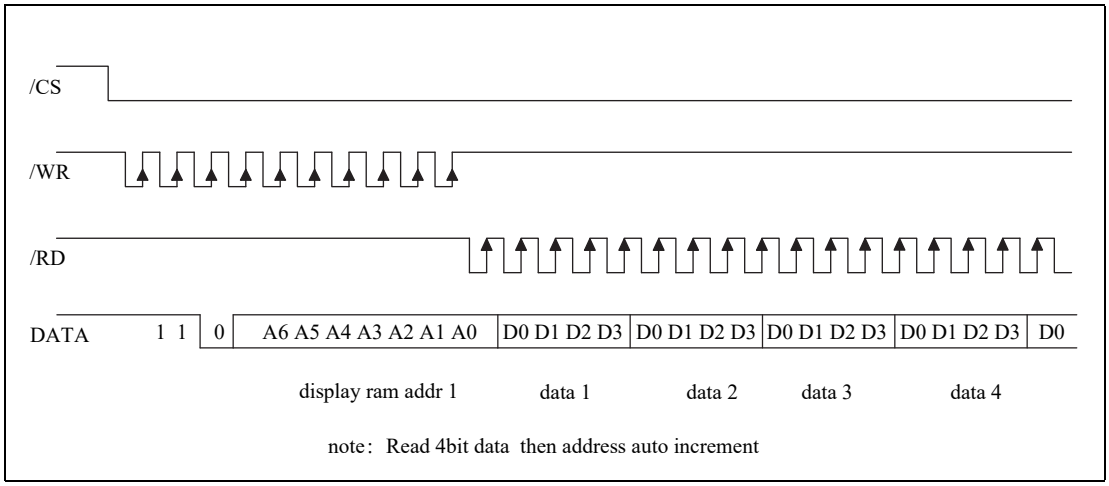
The following are the data mode IDs and the command mode ID Timing Diagrams.

9.1 READ Mode

Command Code : 110

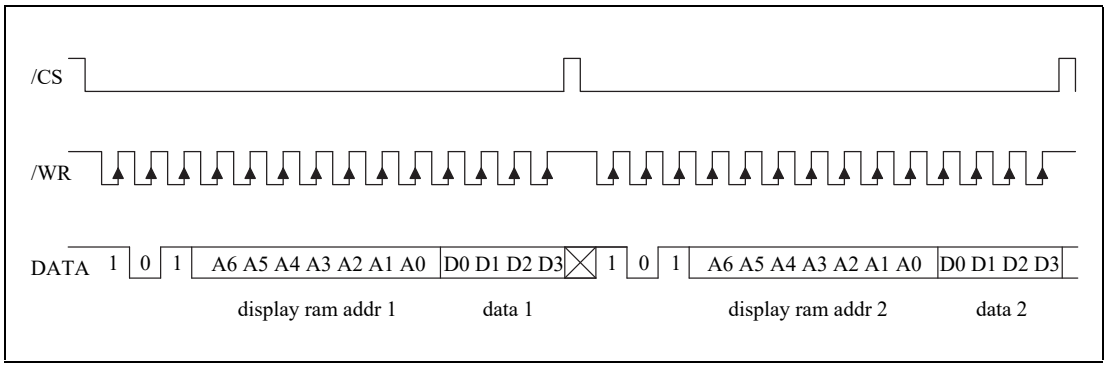


Successive Address Reading

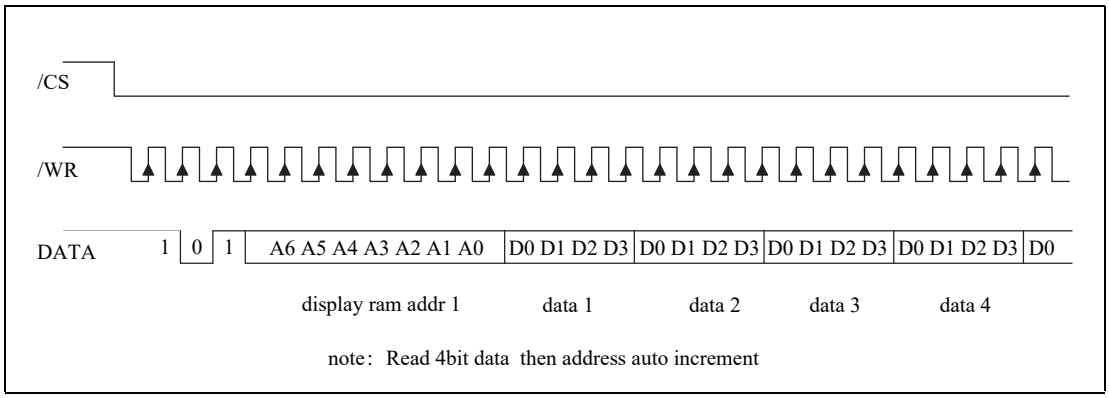


9.2 WRITE Mode

Command Code : 101

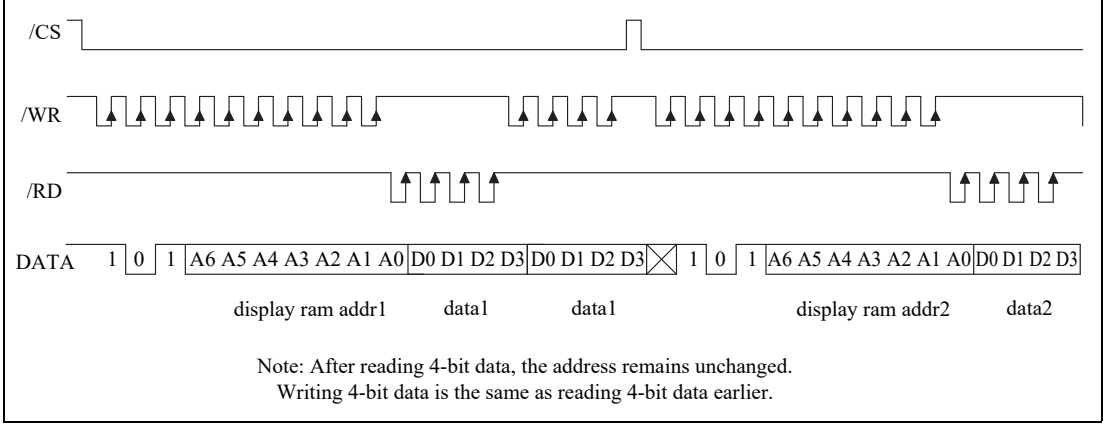


Successive Address Writing



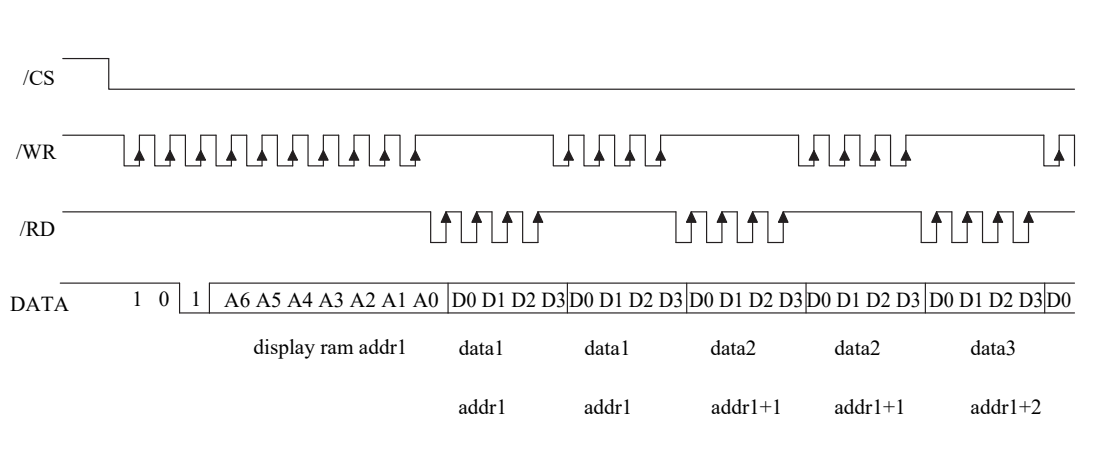
9.3 Read-Modify-Write Mode

Command Code : 101



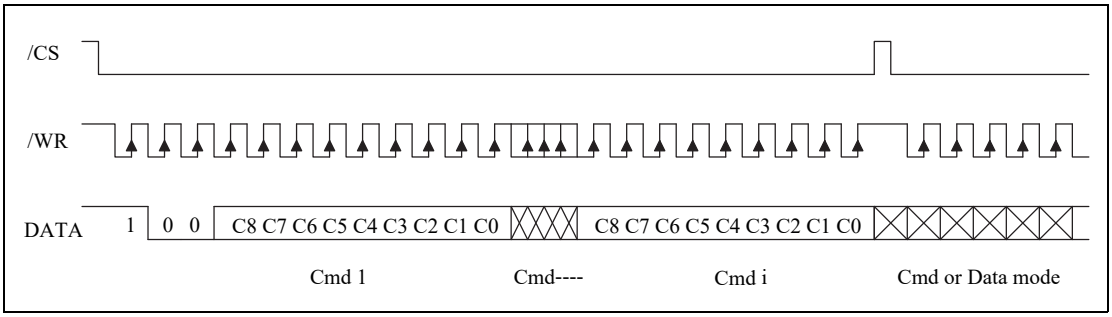
Note: After reading 4-bit data, the address remains unchanged.
Writing 4-bit data is the same as reading 4-bit data earlier.

Successive Address Accessing



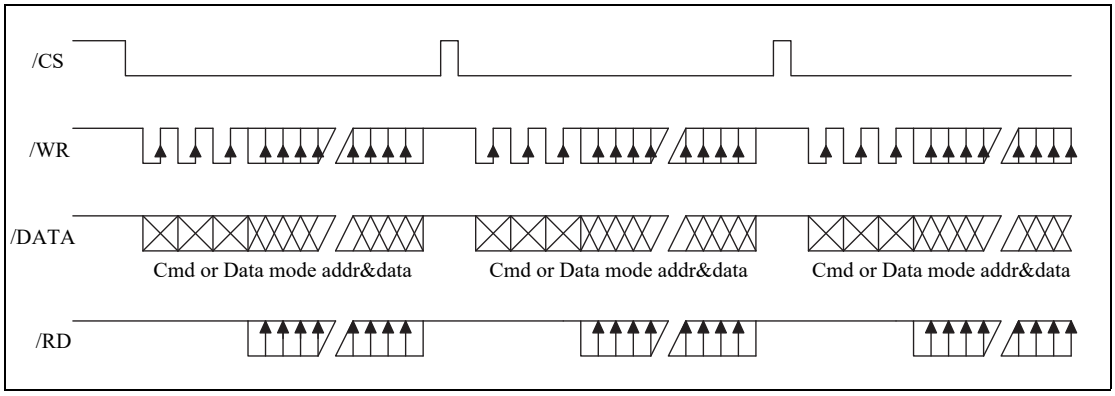
9.4 Command Mode

Command Code : 100



9.5 Data and Command Mode

Data and Command Mode



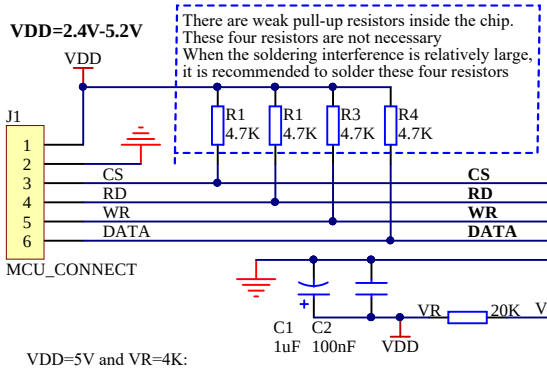
10 Command Summary

Name	ID	Command Code	D/C	Function	Def.
READ	110	A6A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	101	A6A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	101	A6A5A4A3A2A1A0D0D1D2D3	D	READ and WRITE to the RAM	
SYS DIS	100	0000-0000-X	C	Turn off both system oscillator	YES
SYS EN	100	0000-0001-X	C	Turn on system oscillator	
LCD OFF	100	0000-0010-X	C	Turn off LCD bias generator	YES
LCD ON	100	0000-0011-X	C	Turn on LCD bias generator	
TIMERS DIS	100	0000-0100-X	C	Disable time base output	
WDT DIS	100	0000-0101-X	C	Disable WDT time-out flag output	
TIMER EN	100	0000-0110-X	C	Enable time base output	
WDT EN	100	0000-0111-X	C	Enable WDT time-out flag output	
TONE OFF	100	0000-1000-X	C	Turn off tone outputs	YES
CLR TIMER	100	0000-11XX-X	C	Clear the contents of time base generator	
CLR WDT	100	0000-111X-X	C	Clear the contents of WDT stage	
RC32K	100	0001-10XX-X	C	on-chip RC oscillator	YES
EXT_XTAL 32k	100	0001-11XX-X	C	external clock source	
TONE 4k	100	010X-XXXX-X	C	Tone frequency, 4kHz	
TONE 2k	100	011X-XXXX-X	C	Tone frequency, 2kHz	
IRQ DIS	100	100X-0XXX-X	C	Disable IRQ output	YES
IRQ EN	100	100X-1XXX-X	C	Enable IRQ output	
F1	100	101X-X000-X	C	Time base/WDT clock output:1Hz The WDT time-out flag after: 4s	
F2	100	101X-X001-X	C	Time base/WDT clock output:2Hz The WDT time-out flag after: 2s	
F4	100	101X-X010-X	C	Time base/WDT clock output:4Hz The WDT time-out flag after: 1s	
F8	100	101X-X011-X	C	Time base/WDT clock output:8Hz The WDT time-out flag after: 1/2s	
F16	100	101X-X100-X	C	Time base/WDT clock output:16Hz The WDT time-out flag after: 1/4s	
F32	100	101X-X101-X	C	Time base/WDT clock output:32Hz The WDT time-out flag after: 1/8s	
F64	100	101X-X110-X	C	Time base/WDT clock output:64Hz The WDT time-out flag after: 1/16s	
F128	100	101X-X111-X	C	Time base/WDT clock output:128Hz The WDT time-out flag after: 1/32s	YES
TEST	100	1110-0000- X	C	Test mode	
NORMAL	100	1110-0011- X	C	Normal mode	YES

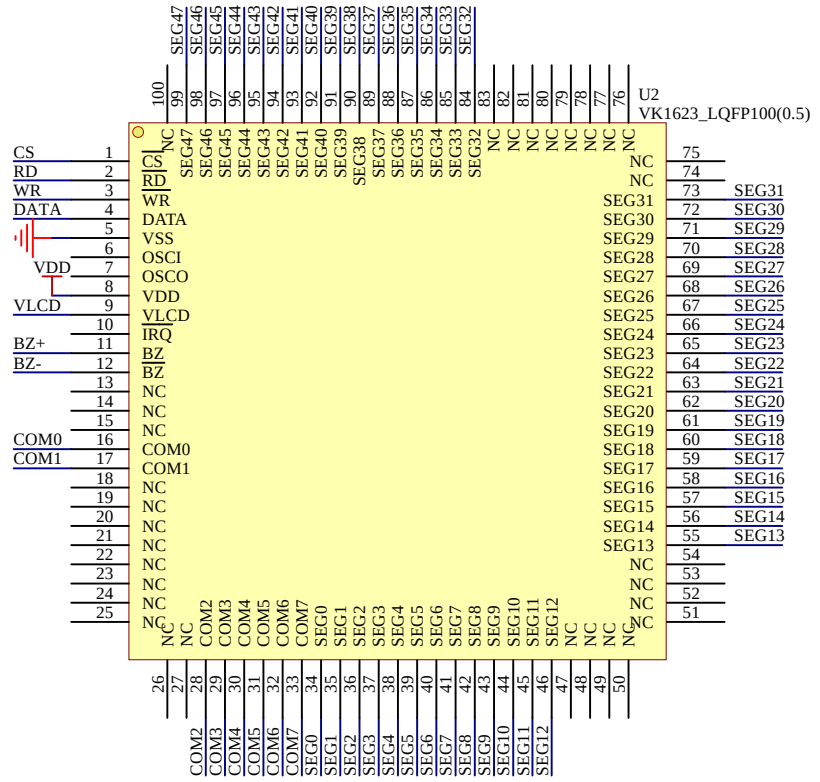
note: X: 0 or 1 D/C:Data/Command mode
A6-A0: Display RAM addresses Def.:Power on reset default
D3-D0:4bit Display RAM data 110,101and 100 is Command ID

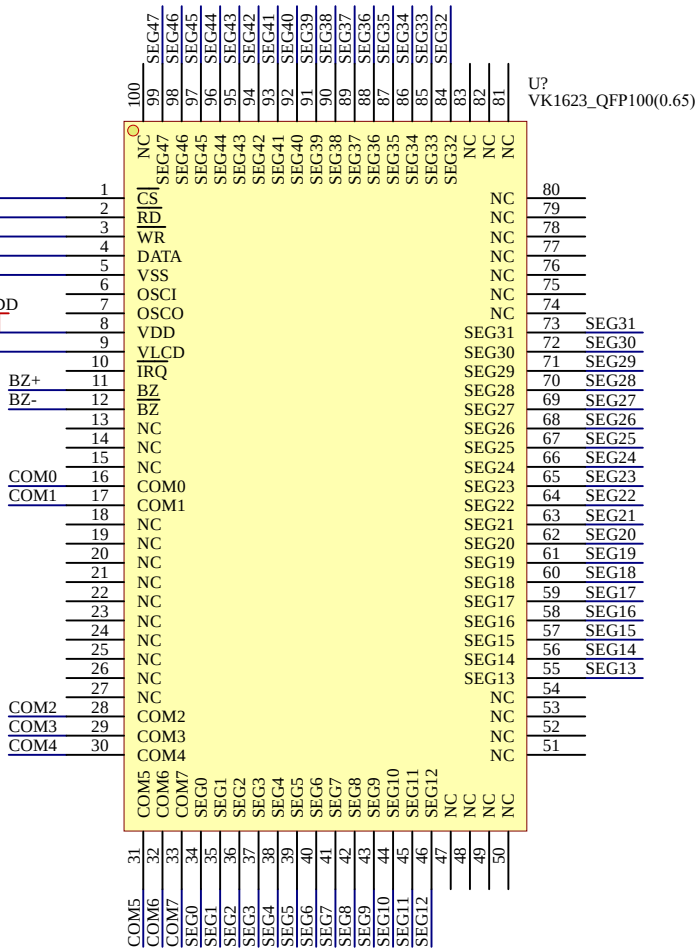
11 Application Circuits

When the LCD only displays, the RD pin can be left floating and not connected
When the surrounding interference is relatively large, a 10R to 1k resistor and a small PF-level capacitor to ground can be connected in series on the communication pin
When the power supply of the chip machine (3.3V) and the driver chip (5V) is inconsistent, it is recommended to add a level conversion circuit to the communication pin

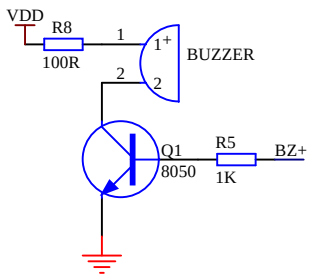


VDD=5V and VR=4K:
The VLCD is approximately 4.2V
It is recommended to use a 20K adjustable resistor for VR to achieve the best display effect and take the resistance value at this time.

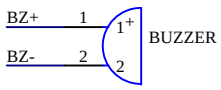




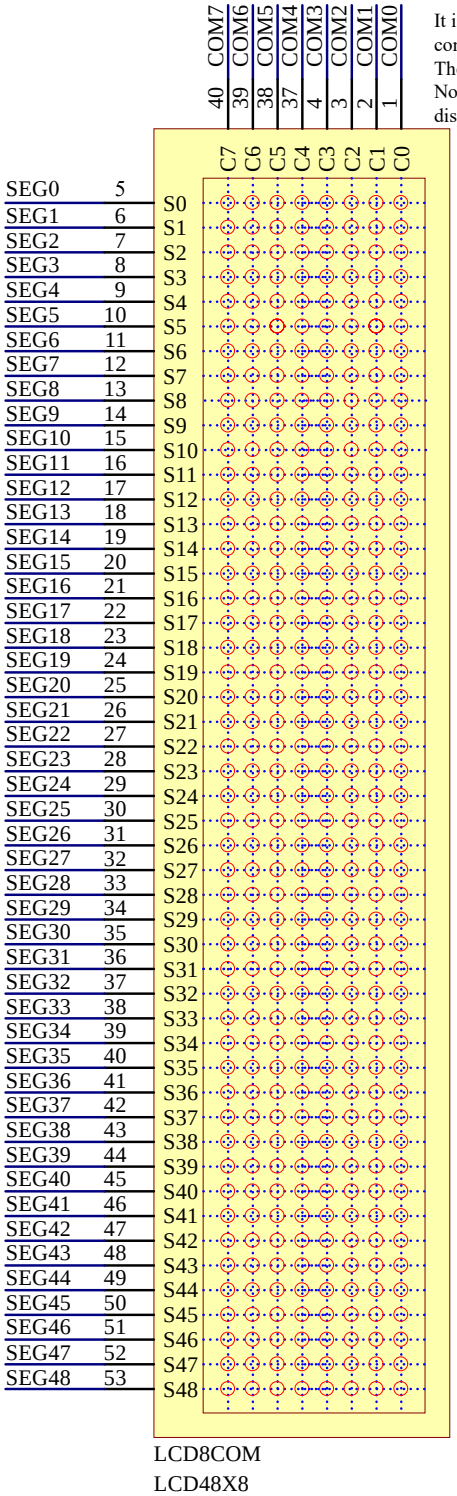
Passive buzzer driving current >1mA circuit



Passive buzzer driving current <1mA circuit



The buzzer frequency is 2kHz or 4kHz, and the buzzer voltage is no more than 5V



It is recommended that the COM pins of the chip and the LCD be connected in a one-to-one sequence
The SEG pins can be shuffled for the convenience of PCB routing
Note that when writing software, the sequence corresponding to the displayed RAM should also be changed

RAM1-BIT3 BIT2 BIT1 BIT0 RAM0- BIT3 BIT2 BIT1
RAM3-BIT3 BIT2 BIT1 BIT0 RAM2- BIT3 BIT2 BIT1
RAM5-BIT3 BIT2 BIT1 BIT0 RAM4- BIT3 BIT2 BIT1

RAM95-BIT3 BIT2 BIT1 BIT0 RAM94- BIT3 BIT2 BIT1 BIT0
RAM97-BIT3 BIT2 BIT1 BIT0 RAM96- BIT3 BIT2 BIT1 BIT0

12 Electrical Characteristics

12.1 Absolute Maximum Ratings

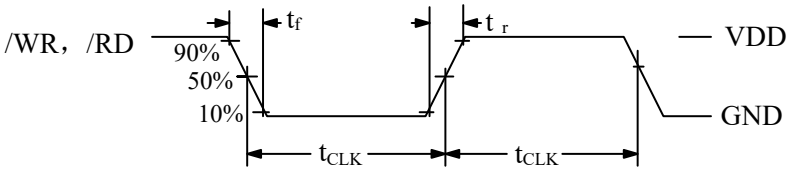
Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3～5.5	V
Input Voltage	VIN	V_{SS}-0.3～V_{DD}+0.3	V
Storage Temperature	T_{STG}	-50～+125	℃
Operating Temperature	T_{OTG}	-40～+85	℃

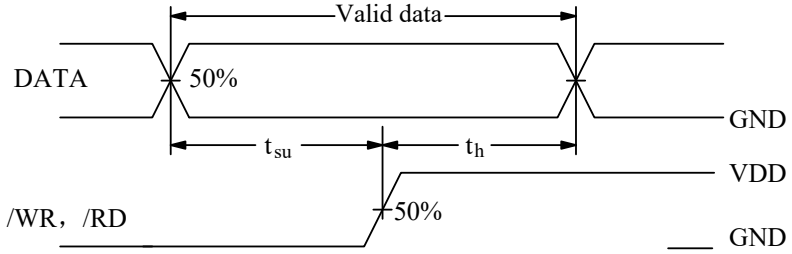
12.2 DC Electrical Characteristics

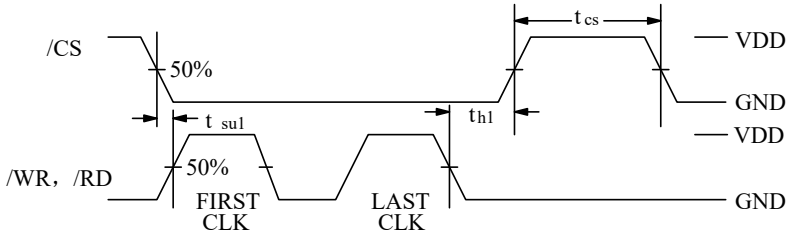
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	2.4	—	5.2	V	—	—
Operating current	I_{DD1}	—	155	310	μA	3V	No load/LCD ON On-chip RC oscillator
		—	260	420		5V	
Operating current	I_{DD2}	—	150	310	μA	3V	No load/LCD ON External crystal
		—	250	420		5V	
Operating current	I_{DD11}	—	8	30	μA	3V	No load/LCD OFF On-chip RC oscillator
		—	20	60		5V	
Operating current	I_{DD22}	—	—	20	μA	3V	No load/LCD OFF External crystal
		—	—	35		5V	
Standby Current	I_{STB}	—	1	10	μA	3V	No load, Power down mode
		—	2	20		5V	
Low-level Input	V_{IL}	0	—	0.6	V	3V	DATA, /WR, /CS,/RD
		0	—	1.0		5V	
High-level Input	V_{IH}	2.4	—	3.0	V	3V	DATA, /WR, /CS,/RD
		4.0	—	5.0		5V	
BZ, /BZ, /IRQ	I_{OL1}	0.9	1.8	—	mA	3V	V_{OL}=0.3V
		1.7	3.0	—		5V	V_{OL}=0.5V
BZ, /BZ	I_{OH1}	-0.9	-1.8	—	mA	3V	V_{OH}=2.7V
		-1.7	-3.0	—		5V	V_{OH}=4.5V
DATA	I_{OH1}	0.9	1.8	—	mA	3V	V_{OL}=0.3V
		1.7	3.0	—		5V	V_{OL}=0.5V
DATA	I_{OH1}	-0.9	-1.8	—	mA	3V	V_{OH}=2.7V
		-1.7	-3.0	—		5V	V_{OH}=4.5V
LCD COM Sink Current	I_{OL2}	80	160	—	μA	3V	V_{OL}=0.3V
		180	360	—		5V	V_{OL}=0.5V
LCD COM Source Current	I_{OH2}	-40	-80	—	μA	3V	V_{OH}=2.7V
		-90	-180	—		5V	V_{OH}=4.5V
LCD SEG Sink Current	I_{OL3}	50	100	—	μA	3V	V_{OL}=0.3V
		120	240	—		5V	V_{OL}=0.5V
LCD SEG Source Current	I_{OH3}	-30	-60	—	μA	3V	V_{OH}=2.7V
		-70	-140	—		5V	V_{OH}=4.5V
Pull-UP Resistor	R_{UP}	100	200	300	kΩ	3V	DATA, /WR, /CS,/RD
		50	100	150		5V	

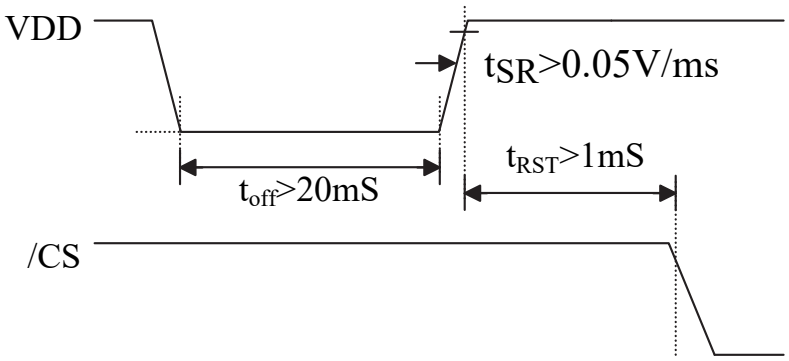
12.3 AC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
System Clock	f_{SYS1}	22	32	40	kHz	3V	On-chip RC oscillator
		24	32	40		5V	
System Clock	f_{SYS2}	—	32	—	kHz	3V	External clock source
		—	32	—		5V	
LCD Clock	f_{LCD1}	44	64	80	Hz	3V	On-chip RC oscillator
		48	64	80	Hz	5V	
	f_{LCD2}	—	64	—	Hz	3V	External clock (32kHz)
		—	64	—	Hz	5V	
LCD Common Period	t_{COM}	—	n/ f_{LCD}	—	sec	—	N：Number of COM
Serial Data Clock(/WR)	F_{CLK1}	—	—	150	kHz	3V	Duty cycle 50%
		—	—	300		5V	
Serial Data Clock(/RD)	F_{CLK2}	—	—	75	kHz	3V	Duty cycle 50%
		—	—	150		5V	
Serial Interface Reset PW	t_{CS}	—	250	—	ns	—	/CS
/WR, /RD Input Pulse Width	t_{CLK}	3.34	—	—	μS	3V	Write mode
		6.67	—	—			Read mode
		1.67	—	—	μS	5V	Write mode
		3.34	—	—			Read mode
Rise/Fall Time Serial Data Clock Width	t_r，t_f	—	120	—	ns	3V	—
						5V	
Setup Time for DATA to /WR, /RD Clock Width	t_{su}	—	120	—	ns	3V	—
						5V	
Hold Time for DATA to /WR, /RD Clock Width	t_h	—	120	—	ns	3V	—
						5V	
Setup Time for /CS to /WR, /RD Clock Width	t_{su1}	—	100	—	ns	3V	—
						5V	
Hold Time for /CS to /WR, /RD Clock Width	t_{h1}	—	100	—	ns	3V	—
						5V	


/WR，/RD
90%
50%
10%
tf
t r
VDD
GND
tCLK
tCLK

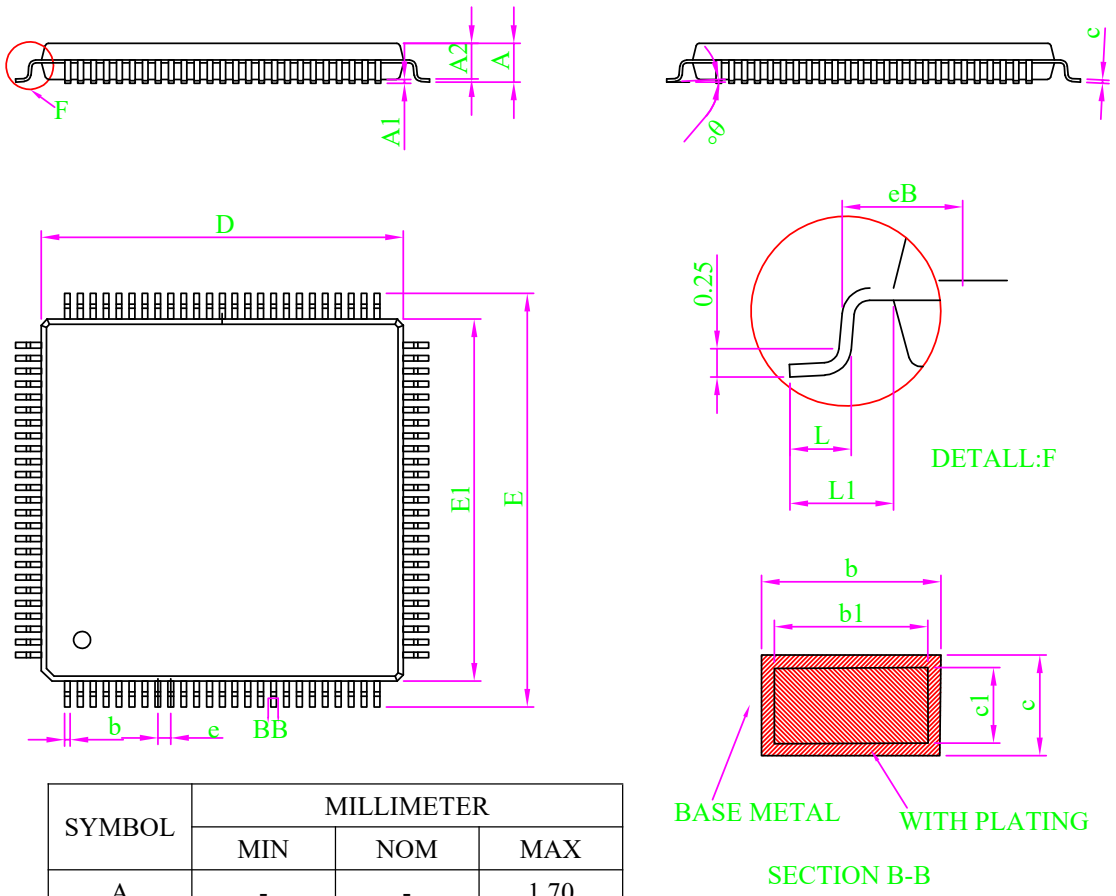

Valid data
DATA
50%
GND
tsu
th
VDD
/WR，/RD
50%
GND


/CS
50%
t cs
VDD
GND
t su1
th1
VDD
/WR，/RD
50%
FIRST CLK
LAST CLK
GND


VDD
tSR>0.05V/ms
tRST>1mS
toff>20mS
/CS

13 Package Information

13.1 LQFP100(14.0mm×14.0mm PP=0.5mm)

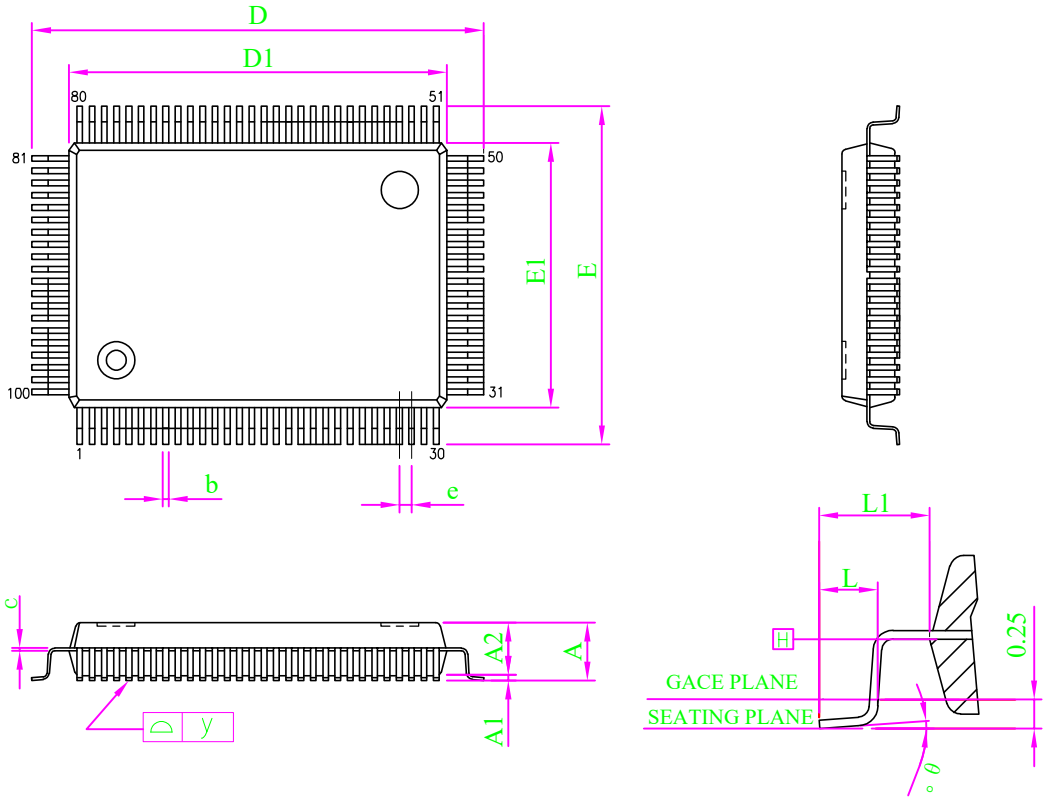


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.70
A1	0.10	0.15	0.20
A2	1.30	1.40	1.50
b	0.17	-	0.27
b1	0.16	0.20	0.24
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
eB	15.05	-	15.40
e	0.50BSC		
L	0.42	0.57	0.72
L1	0.95	1.00	1.15
θ	0	-	10°

Note:

1. All dimension are in mm.
2. Dim D&El does not include plastic flash; Flash: Plastic residual around body edge after de junk/singulation.
3. Dim b does not include dambar protrusion/intrusion.
4. Plating thickness 0.007mm-0.015mm

13.2 QFP100(20.0mm × 14.0mm PP=0.65mm)



SYMBOL	MIN	NOMINAL	MAX
A	—	—	3.40
A1	0.25	—	0.50
A2	2.57	2.72	2.87
b	—	0.30	—
c	0.10	0.15	0.20
D	23.65	23.90	24.15
D1	19.90	20.00	20.10
e	—	0.65	—
E	17.65	17.90	18.15
E1	13.90	14.00	14.10
L	0.65	0.80	0.95
L1	—	1.95	—
y	—	—	0.10
θ°	0	—	7

UNIT:mm

NOTES:

1.JEDEC OUTLINE:MO-112 CC-1

2.DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THW BODY.

3.DIMENSIONS D1 AND E1 D0 NOT INCLUDE MOLD PROTRUSION, ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 D0 NOT INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

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15 Revision History

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	initial release	YES
2	1.1	2018-10-11	Add reference circuit	YES
3	1.2	2019-03-21	Alignment correction	YES
4	1.3	2025-06-11	Change Description	YES

[1] Please refer to the latest version of this document before starting or finalizing any design.

[2] Since the release of this document, the status or availability of this product may have changed. For the most up-to-date information, please visit: https://www.szvinka.com/