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Vinka Microelectronics

VK1621S-1 Datasheet

32×4 LCD DRIVER

Rev.1.3

1 General Description

The VK1621S-1 is a RAM-mapped LCD segment driver capable of supporting up to 128 segments (32 SEG × 4 COM). It supports 2-COM,3-COM and 4-COM display configurations.
The device communication via a 3-wire or 4-wire serial interface, which is used for display parameter configuration, data transmission, and Power-down control.

2 Key Features

- Operating voltage:2.4-5.2V
- Integrated RC oscillator (default)
- External crystal input: 32.768 kHz (OSCO, OSCI)
- External clock source: 256 kHz (OSCI)
- Selectable LCD bias: 1/2 or 1/3
- Selectable LCD duty: 1/2, 1/3, or 1/4
- Built-in 32 × 4 bit display RAM
- Configurable buzzer output: 2 kHz or 4 kHz
- Power-down mode via software command(LCD OFF, SYS DIS)
- Eight selectable clock sources for time base / WDT
- WDT or time base overflow flag output via /IRQ pin
- 3 wire or 4 wire serial communication interface
- Software-configurable of LCD parameters
- Dual command formats for configuration and access
- Auto-increment addressing for sequential read/write
- Three RAM accessing modes
- VLCD adjustable via external pin (≤ VDD)
- Available Packages:
  SSOP48(300mil)(15.9mm × 7.5mm PP=0.635mm)
  LQFP48(7.0mm × 7.0mm PP=0.5mm)
  LQFP44(10.0mm × 10.0mm PP=0.8mm)
  SDIP28(288mil)(35.3mm × 7.3mm PP=2.54mm)
  DICE
  COG

3 Product Selection

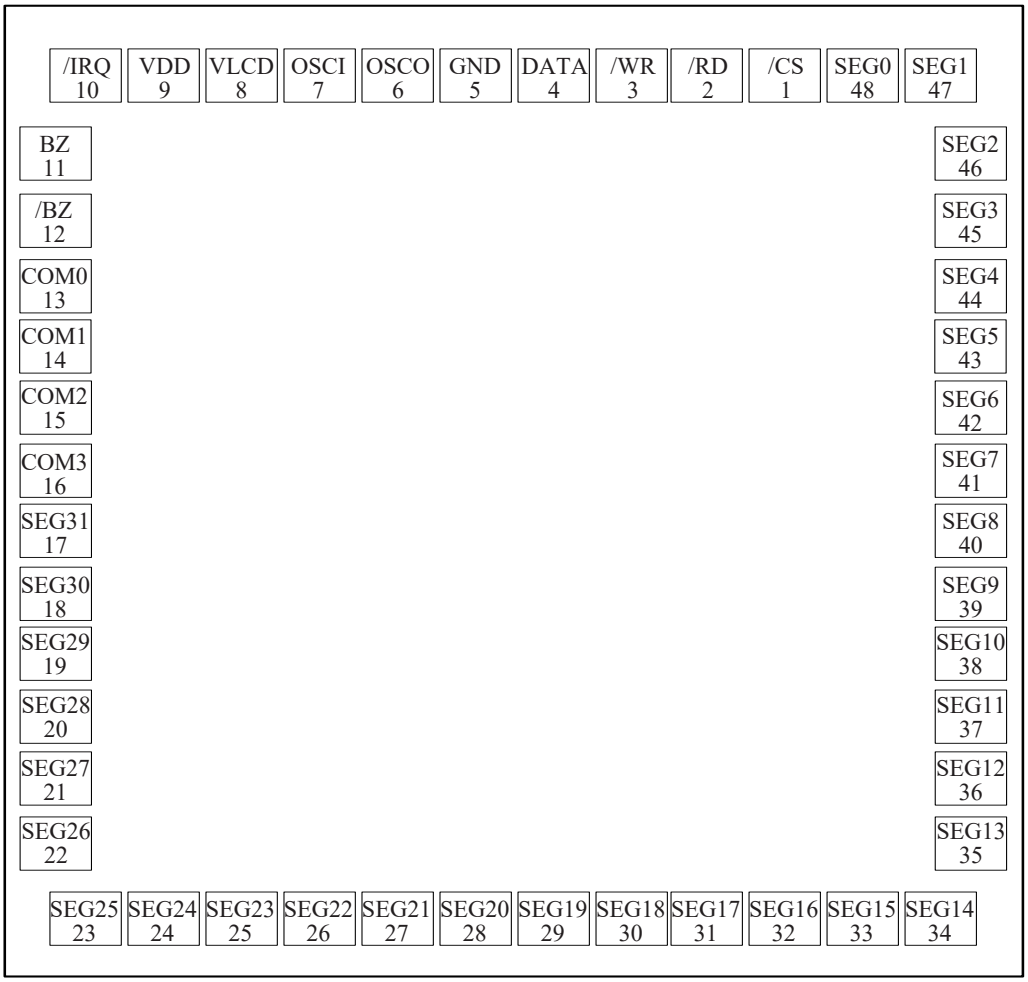
Part No.	VK1620	VK1621S-1	VK1622S-1	VK1623S	VK1625	VK1626
COM	4	4	8	8	8	16
SEG	32	32	32	48	64	48
On-chip Oscillator	-	√	√	√	√	√
Crystal Oscillator	√	√	-	√	√	√
External clock	√	√	√	√	√	√

4 Ordering Information

Part No.	Packaging	Tube Qty	Tray Qty	Box Qty	Total Qty	Notes
VK1620	LQFP64		250/tray	2500/box	15000 PCS	
	DICE		300/tray	1500/box	3000 PCS	DICE
VK1621S-1	LQFP44		160/tray	1600/box	9600 PCS	
	LQFP48		250/tray	2500/box	15000 PCS	
	SSPO48	30/tube		2400/box	24000 PCS	
	DICE		300/tray	1500/box	3000 PCS	DICE
VK1622S-1	LQFP44		160/tray	1600/box	5400 PCS	
	LQFP52		90/tray	900/box	5400 PCS	
	LQFP64		250/tray	2500/box	15000 PCS	
	QFP64		66/tray	660/box	3960 PCS	
	DICE		250/tray	1000/box	2000 PCS	DICE
VK1623S	LQFP100		90/tray	900/box	5400 PCS	
	QFP100		66/tray	660/box	3960 PCS	
	DICE		100/tray	500/box	1000 PCS	DICE
VK1625	LQFP100		90/tray	900/box	5400 PCS	
	QFP100		66/tray	660/box	3960 PCS	
	DICE		100/tray	500/box	1000 PCS	DICE
VK1626	LQFP100		90/tray	900/box	5400 PCS	
	QFP100		66/tray	660/box	3960 PCS	
	DICE		110/tray	550/box	1500 PCS	DICE

5 COB Pad Information

5.1 COB Pad Assignment



Chip Dimensions: 1630×1755 μm², substrate potential: VDD

Pad size: 90×90 μm, Pad spacing: 112 μm,

Al Pad size: 100×100μm, Al pad thickness: 1μm,

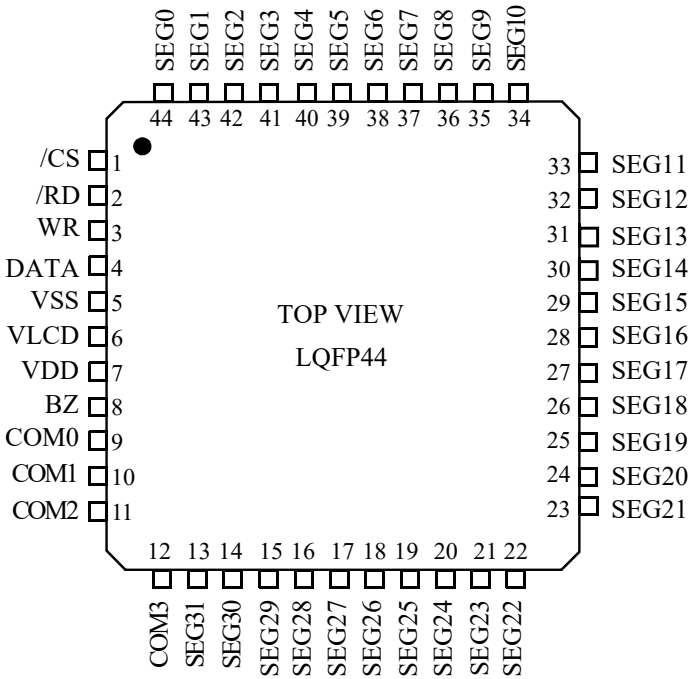
Note: VLCD≤VDD

5.2 COB PAD Coordinates

Unit: um

Pad No	Name	X	Y	Pad No	Name	X	Y
1	/CS	411.5	732.9	25	SEG23	-397.5	-738
2	/RD	298.5	732.9	26	SEG22	-282.5	-738
3	/WR	185.5	732.9	27	SEG21	-167.5	-738
4	DATA	63	732.9	28	SEG20	-52.5	-738
5	GND	-52	732.9	29	SEG19	62.5	-738
6	OSCO	-167	732.9	30	SEG18	177.5	-738
7	OSCI	-282	732.9	31	SEG17	292.5	-738
8	VLCD	-397	732.9	32	SEG16	407.5	-738
9	VDD	-512	732.9	33	SEG15	522.5	-738
10	/IRQ	-627.	732.9	34	SEG14	637.5	-738
11	BZ	-664.5	619.8	35	SEG13	675.5	-626
12	/BZ	-664.5	494	36	SEG12	675.5	-513
13	COM0	-664.5	382	37	SEG11	675.5	-400
14	COM1	-664.5	270	38	SEG10	675.5	-287
15	COM2	-664.5	158	39	SEG9	675.5	-174
16	COM3	-664.5	46	40	SEG8	675.5	-61
17	SEG31	-664.5	-66	41	SEG7	675.5	52
18	SEG30	-664.5	-178	42	SEG6	675.5	165
19	SEG29	-664.5	-290	43	SEG5	675.5	278
20	SEG28	-664.5	-402	44	SEG4	675.5	391
21	SEG27	-664.5	-514	45	SEG3	675.5	504
22	SEG26	-664.5	-626	46	SEG2	675.5	617
23	SEG25	-627	-738	47	SEG1	637.5	732.9
24	SEG24	-512.5	-738	48	SEG0	524.5	732.9

6 Package Pinout Information(LQFP44)

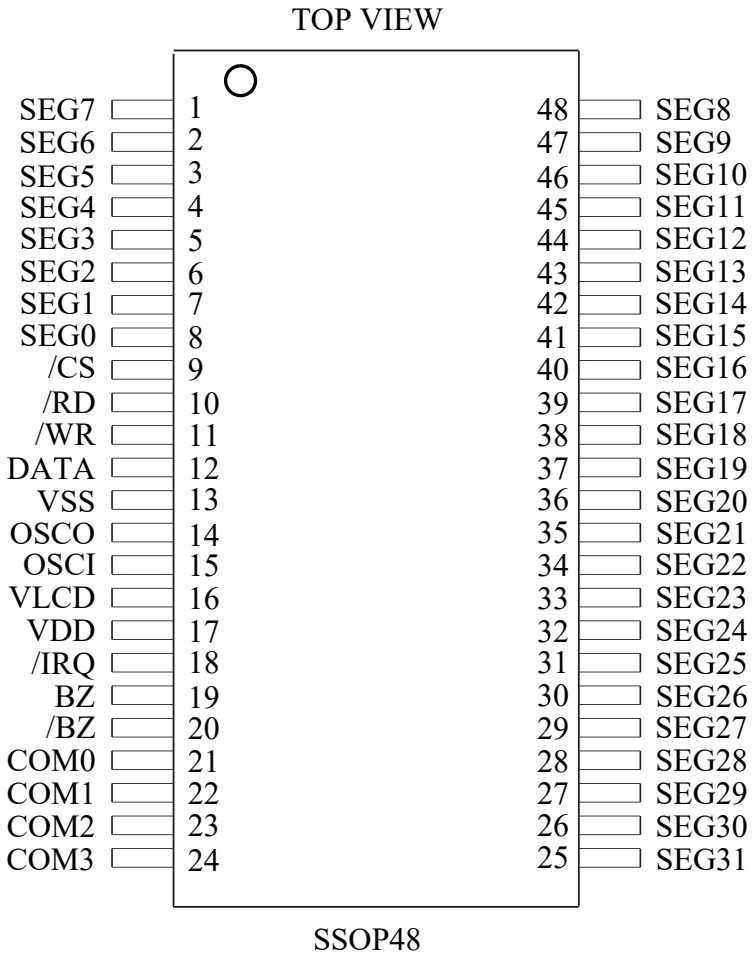


For more information: Page 28

6.1 VK1621A/LQFP44 Pin Description

No.	Name	I/O	Function
1	/CS	I	Chip select signal with pull-up resistor ,active low.
2	/RD	I	Serial read signal with pull-up resistor, data out on the falling edge of the /RD signal.
3	/WR	I	Serial write signal with pull-up resistor, data latched on the rising edge of the /WR signal.
4	DATA	I/O	Serial data signal with pull-up resistor, input/output depending on access mode.
5	VSS	VSS	Negative power supply
6	VLCD	I	LCD driving voltage input,must be ≤VDD
7	VDD	VDD	Positive power supply
8	BZ	O	2kHz or 4kHz tone frequency output, when TONE OFF the /BZ pin output low level.
9-12	COM0-COM3	O	LCD COM drive outputs
13-44	SEG31-SEG0	O	LCD SEG drive outputs

7 Package Pinout Information(SSOP48)



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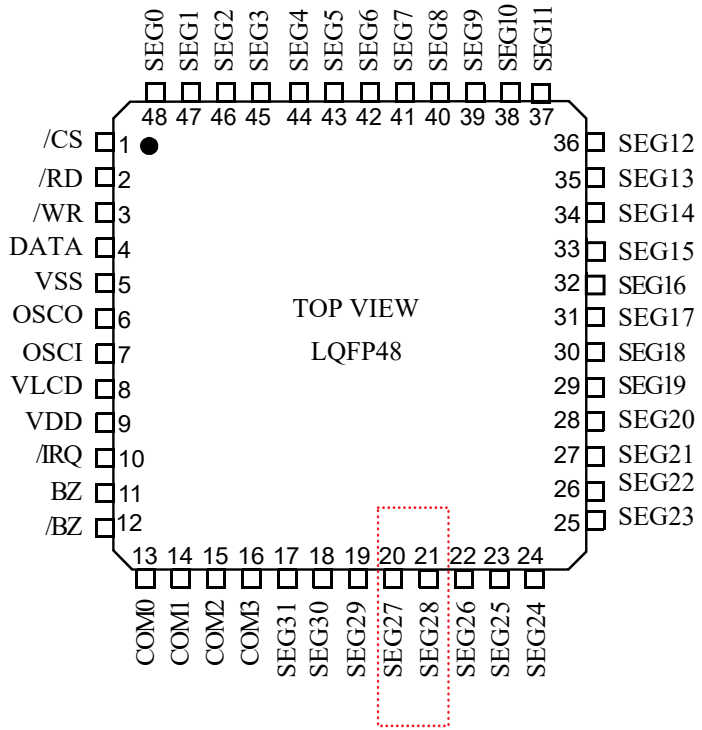
7.1 VK1621B/SSOP48 Pin Description

No.	Name	I/O	Function
1-8	SEG7-SEG0	O	LCD SEG drive outputs
9	/CS	I	Chip select signal with pull-up resistor ,active low.
10	/RD	I	Serial read signal with pull-up resistor, data out on the falling edge of the /RD signal.
11	/WR	I	Serial write signal with pull-up resistor, data latched on the rising edge of the /WR signal.
12	DATA	I/O	Serial data signal with pull-up resistor, input/output depending on access mode.
13	VSS	VSS	Negative power supply
14	OSCO	O	Crystal oscillator: OSCI and OSCO pins are connected to a 32.768kHz crystal External clock source: OSCI pin is connected to a, external clock source On-chip RC oscillator: the OSCI and OSCO pins can be left open.
15	OSCI	I	
16	VLCD	I	LCD driving voltage input,must be ≤VDD
17	VDD	VDD	Positive power supply
18	/IRQ	O	Time base or WDT overflow flag, NMOS open drain output.
19	BZ	O	2kHz or 4kHz tone frequency output pair， when TONE OFF the BZ and /BZ pins output low level.
20	/BZ	O	
21-24	COM0-COM3	O	LCD COM drive outputs
25-48	SEG31-SEG8	O	LCD SEG drive outputs

8 Package Pinout Information(LQFP48)

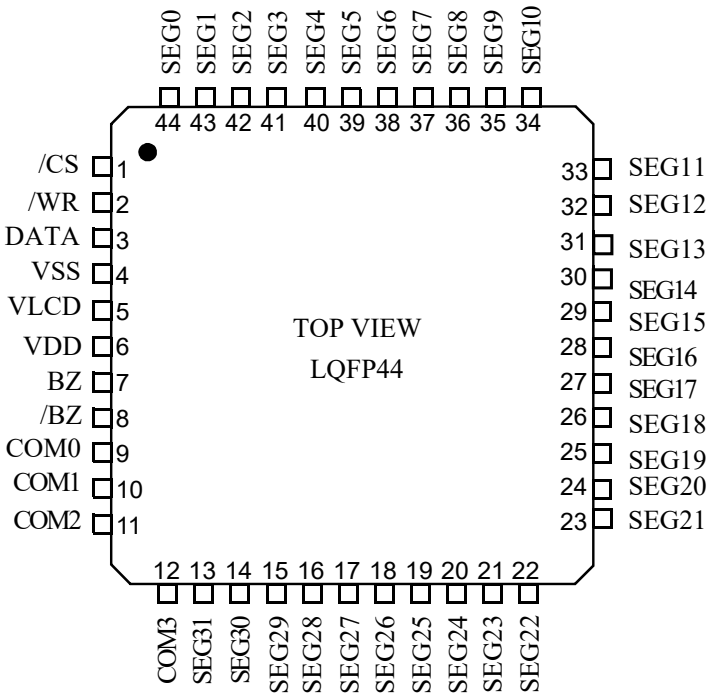


For more information: Page 30

8.1 VK1621B/ LQFP48 Pin Description

No.	Name	I/O	Function
1	/CS	I	Chip select signal with pull-up resistor ,active low.
2	/RD	I	Serial read signal with pull-up resistor, data out on the falling edge of the /RD signal.
3	/WR	I	Serial write signal with pull-up resistor, data latched on the rising edge of the /WR signal.
4	DATA	I/O	Serial data signal with pull-up resistor, input/output depending on access mode.
5	VSS	VSS	Negative power supply
6	OSCO	O	Crystal oscillator: OSCI and OSCO pins are connected to a 32.768kHz crystal External clock source: OSCI pin is connected to a, external clock source On-chip RC oscillator: the OSCI and OSCO pins can be left open.
7	OSCI	I	
8	VLCD	I	LCD driving voltage input,must be ≤VDD
9	VDD	VDD	Positive power supply
10	/IRQ	O	Time base or WDT overflow flag, NMOS open drain output.
11	BZ	O	2kHz or 4kHz tone frequency output pair， when TONE OFF the BZ and /BZ pins output low level.
12	/BZ	O	
13-16	COM0-COM3	O	LCD COM drive outputs
17-19 22-48	SEG31-SEG29 SEG26-SEG0	O	LCD SEG drive outputs
20,21	SEG27,SEG28	O	LCD SEG drive outputs

9 Package Pinout Information(LQFP44)



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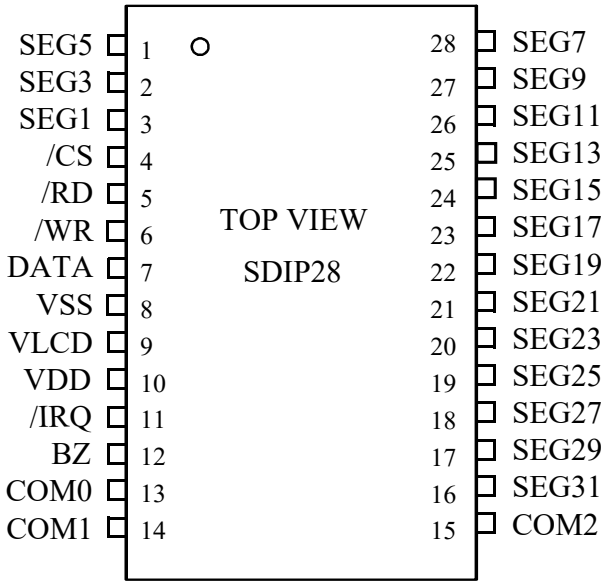
9.1 VK1621B/LQFP44 Pin Description

No.	Name	I/O	Function
1	/CS	I	Chip select signal with pull-up resistor ,active low.
2	/WR	I	Serial write signal with pull-up resistor, data latched on the rising edge of the /WR signal.
3	DATA	I/O	Serial data signal with pull-up resistor, input/output depending on access mode.
4	VSS	VSS	Negative power supply
5	VLCD	I	LCD driving voltage input,must be ≤VDD
6	VDD	VDD	Positive power supply
7	BZ	O	2kHz or 4kHz tone frequency output， when TONE OFF the /BZ pin output low level.
8	/BZ	O	
9-12	COM0-COM3	O	LCD COM drive outputs
13-44	SEG31-SEG0	O	LCD SEG drive outputs

10 Package Pinout Information(SDIP28)



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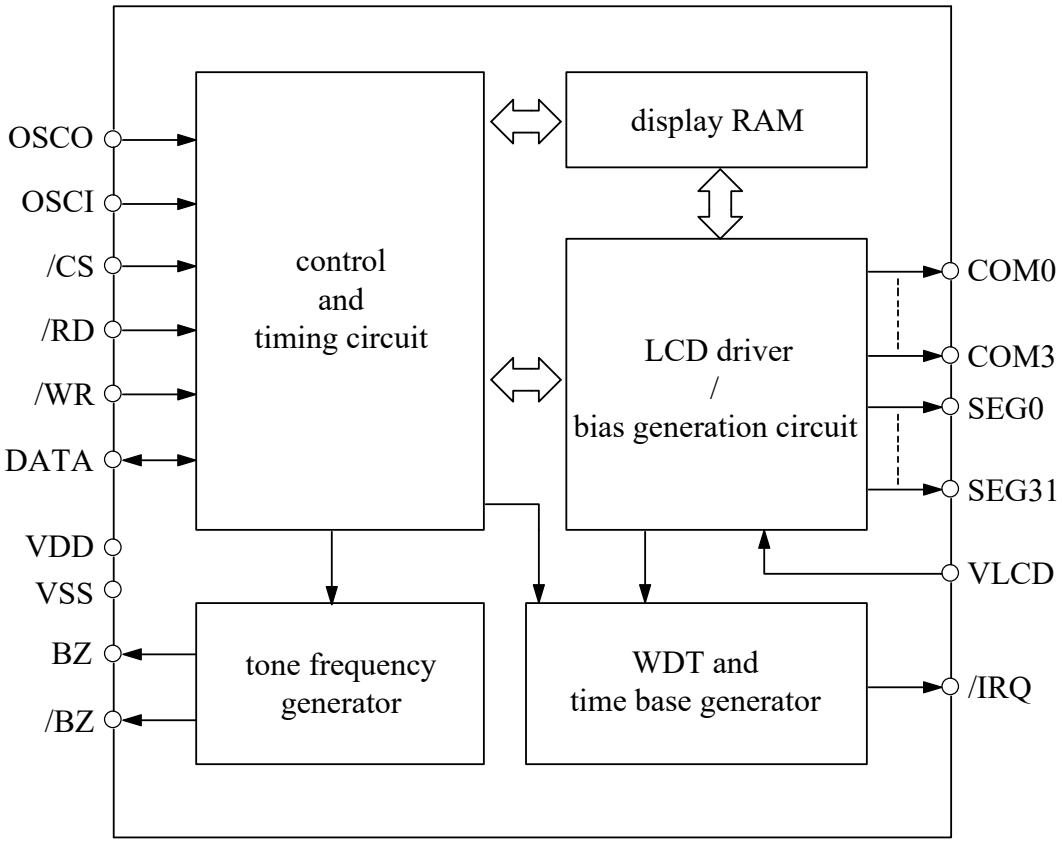
10.1 VK1621D/SDIP28 Pin Description

No.	Name	I/O	Function
1,2,3	SEG1,3,5	O	LCD SEG drive outputs
4	/CS	I	Chip select signal with pull-up resistor ,active low.
5	/RD	I	READ clock input with pull-up resistor, data out on the falling edge of the /RD signal.
6	/WR	I	Serial write signal with pull-up resistor, data latched on the rising edge of the /WR signal.
7	DATA	I/O	Serial data signal with pull-up resistor, input/output depending on access mode.
8	VSS	VSS	Negative power supply
9	VLCD	I	LCD driving voltage input,must be ≤VDD
10	VDD	VDD	Positive power supply
11	/IRQ	O	Time base or WDT overflow flag, NMOS open drain output.
12	BZ	O	2kHz or 4kHz tone frequency output, when TONE OFF the BZ pin output low level
13-15	COM0-COM2	O	LCD COM drive outputs
16-28	SEG31,29,27, 25,23,21,19, 17,15,13,11, 9,SEG7	O	LCD SEG drive outputs

11 Functional Description

11.1 Block Diagram



11.2 Display RAM

The VK1621S-1 integrates 32 × 4-bit RAM for LCD display. directly mapped to SEGx/COMx segments. Data is latched and updated on the LCD according to scan timing set by the system configuration. The display RAM can be accessed using three commands: READ, WRITE, and READ-MODIFY-WRITE. Each RAM address corresponds to a specific combination of SEG and COM lines.

The following is a mapping from the RAM to the LCD pattern:

	COM3	COM2	COM1	COM0		
SEG0					0	address 6 bit （A5----A0）
SEG1					1	
SEG2					2	
SEG3					3	
⋮					⋮	
SEG31					31	
	D3	D2	D1	D0	Data\Addr	

11.3 System Oscillator

The VK1621 system clock is used to generate the time base/Watchdog Timer (WDT) clock, LCD driving clock, and tone signal.

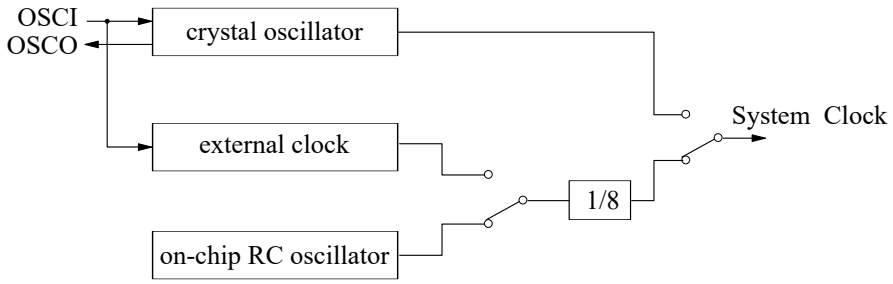
It supports three sources: an internal RC oscillator (default), a 32.768 kHz external crystal (connected to OSCI/OSCO), or an external clock signal input via OSCI (e.g., 256 kHz clock from an MCU GPIO).

After executing the SYS DIS command, the system clock stops, the LCD bias generator shuts down, and the LCD display goes blank. The time base and WDT functions are also disabled. However, the SYS DIS command only applies when the system clock is sourced from the internal RC or crystal oscillator. If an external clock is selected, SYS DIS does not disable the oscillator or trigger Power-down mode.

The LCD OFF command disables the LCD bias generator. When combined with SYS DIS, it reduces power consumption and effectively enters Power-down mode.

Upon system power-up, the VK1621 defaults to the SYS DIS state.

System Oscillator Configuration：



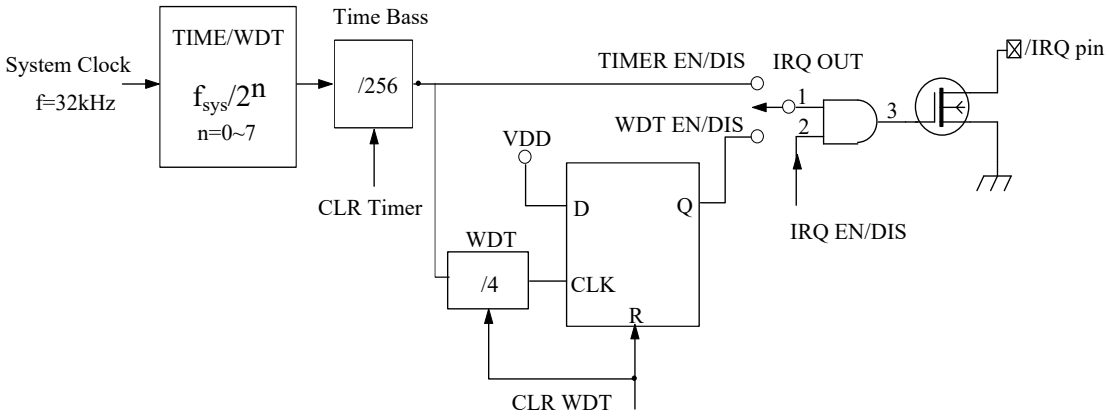
11.4 Time Base and WDT

The time base generator consists of an 8-stage ripple counter and provides accurate timing functionality. The Watchdog Timer (WDT) comprises the 8-stage time base plus an additional 2-stage counter. It helps reset or interrupt the host system in case of abnormal operation, such as unexpected jumps or execution errors. A WDT timeout sets an internal status flag. Both the time base overflow and WDT timeout flags can be routed to the /IRQ pin through software configuration. Eight frequency division options are available for the time base and WDT clock, derived using the formula:

$$f_{WDT}=fsys/2^n \quad (n=0\sim7) \quad fsys=32kHz$$

The time base generator and the Watchdog Timer (WDT) share the same 8-stage counter. The WDT is cleared by executing the CLR WDT command, while the time base generator can be cleared using either the CLR WDT or the CLR TIMER command. Executing the WDT EN command enables both the time base generator and the WDT timeout flag output, which can be routed to the /IRQ pin. Conversely, executing the WDT DIS command disables the time base generator. After the TIMER EN command is issued, the WDT is disconnected from the /IRQ pin, and the time base overflow signal is instead connected to it. The /IRQ output can be globally enabled or disabled using the IRQ EN and IRQ DIS commands, respectively.By default, the /IRQ output is disabled upon system power-up

Timer and WDT Configurations:



11.5 Tone Output

The VK1621 integrates a basic tone generator capable of producing 2 kHz or 4 kHz output signals. The output consists of a differential pair: BZ and /BZ, designed to drive a passive piezoelectric buzzer. Use the TONE 2K or TONE 4K commands to select the desired tone frequency. Tone output can be enabled or disabled via the TONE ON or TONE OFF commands. When the tone function is disabled or the system is powered down, both BZ and /BZ will remain at low level.

11.6 LCD Driver

The VK1621 is a 128-segment LCD driver (32SEG × 4 COM). It supports software-configurable bias settings of 1/2 or 1/3, and COM configurations of 2, 3, or 4.

11.7 Communication Interfacing

The VK1621 communicates with the host via a 3-wire or 4-wire serial interface.

When used solely for display output, only 3 lines are required (/CS, /WR, and DATA);/RD is optional for reading.

- /CS: Chip select input. It enables the serial interface when low and terminates communication when high.
- /RD: Read clock input. On the falling edge, data is output from the device onto the DATA line.
- /WR: Write clock input. On the rising edge, data and commands from DATA are latched into the device.
- DATA: Bidirectional serial data line used to transfer both command and display data.
- /IRQ: Open-drain output pin for either WDT timeout or time base overflow flag, selectable via software.

11.8 Command Format

The VK1621 is configured via software commands that support two primary modes: command mode and data mode.

- Command mode is used to configure system-level parameters. It is identified by a command mode ID of 100.
- Data mode supports three types of memory operations: READ, WRITE, and READ-MODIFY-WRITE.

These commands allow the host controller to configure LCD behavior and access display RAM contents.

The following are the data mode IDs and the command mode ID:

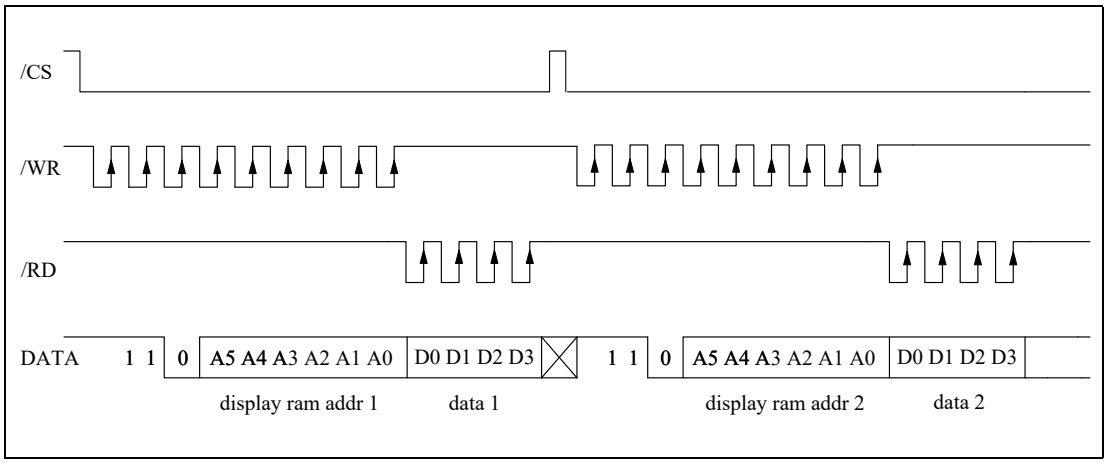
Command	MODE	ID
READ	DATA	110
WRITE	DATA	101
Read-Modify-Write	DATA	101
COMMAND	COMMAND	100

12 Cmd/Data Timing Diagram

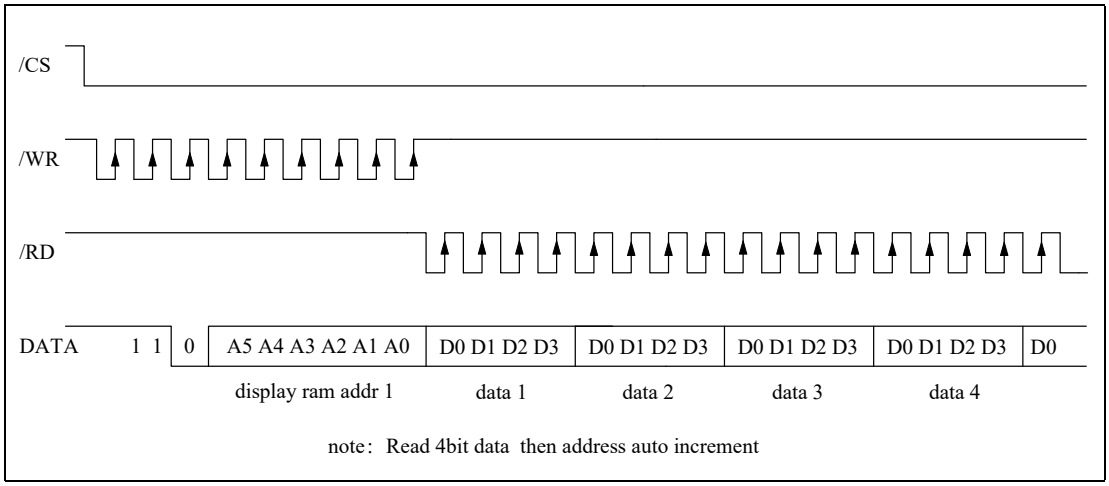
The following are the data mode IDs and the command mode ID Timing Diagrams.

12.1 READ Mode

Command Code : 110

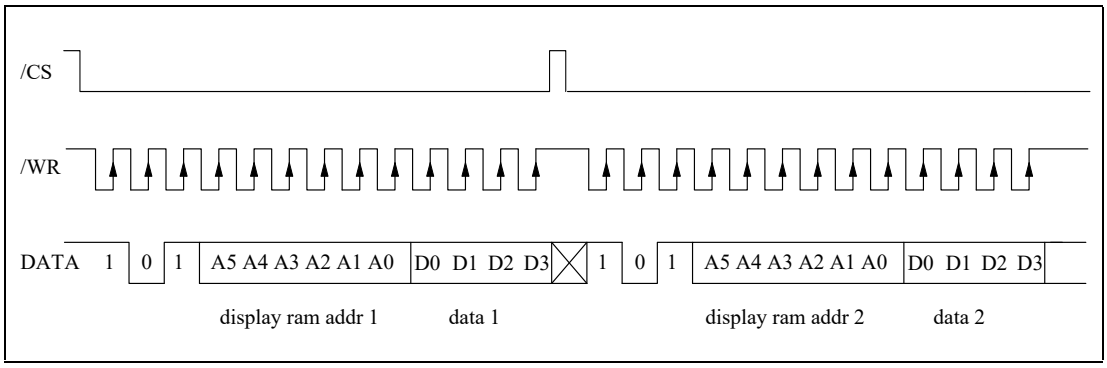


Successive Address Reading

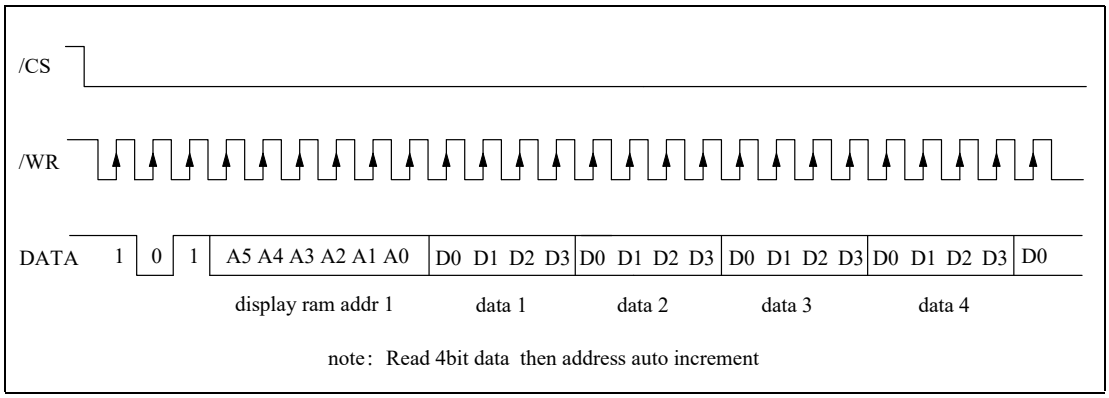


12.2 WRITE Mode

Command Code : 101

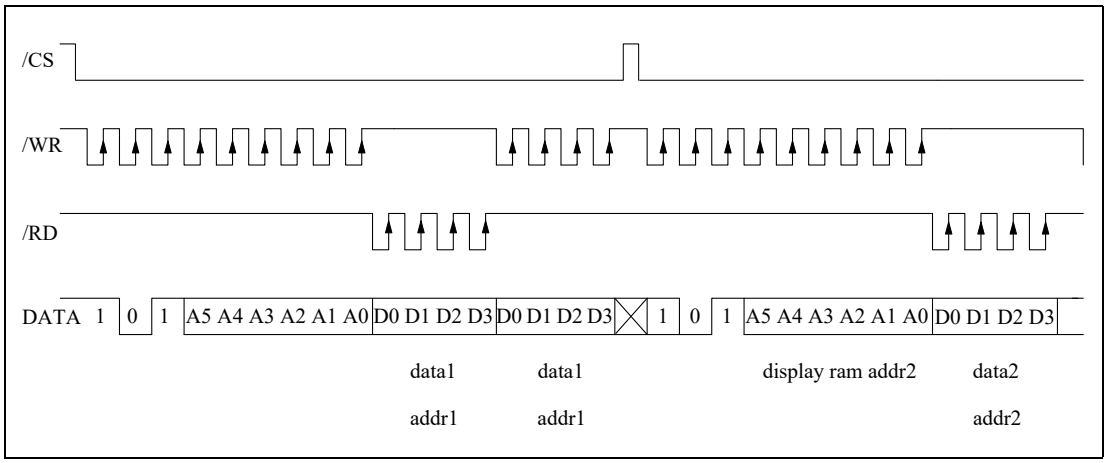


Successive Address Writing

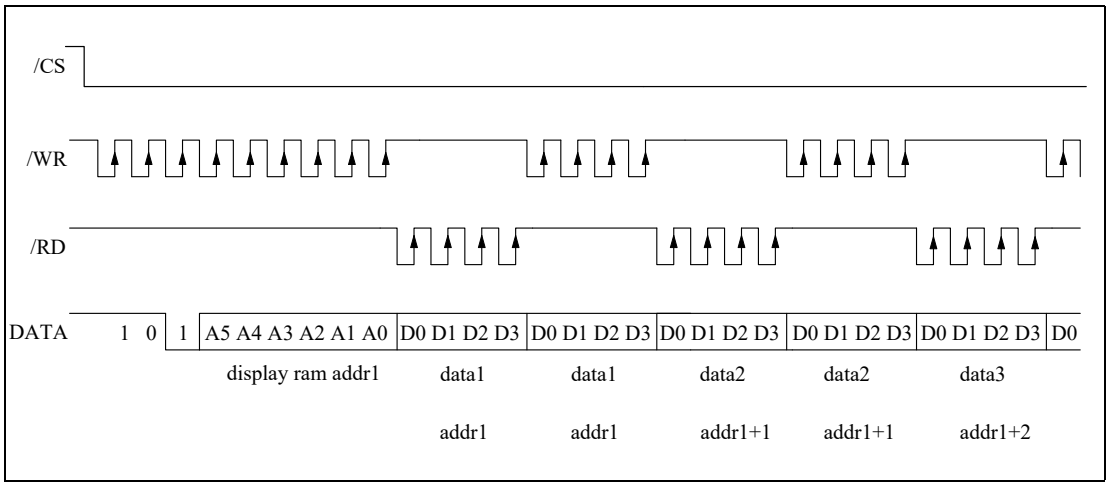


12.3 Read-Modify-Write Mode

Command Code : 101

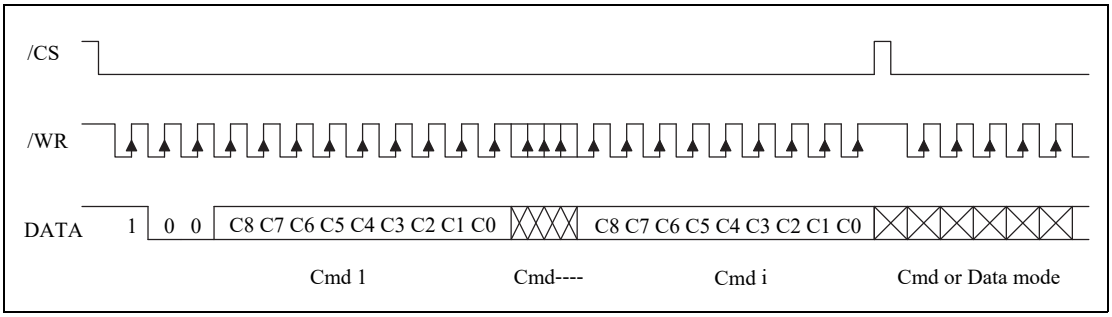


Successive Address Accessing



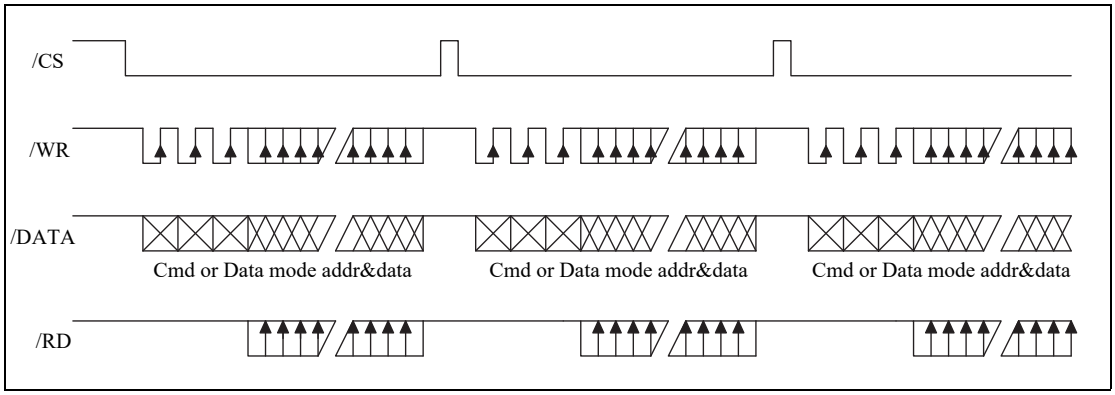
12.4 Command Mode

Command Code : 100



12.5 Data and Command Mode

Data and Command Mode



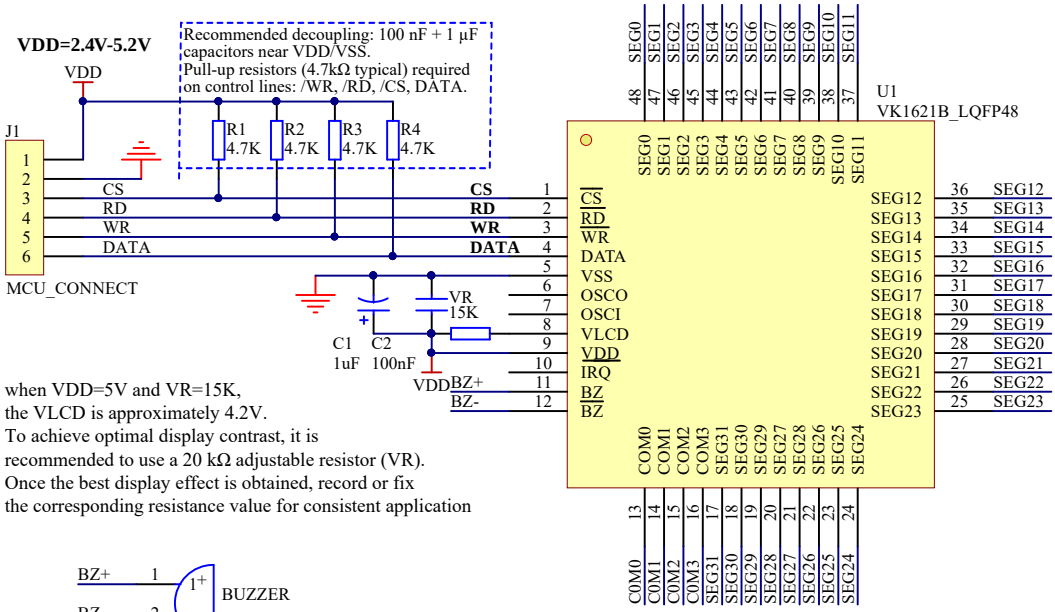
13 Command Summary

Name	ID	Command Code	D/C	Function	Def.
READ	110	A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	READ and WRITE to the RAM	
SYS DIS	100	0000-0000-X	C	Turn off system oscillator	YES
SYS EN	100	0000-0001-X	C	Turn on system oscillator	
LCD OFF	100	0000-0010-X	C	Turn off LCD bias generator	YES
LCD ON	100	0000-0011-X	C	Turn on LCD bias generator	
TIMERS DIS	100	0000-0100-X	C	Disable time base output	
WDT DIS	100	0000-0101-X	C	Disable WDT time-out flag outpu	
TIMER EN	100	0000-0110-X	C	Enable time base output	
WDT EN	100	0000-0111-X	C	Enable WDT time-out flag output	
TONE OFF	100	0000-1000-X	C	Turn off tone outputs	YES
TONE ON	100	0000-1001-X	C	Turn on tone outputs	
CLR TIMER	100	0000-11XX-X	C	Clear the contents of time base generator	
CLR WDT	100	0000-111X-X	C	Clear the contents of WDT stage	
XTAL 32k	100	0001-01XX-X	C	crystal oscillator	
RC 256k	100	0001-10XX-X	C	on-chip RC oscillator	YES
EXT 256k	100	0001-11XX-X	C	external clock source	
BIAS 1/2	100	0010-abX0-X	C	LCD 1/2bias option ab=00：2 COMS ab=01：3 COMS ab=10：4 COMS	
BIAS 1/3	100	0010-abX1-X	C	LCD 1/3 bias option ab=00：2 COMs ab=01：3 COMs ab=10：4 COMs	
TONE 4k	100	010X-XXXX-X	C	Tone frequency, 4kHz	
TONE 2k	100	011X-XXXX-X	C	Tone frequency, 2kHz	
IRQ DIS	100	100X-0XXX-X	C	Disable IRQ output	YES
IRQ EN	100	100X-1XXX-X	C	Enable IRQ output	
F1	100	101X-X000-X	C	Time base/WDT clock output:1Hz The WDT time-out flag after: 4s	
F2	100	101X-X001-X	C	Time base/WDT clock output:2Hz The WDT time-out flag after: 2s	
F4	100	101X-X010-X	C	Time base/WDT clock output:4Hz The WDT time-out flag after: 1s	
F8	100	101X-X011-X	C	Time base/WDT clock output:8Hz The WDT time-out flag after: 1/2s	
F16	100	101X-X100-X	C	Time base/WDT clock output:16Hz The WDT time-out flag after: 1/4s	
F32	100	101X-X101-X	C	Time base/WDT clock output:32Hz The WDT time-out flag after: 1/8s	
F64	100	101X-X110-X	C	Time base/WDT clock output:64Hz The WDT time-out flag after: 1/16s	
F128	100	101X-X111-X	C	Time base/WDT clock output:128Hz The WDT time-out flag after: 1/32s	YES
TEST	100	1110-0000- X	C	Test mode	
NORMAL	100	1110-0011- X	C	Normal mode	YES

note: X: 0 or 1
A5-A0: Display RAM addresses
D3-D0:4bit Display RAM data
D/C:Data/Command mode
Def.:Power on reset default
110,101and 100 is Command ID

14 Application Circuits

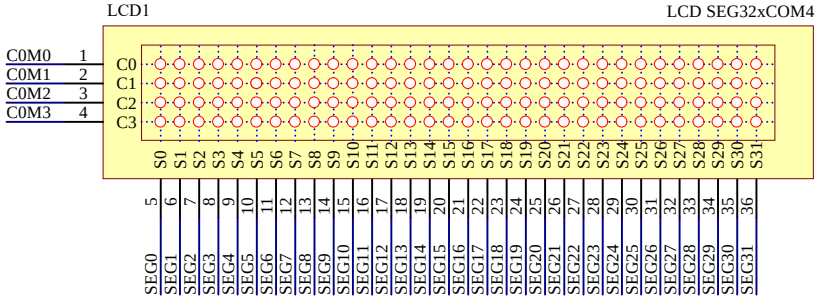
If only display output is needed, the /RD pin can be left floating.
In noisy environments, add a small series resistor (10Ω–1kΩ) and a pF - level capacitor to ground on each communication line.
If the MCU operates at 3.3V and VK1621 at 5V, a level shifting circuit is recommended on communication lines.

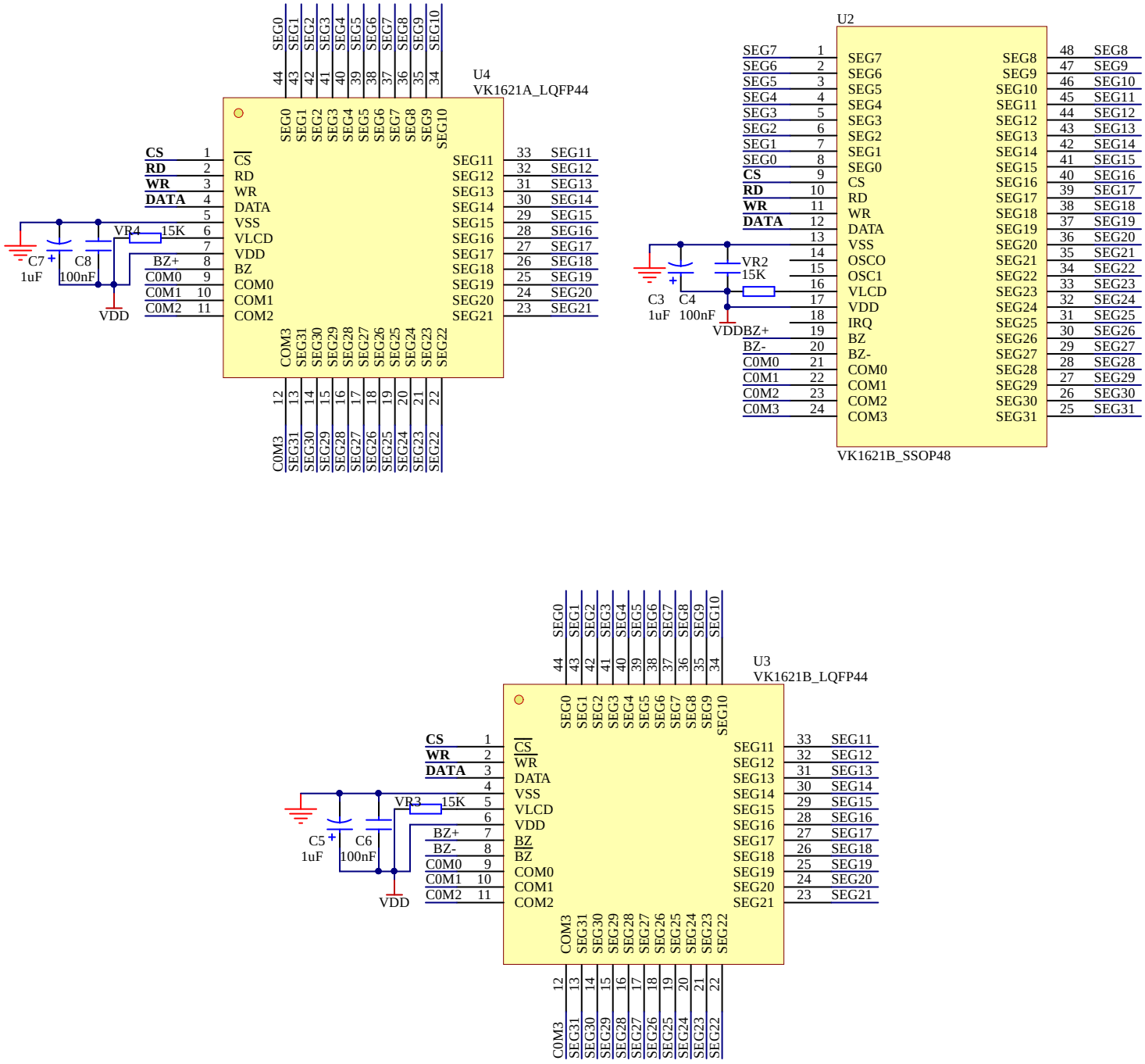


when VDD=5V and VR=15K,
the VLCD is approximately 4.2V.
To achieve optimal display contrast, it is recommended to use a 20 kΩ adjustable resistor (VR).
Once the best display effect is obtained, record or fix the corresponding resistance value for consistent application

BZ and /BZ are used to drive a passive piezoelectric buzzer.
Typical output frequency: 2 kHz or 4 kHz.
Recommended buzzer voltage: ≤ 5V, drive current < 1 mA.

If only display output is needed, the /RD pin can be left floating.
It is recommended to connect COM pins to the LCD in order (COM0 → COM3).
SEG pins can be reassigned for routing convenience, but must match software RAM mapping




U4
VK1621A_LQFP44
U2
VK1621B_SSOP48
U3
VK1621B_LQFP44
CS
RD
WR
DATA
VSS
VLCD
VDD
BZ
COM0
COM1
COM2
COM3
BZ+
BZ-
C0M0
C0M1
C0M2
C0M3
SEG0
SEG1
SEG2
SEG3
SEG4
SEG5
SEG6
SEG7
SEG8
SEG9
SEG10
SEG11
SEG12
SEG13
SEG14
SEG15
SEG16
SEG17
SEG18
SEG19
SEG20
SEG21
SEG22
SEG23
SEG24
SEG25
SEG26
SEG27
SEG28
SEG29
SEG30
SEG31
OSCO
OSC1
IRQ
VR4
VR2
VR3
15K
C7
1uF
C8
100nF
C3
C4
C5
C6

15 Electrical Characteristics

15.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3～5.5	V
Input Voltage	VIN	V_{SS}-0.3～V_{DD}+0.3	V
Storage Temperature	T_{STG}	-50～+125	℃
Operating Temperature	T_{OTG}	-40～+85	℃

15.2 DC Electrical Characteristics

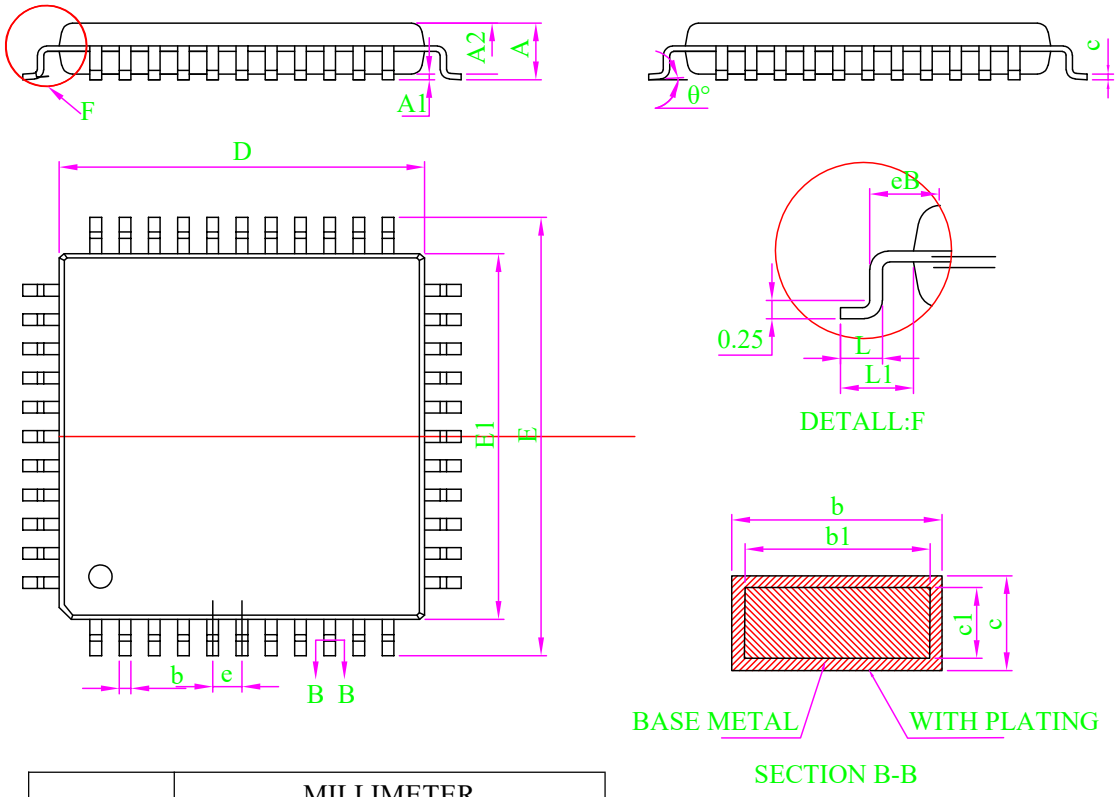
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	2.4	—	5.2	V	—	—
Operating current	I_{DD1}	—	150	300	μA	3V	No load/LCD ON On-chip RC oscillator
		—	300	600		5V	
Operating current	I_{DD2}	—	60	120	μA	3V	No load/LCD ON Crystal oscillator
		—	120	240		5V	
Operating current	I_{DD3}	—	100	200	μA	3V	No load/LCD ON External clock source
		—	200	400		5V	
Standby Current	I_{STB}	—	0.1	5	μA	3V	No load, Power down mode
		—	0.3	10		5V	
Low-level Input	V_{IL}	0	—	0.6	V	3V	DATA, /WR, /CS,/RD
		0	—	1.0		5V	
High-level Input	V_{IH}	2.4	—	3.0	V	3V	DATA, /WR, /CS,/RD
		4.0	—	5.0		5V	
DATA, BZ, /BZ, /IRQ	I_{OL1}	0.5	1.2	—	mA	3V	V_{OL}=0.3V
		1.3	2.6	—		5V	V_{OL}=0.5V
DATA, BZ, /BZ	I_{OH1}	-0.4	-0.8	—	mA	3V	V_{OH}=2.7V
		-0.9	-1.8	—		5V	V_{OH}=4.5V
LCD COM Sink Current	I_{OL2}	80	150	—	μA	3V	V_{OL}=0.3V
		150	250	—		5V	V_{OL}=0.5V
LCD COM Source Current	I_{OH2}	-80	-120	—	μA	3V	V_{OH}=2.7V
		-120	-200	—		5V	V_{OH}=4.5V
LCD SEG Sink Current	I_{OL3}	60	120	—	μA	3V	V_{OL}=0.3V
		120	200	—		5V	V_{OL}=0.5V
LCD SEG Source Current	I_{OH3}	-40	-70	—	μA	3V	V_{OH}=2.7V
		-70	-100	—		5V	V_{OH}=4.5V
Pull-UP Resistor	R_{UP}	40	80	150	kΩ	3V	DATA, /WR, /CS,/RD
		30	60	100		5V	

15.3 AC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
System Clock	f_{SYS1}	—	256	—	kHz	3V	On-chip RC oscillator
		—	256	—		5V	On-chip RC oscillator
System Clock	f_{SYS2}	—	32.768	—	kHz	3V	Crystal oscillator
		—	32.768	—		5V	
System Clock	f_{SYS3}	—	256	—	kHz	3V	External clock source
		—	256	—		5V	
LCD Clock	f_{LCD1}	—	$f_{SYS1}/1024$	—	Hz	—	On-chip RC oscillator
		—	$f_{SYS2}/128$	—			Crystal oscillator
		—	$f_{SYS3}/1024$	—			External clock source
LCD Common Period	t_{COM}	—	n/ f_{LCD}	—	sec	—	N：Number of COM
Serial Data Clock(/WR)	F_{CLK1}	—		150	kHz	3V	Duty cycle 50%
		—		300		5V	
Serial Data Clock(/RD)	F_{CLK2}	—		75	kHz	3V	Duty cycle 50%
		—		150		5V	
Serial Interface Reset PW	t_{CS}	—	250	—	ns	—	/CS
/WR, /RD Input Pulse Width	t_{CLK}	3.34	—	—	μS	3V	Write mode
		6.67	—	—			Read mode
		1.67	—	—	μS	5V	Write mode
		3.34	—	—			Read mode
Rise/Fall Time Serial Data Clock Width	t_r，t_f	—	120	—	ns	3V	—
						5V	
Setup Time for DATA to /WR, /RD Clock Width	t_{su}	—	120	—	ns	3V	—
						5V	
Hold Time for DATA to /WR, /RD Clock Width	t_h	—	120	—	ns	3V	—
						5V	
Setup Time for /CS to /WR, /RD Clock Width	t_{su1}	—	100	—	ns	3V	—
						5V	
Hold Time for /CS to /WR, /RD Clock Width	t_{h1}	—	100	—	ns	3V	—
						5V	

16 Package Information

16.1 LQFP44(10.0mm x 10.0mm PP=0.8mm)

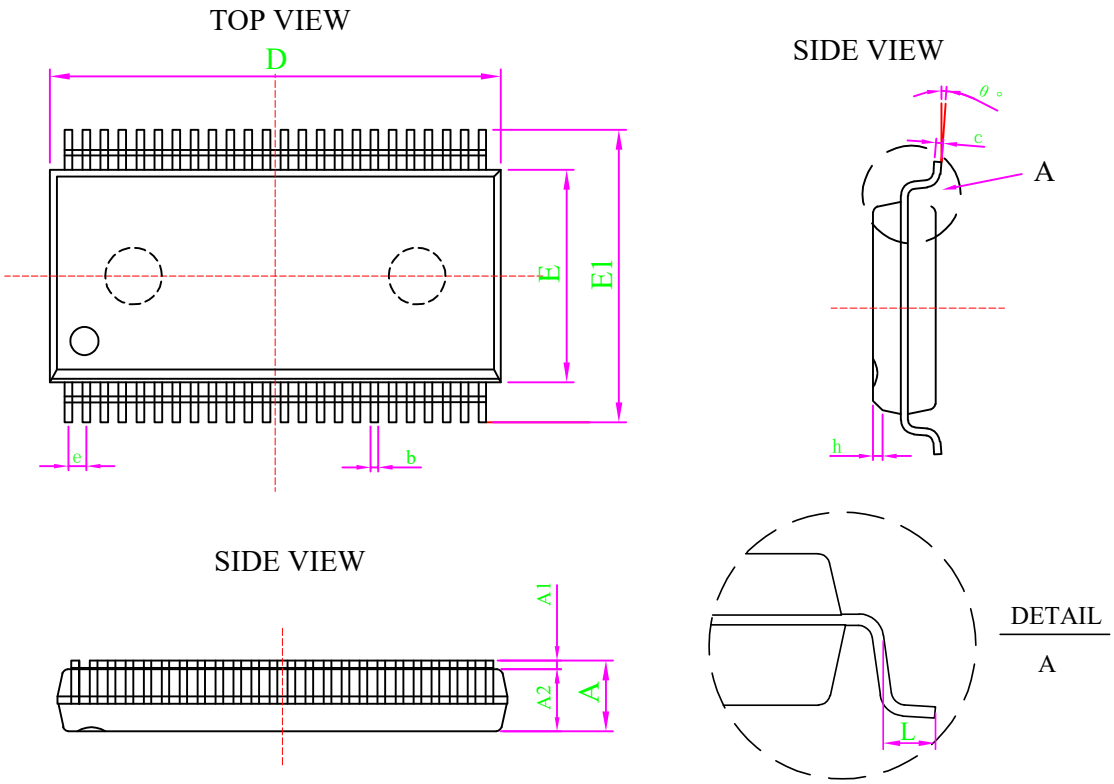


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.70
A1	0.10	0.15	0.20
A2	1.30	1.40	1.50
b	0.28	-	0.36
b1	0.27	0.30	0.33
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	9.90	10.00	10.10
E	11.80	12.00	12.20
eB	11.05	-	11.30
E1	9.90	10.00	10.10
e	0.80 BSC		
L	0.42	0.57	0.72
L1	0.95	1.00	1.15
θ	0	-	8°

Note:

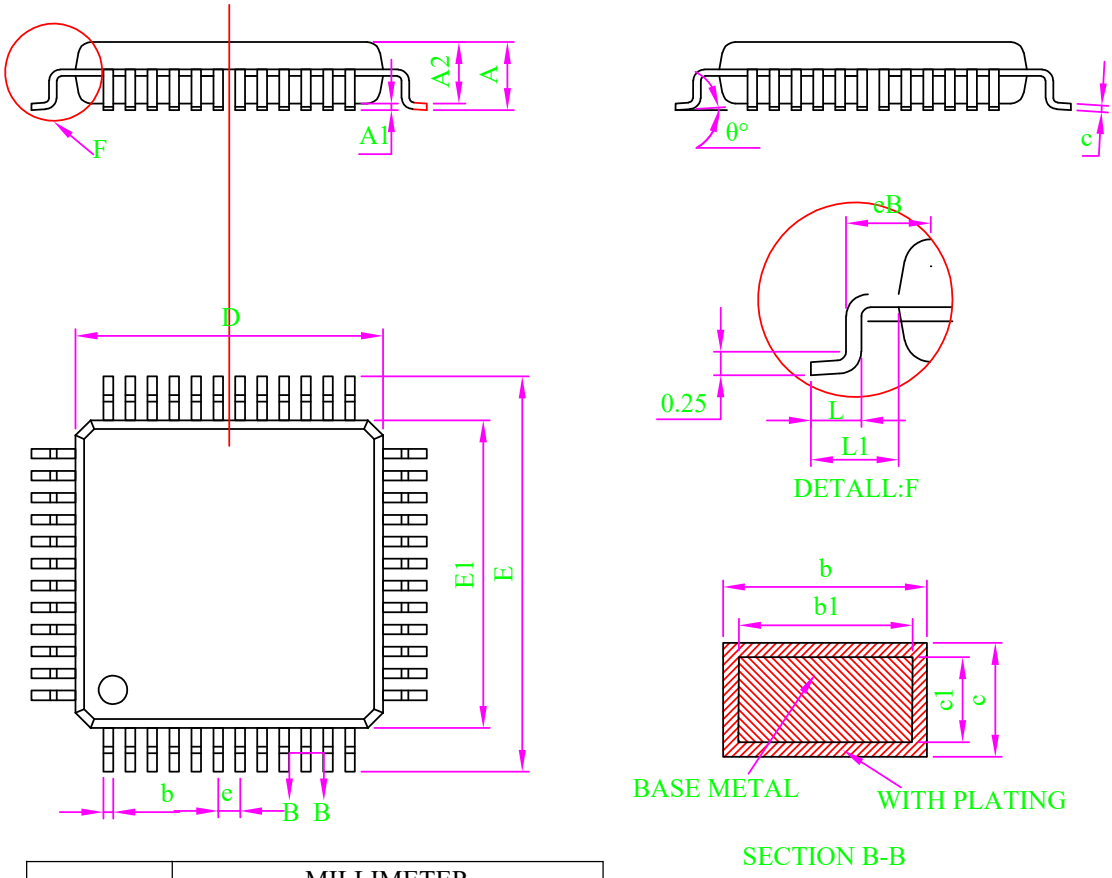
1. All dimension are in mm.
2. Dim D&El does not include plastic flash; Flash: Plastic residual around body edge after de junk/singulation.
3. Dim b does not include dambar protrusion/intrusion.
4. Plating thickness 0.007mm-0.015mm

16.2 SSOP48 (300mil) (15.9mm×7.5mm PP=0.635mm)



Dimensions			
SYMBOL	MIN	NOMINAL	MAX
A	—	—	2.80
A1	0.20	0.30	0.40
A2	2.20	2.30	2.40
b	0.24	—	0.33
c	0.14	—	0.25
D	15.80	15.90	16.00
E	7.40	7.5	7.60
E1	10.10	10.30	10.50
e	0.635BSC		
L	0.61	—	0.91
h	0.30	—	0.50
	0°	—	8°

16.3 LQFP48（7.0mm × 7.0mm PP=0.5mm）

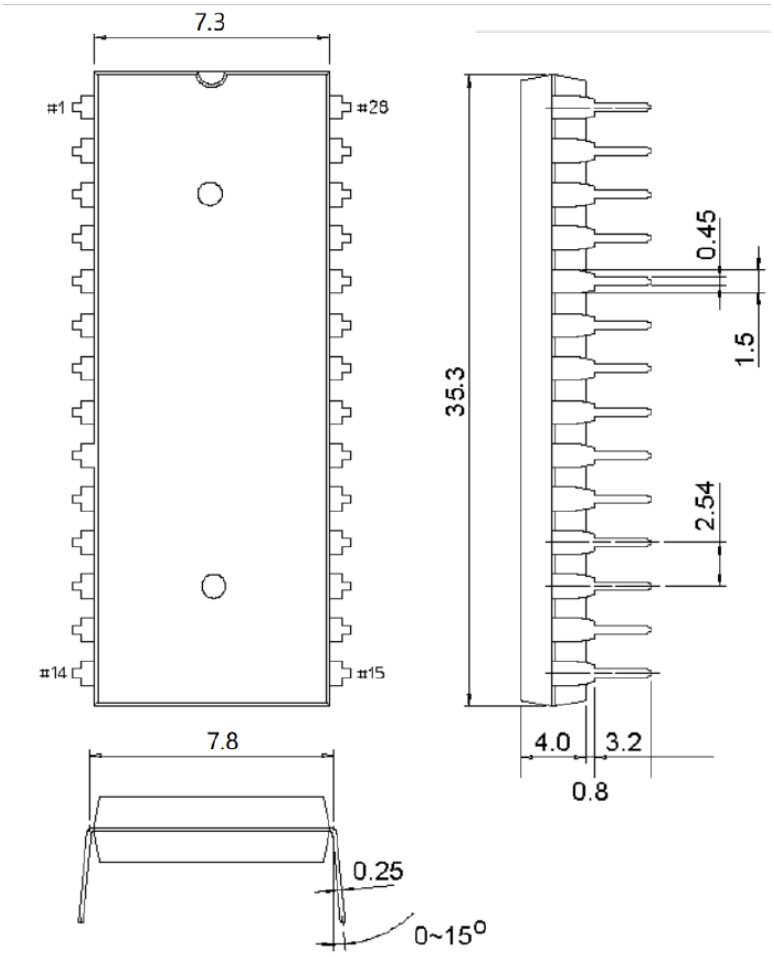


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.70
A1	0.10	0.15	0.20
A2	1.30	1.40	1.50
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	6.90	7.00	7.10
E	8.80	9.00	9.20
eB	8.10	-	8.28
E1	6.90	7.00	7.10
e	0.50 BSC		
L	0.42	0.57	0.72
L1	0.90	1.00	1.10
θ	0	-	10°

Note:

1. All dimension are in mm.
2. Dim D&El does not include plastic flash； Flash: Plastic residual around body edge after de junk/singulation.
3. Dim b does not include dambar protrusion/intrusion.
4. Plating thickness 0.007mm-0.015mm

16.4 SDIP28：(288mil)(35.3mm×7.3mm PP=2.54mm)



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18 Revision History

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	initial release	YES
2	1.1	2018-10-11	Add reference circuit	YES
3	1.2	2019-03-21	Alignment correction	YES
4	1.3	2025-06-16	Change Description	YES

[1] Please refer to the latest version of this document before starting or finalizing any design.

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