



VK1128C Datasheet

32×4 LCD DRIVER

Rev.1.3

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1 General Description

The VK1128C is a dot-matrix story-mapped LCD driver that supports LCD screens with a maximum of 128 dots (32SEG×4COM), as well as 2COM and 3COM LCD screens. The single-chip microcomputer can be configured to display parameters and send display data through 3/4 of the communication pins, and can also enter power-saving mode through instructions.

2 Key Features

- Operating voltage: 2.4-5.2V
- Integrated RC oscillator (default)
- External crystal input: 32.768 kHz (OSCO, OSC1)
- External clock source: 256 kHz (OSCI)
- Selectable LCD bias: 1/2 or 1/3
- Selectable LCD duty: 1/2, 1/3, or 1/4
- Built-in 32 × 4 bit display RAM
- Configurable buzzer output: 2 kHz or 4 kHz
- Power-down mode via software command(LCD OFF, SYS DIS)
- Eight selectable clock sources for time base / WDT
- WDT or time base overflow flag output via /IRQ pin
- 3 wire or 4 wire serial communication interface
- Software-configurable of LCD parameters
- Auto-increment addressing for sequential read/write
- Dual command formats for configuration and access
- Three RAM accessing modes
- VLCD adjustable via external pin (\leq VDD)
- Available Packages:
QFN48L (5.0mm × 5.0mm PP=0.35mm)

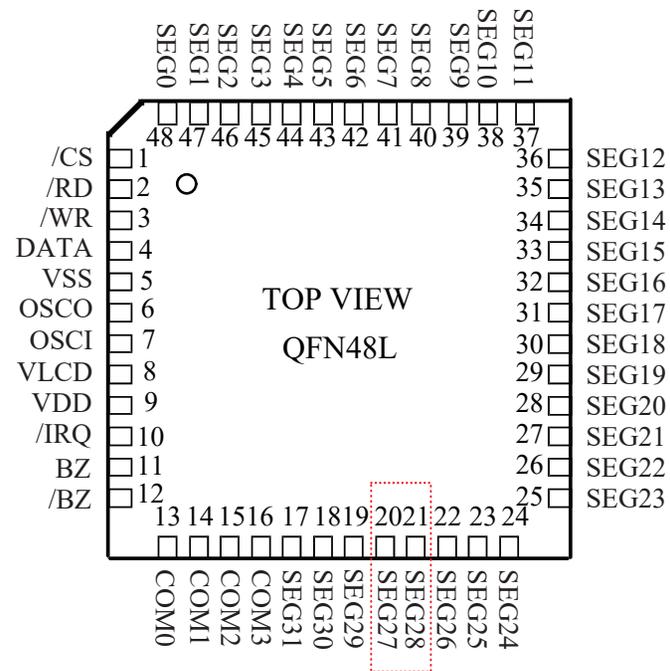
3 Product Selection

Part No.	SEG × COM	BIAS	DUTY	Packaging
VK1024B	6×4,6×3,6×2	1/2,1/3	1/2,1/3,1/4	SOP16
VK1056B	14×4,14×3,14×2	1/2,1/3	1/2,1/3,1/4	SOP24
VK1056C	14×4,14×3,14×2	1/2,1/3	1/2,1/3,1/4	SSOP24
VK1056Q	14×4,14×3,14×2	1/2,1/3	1/2,1/3,1/4	QFN24L
VK1072B	18×4,18×3,18×2	1/2,1/3	1/2,1/3,1/4	SOP28
VK1072C	18×4,18×3,18×2	1/2,1/3	1/2,1/3,1/4	SOP28
VK1072D	18×4,18×3,18×2	1/2,1/3	1/2,1/3,1/4	SSOP28
VK1088B	22×4,22×3,22×2	1/2,1/3	1/2,1/3,1/4	QFN32L
VK1128C	32×4,32×3,32×2	1/2,1/3	1/2,1/3,1/4	QFN48L

4 Ordering Information

Part No.	Packaging	Tube Qty	Tray Qty	Box Qty	Total Qty	Notes
VK1024B	SOP16	50/tube		10000/box	100000 PCS	
VK1056B	SOP24	30/tube		2400/box	24000 PCS	
VK1056C	SSOP24	60/tube		6000/box	60000 PCS	
VK1056Q	QFN24L		490/tray	4900/box	29400 PCS	
VK1072B	SOP28	26/tube		2080/box	20800 PCS	
VK1072C	SOP28	26/tube		2080/box	20800 PCS	
VK1072D	SSOP28	50/tube		5000/box	50000 PCS	
VK1088B	QFN32L			3000/box	24000 PCS	
VK1128C	QFN48L		3000/tray		24000 PCS	

5 Package Pinout Information(QFN48L)



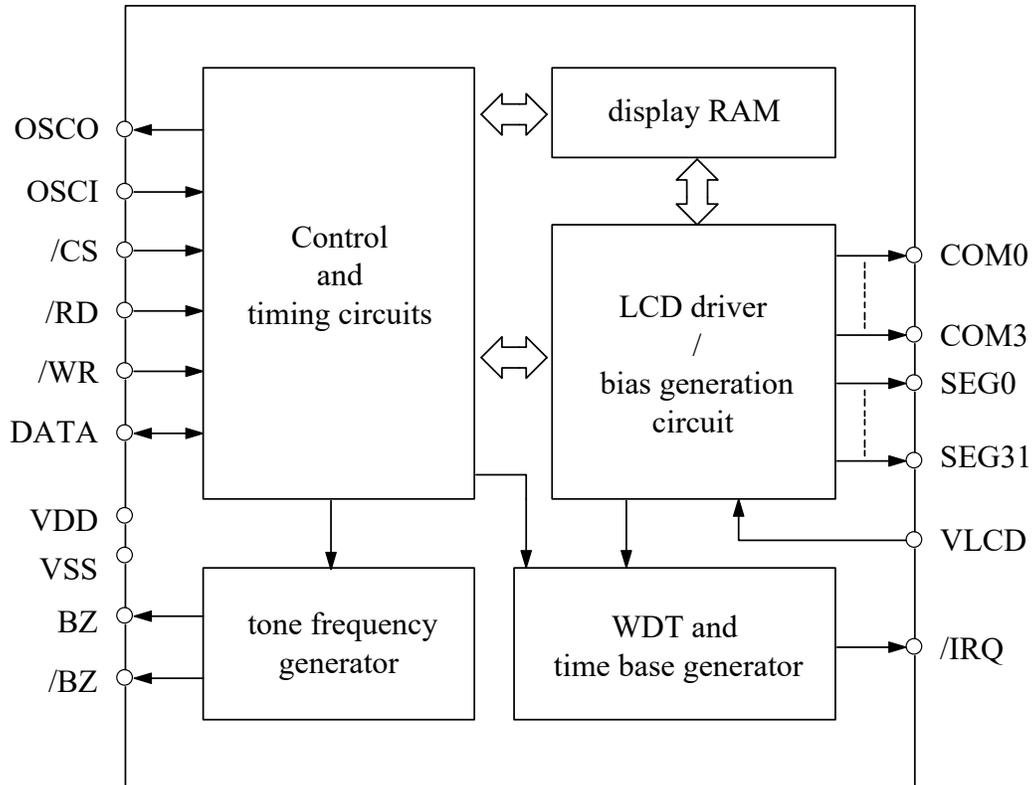
For more information: [Page 17](#)

5.1 VK1128C/QFN48L Pin Description

No.	Name	I/O	Function
1	/CS	I	Chip select signal with pull-up resistor ,active low.
2	/RD	I	Serial read signal with pull-up resistor, data out on the falling edge of the /RD signal.
3	/WR	I	Serial write signal with pull-up resistor, data latched on the rising edge of the /WR signal.
4	DATA	I/O	Serial data signal with pull-up resistor, input/output depending on access mode.
5	VSS	VSS	Negative power supply
6	OSCO	O	Crystal oscillator: OSCI and OSCO pins are connected to a 32.768kHz crystal
7	OSCI	I	External clock source: OSCI pin is connected to a, external clock source On-chip RC oscillator: the OSCI and OSCO pins can be left open.
8	VLCD	I	LCD driving voltage input,must be $\leq VDD$
9	VDD	VDD	Positive power supply
10	/IRQ	O	Time base or WDT overflow flag, NMOS open drain output.
11	BZ	O	2kHz or 4kHz tone frequency output pair, when TONE OFF the BZ and /BZ pins output low level.
12	/BZ	O	
13-16	COM0-COM3	O	LCD COM drive outputs
17-48	SEG31-SEG8	O	LCD SEG drive outputs

6 Functional Description

6.1 Block Diagram



6.2 Display RAM

The VK1128C integrates 32×4 -bit RAM for LCD display, directly mapped to SEGx/COMx segments. Data is latched and updated on the LCD according to scan timing set by the system configuration. The display RAM can be accessed using three commands: READ, WRITE, and READ-MODIFY-WRITE. Each RAM address corresponds to a specific combination of SEG and COM lines.

The following is a mapping from the RAM to the LCD pattern:

	COM3	COM2	COM1	COM0		address 6 bit (A5---A0)
SEG0					0	
SEG1					1	
SEG2					2	
SEG3					3	
⋮					⋮	
SEG31					31	
	D3	D2	D1	D0	Data\Addr	

6.3 System Oscillator

The VK1128C system clock is used to generate the time base/Watchdog Timer (WDT) clock, LCD driving clock, and tone signal.

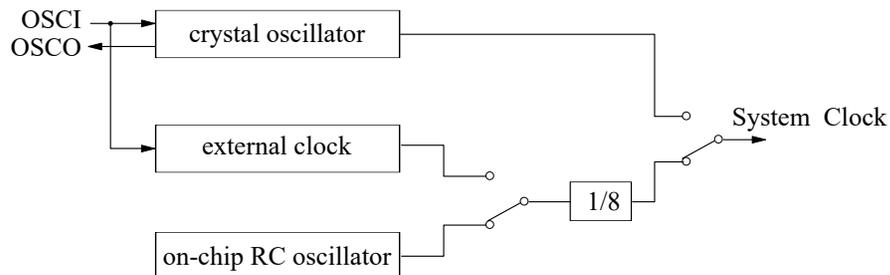
It supports three sources: an internal RC oscillator (default), a 32.768 kHz external crystal (connected to OSCI/OSCO), or an external clock signal input via OSCI (e.g., 256 kHz clock from an MCU GPIO).

After executing the SYS DIS command, the system clock stops, the LCD bias generator shuts down, and the LCD display goes blank. The time base and WDT functions are also disabled. However, the SYS DIS command only applies when the system clock is sourced from the internal RC or crystal oscillator. If an external clock is selected, SYS DIS does not disable the oscillator or trigger Power-down mode.

The LCD OFF command disables the LCD bias generator. When combined with SYS DIS, it reduces power consumption and effectively enters Power-down mode.

Upon system power-up, the VK1128C defaults to the SYS DIS state.

System Oscillator Configuration:



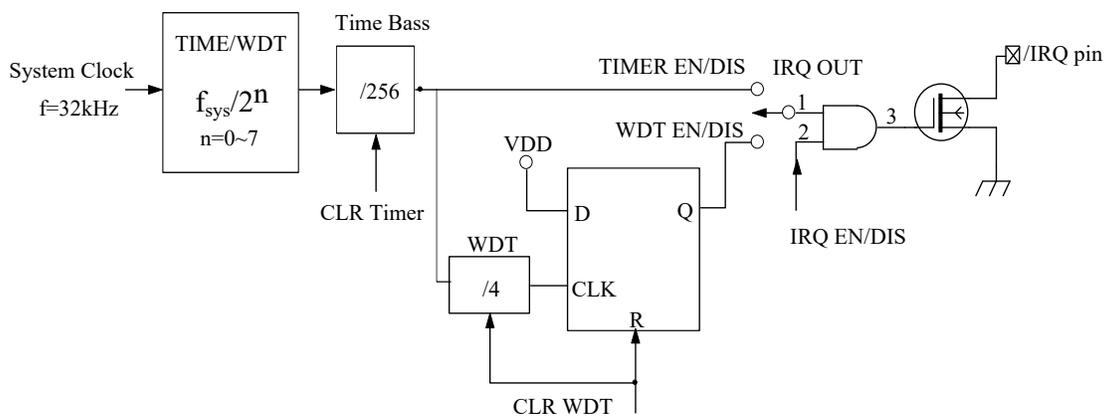
6.4 Time Base and WDT

The time base generator consists of an 8-stage ripple counter and provides accurate timing functionality. The Watchdog Timer (WDT) comprises the 8-stage time base plus an additional 2-stage counter. It helps reset or interrupt the host system in case of abnormal operation, such as unexpected jumps or execution errors. A WDT timeout sets an internal status flag. Both the time base overflow and WDT timeout flags can be routed to the /IRQ pin through software configuration. Eight frequency division options are available for the time base and WDT clock, derived using the formula:

$$f_{\text{WDT}} = f_{\text{sys}} / 2^n \quad (n=0\sim7) \quad f_{\text{sys}} = 32\text{kHz}$$

The time base generator and the Watchdog Timer (WDT) share the same 8-stage counter. The WDT is cleared by executing the CLR WDT command, while the time base generator can be cleared using either the CLR WDT or the CLR TIMER command. Executing the WDT EN command enables both the time base generator and the WDT timeout flag output, which can be routed to the /IRQ pin. Conversely, executing the WDT DIS command disables the time base generator. After the TIMER EN command is issued, the WDT is disconnected from the /IRQ pin, and the time base overflow signal is instead connected to it. The /IRQ output can be globally enabled or disabled using the IRQ EN and IRQ DIS commands, respectively. By default, the /IRQ output is disabled upon system power-up

Timer and WDT Configurations :



6.5 Tone Output

The VK1128C integrates a basic tone generator capable of producing 2 kHz or 4 kHz output signals. The output consists of a differential pair: BZ and /BZ, designed to drive a passive piezoelectric buzzer. Use the TONE 2K or TONE 4K commands to select the desired tone frequency. Tone output can be enabled or disabled via the TONE ON or TONE OFF commands. When the tone function is disabled or the system is powered down, both BZ and /BZ will remain at low level.

6.6 LCD Driver

The VK1128C is a 128-segment LCD driver (32SEG × 4 COM). It supports software-configurable bias settings of 1/2 or 1/3, and COM configurations of 2, 3, or 4.

6.7 Communication Interfacing

The VK1128C communicates with the host via a 3-wire or 4-wire serial interface.

When used solely for display output, only 3 lines are required (/CS, /WR, and DATA); /RD is optional for reading.

- /CS: Chip select input. It enables the serial interface when low and terminates communication when high.
- /RD: Read clock input. On the falling edge, data is output from the device onto the DATA line.
- /WR: Write clock input. On the rising edge, data and commands from DATA are latched into the device.
- DATA: Bidirectional serial data line used to transfer both command and display data.
- /IRQ: Open-drain output pin for either WDT timeout or time base overflow flag, selectable via software.

6.8 Command Format

The VK1128C is configured via software commands that support two primary modes: command mode and data mode.

- Command mode is used to configure system-level parameters. It is identified by a command mode ID of 100.
- Data mode supports three types of memory operations: READ, WRITE, and READ-MODIFY-WRITE.

These commands allow the host controller to configure LCD behavior and access display RAM contents.

The following are the data mode IDs and the command mode ID:

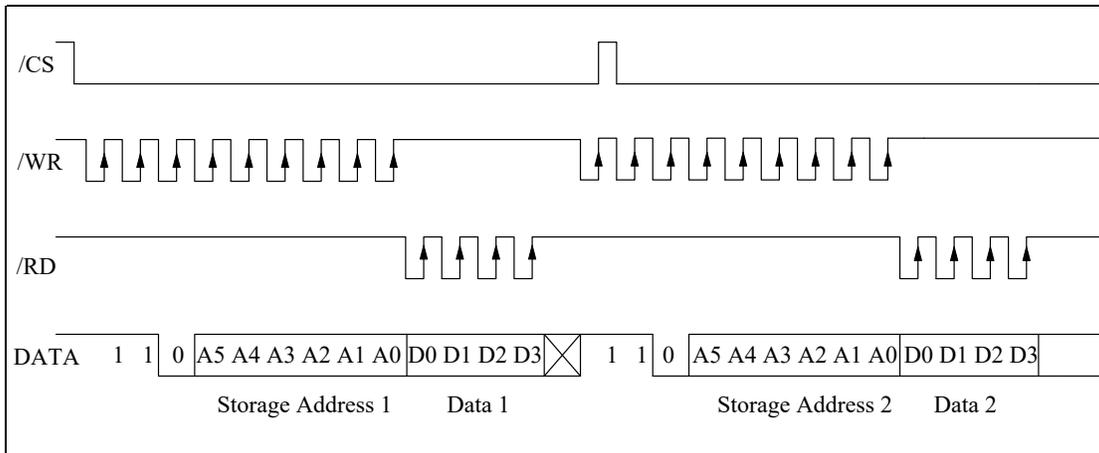
Command	MODE	ID
READ	DATA	110
WRITE	DATA	101
Read-Modify-Write	DATA	101
COMMAND	COMMAND	100

7 CMD/Data Timing Diagrams

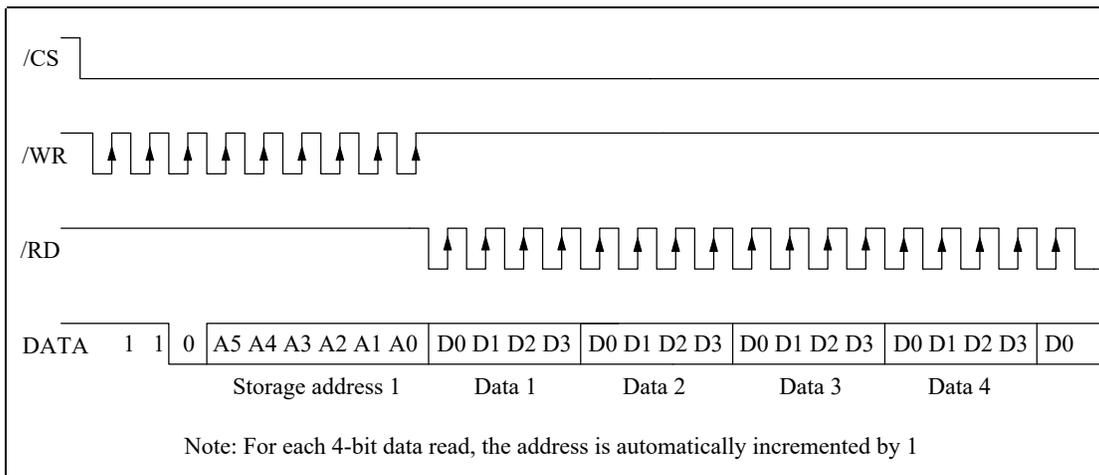
The command sequence corresponds to four ID codes.

7.1 READ Mode

Command Code : 110

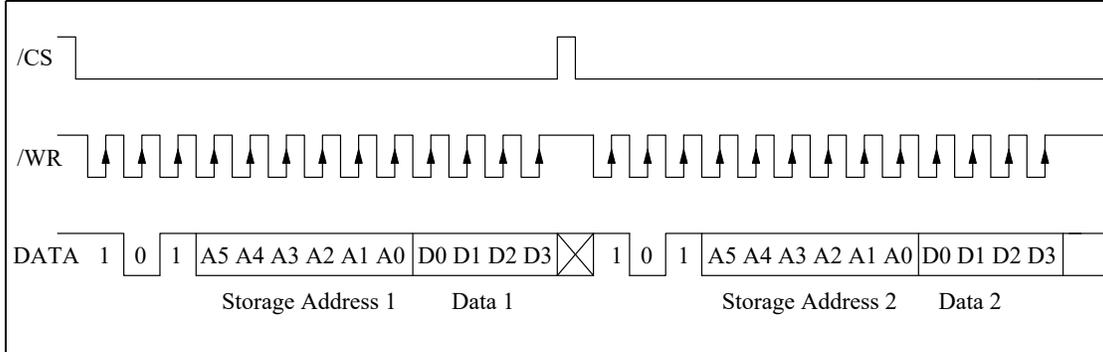


Successive Address Reading

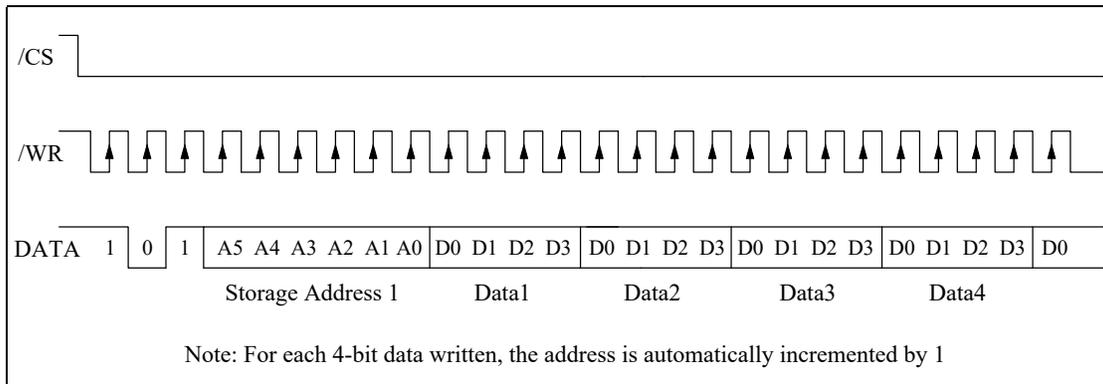


7.2 WRITE Mode

Command Code : 101

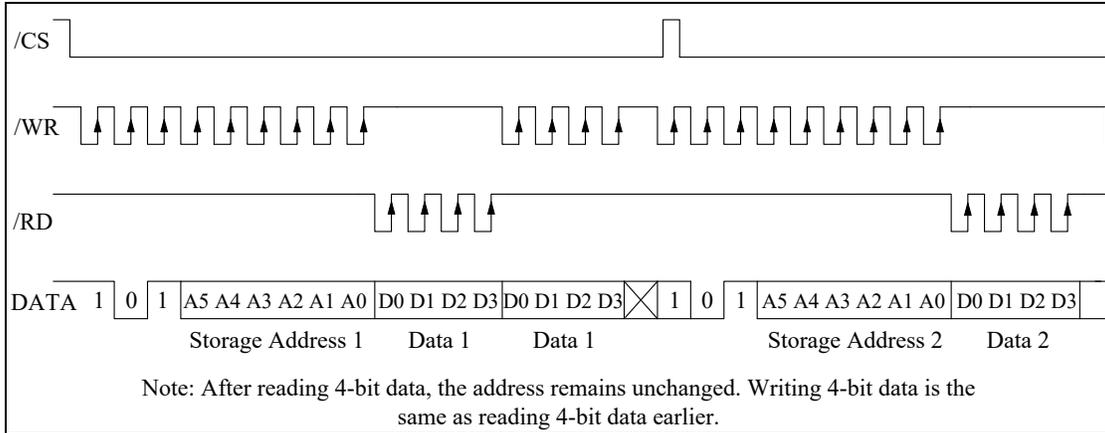


Successive Address Writing

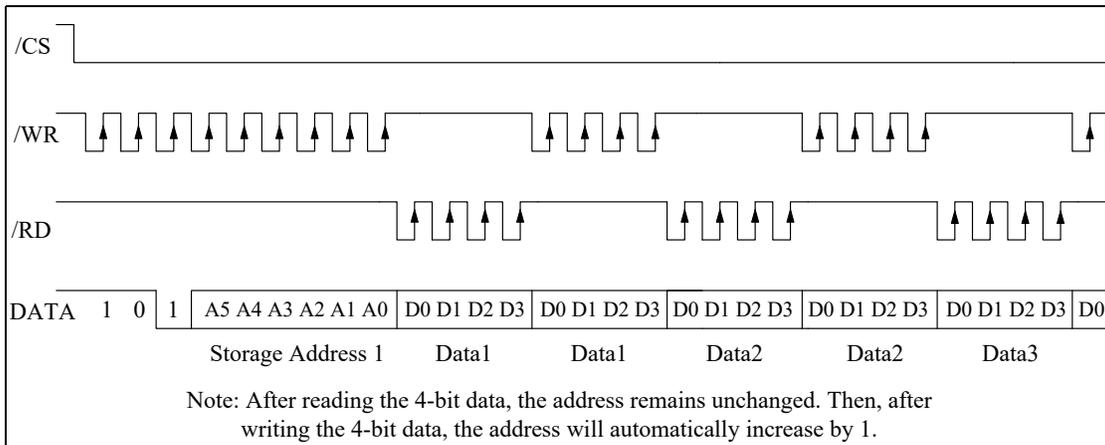


7.3 Read-Modify-Write Mode

Command Code : 101

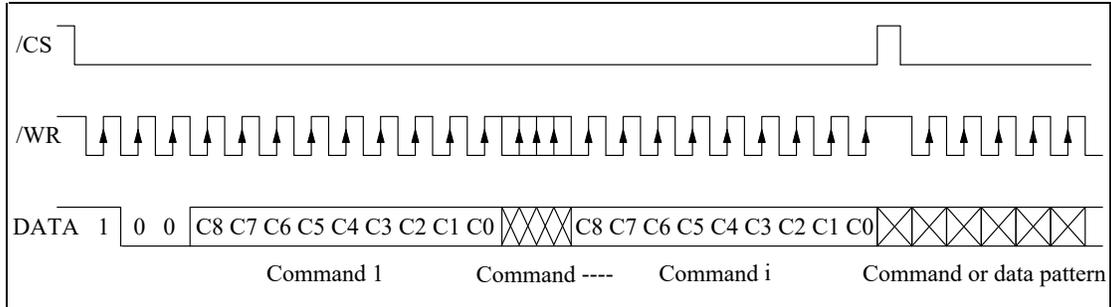


Successive Address Accessing



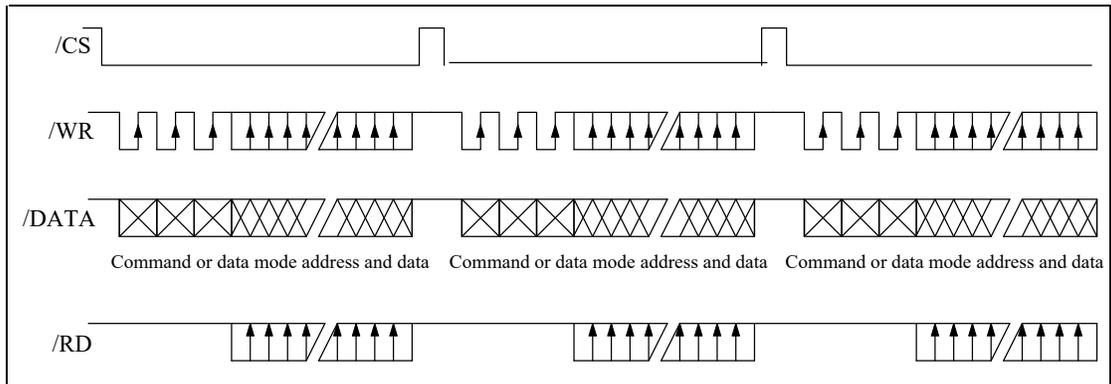
7.4 Command Mode

Command Code : 100



7.5 Data and Command Mode

Data and Command Mode



8 Command Summary

Name	ID	Command Code	D/C	Function	Def.
READ	110	A5A4A3A2A1A0D0D1D2D3	D	Read data from RAM	
WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	Write the data into RAM	
READ-MODIFY-WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	Read and write data from RAM	
SYS DIS	100	0000 - 0000 - X	C	Turn off the system clock and the LCD bias generator	YES
SYS EN	100	0000 - 0001 - X	C	Turn on the system clock	
LCD OFF	100	0000 - 0010 - X	C	Turn off the LCD bias generator	YES
LCD ON	100	0000 - 0011 - X	C	Turn on the LCD bias generator	
TIMERS DIS	100	0000 - 0100 - X	C	The timing reference output is prohibited	
WDT DIS	100	0000 - 0101 - X	C	Prohibit the output of the WDT pause flag	
TIMER EN	100	0000 - 0110 - X	C	Allow timing reference output	
WDT EN	100	0000 - 0111 - X	C	Allow WDT to pause the flag output	
TONE OFF	100	0000 - 1000 - X	C	Turn off the buzzer output	YES
TONE ON	100	0000 - 1001 - X	C	Turn on the buzzer output	
CLR TIMER	100	0000 - 11XX - X	C	Clear the contents in the timing reference generator	
CLR WDT	100	0000 - 111X - X	C	Clear the contents in WDT	
XTAL 32k	100	0001 - 01XX - X	C	System clock, crystal oscillator	
RC 256k	100	0001 - 10XX - X	C	System clock, on-chip RC oscillation	YES
EXT 256k	100	0001 - 11XX - X	C	External clock	
BIAS 1/2	100	0010 - abX0 - X	C	LCD 1/2 Bias setting ab=00: 2 COMS ab=01: 3 COMS ab=10: 4 COMS	
BIAS 1/3	100	0010 - abX1 - X	C	LCD 1/3 Bias setting ab=00: 2 COMS ab=01: 3 COMS ab=10: 4 COMS	
TONE 4k	100	010X - XXXX - X	C	Buzzer frequency output: 4kHz	
TONE 2k	100	011X - XXXX - X	C	Buzzer frequency output: 2kHz	
IRQ DIS	100	100X - 0XXX - X	C	Disable IRQ output	YES
IRQ EN	100	100X - 1XXX - X	C	Enable IRQ output	
F1	100	101X - X000 - X	C	Time base/WDT clock output:1Hz The WDT time-out flag after: 4s	
F2	100	101X - X001 - X	C	Time base/WDT clock output:2Hz The WDT time-out flag after: 2s	
F4	100	101X - X010 - X	C	Time base/WDT clock output:4Hz The WDT time-out flag after: 1s	
F8	100	101X - X011 - X	C	Time base/WDT clock output:8Hz The WDT time-out flag after: 1/2s	
F16	100	101X - X100 - X	C	Time base/WDT clock output:16Hz The WDT time-out flag after: 1/4s	
F32	100	101X - X101 - X	C	Time base/WDT clock output:32Hz The WDT time-out flag after: 1/8s	
F64	100	101X - X110 - X	C	Time base/WDT clock output:64Hz The WDT time-out flag after: 1/16s	
F128	100	101X - X111 - X	C	Time base/WDT clock output:128Hz The WDT time-out flag after: 1/32s	YES
TEST	100	1110 - 0000 - X	C	Test mode	
NORMAL	100	1110 - 0011 - X	C	Normal mode	YES

Note: X: 0 or 1

A5-A0: Display the RAM bit address

D3-D0: 4-bit display data

D/C: Data/Command Mode

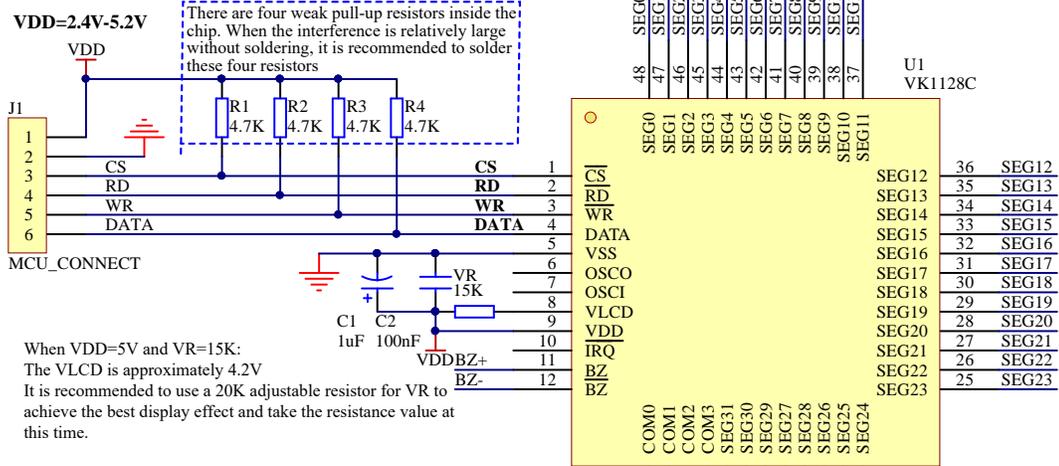
Reset: Default state upon power-on

110,101 and 100 are instruction ids

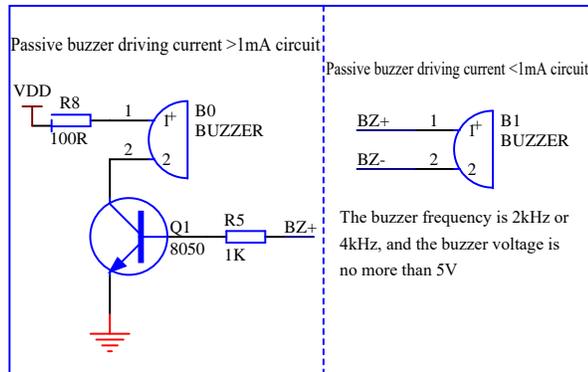
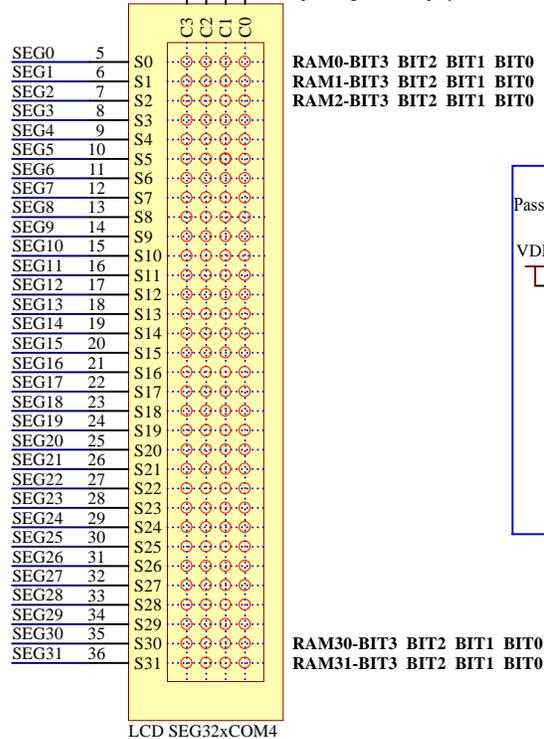
9 Application Circuits

When the LCD only displays, the RD pin can be left floating and not connected
When the surrounding interference is relatively large, a 10R to 1k resistor and a PF-level small capacitor to ground can be connected in series on the communication pin

When the power supply of the single-chip microcomputer (3.3V) and the driver chip (5V) is inconsistent, it is recommended to add a level conversion circuit to the communication pin



It is recommended that the COM pins of the chip and the LCD be connected in a one-to-one sequence. For the convenience of PCB routing, the SEG pins can be shuffled
Note that when writing software, the sequence corresponding to the displayed RAM should also be changed



10 Electrical Characteristics

10.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3~5.5	V
Input voltage	VIN	VSS-0.3~VDD+0.3	V
Storage temperature	TSTG	-50~+125	°C
Operating Temperature	TOTG	-40~+85	°C

10.2 DC Electrical Characteristics

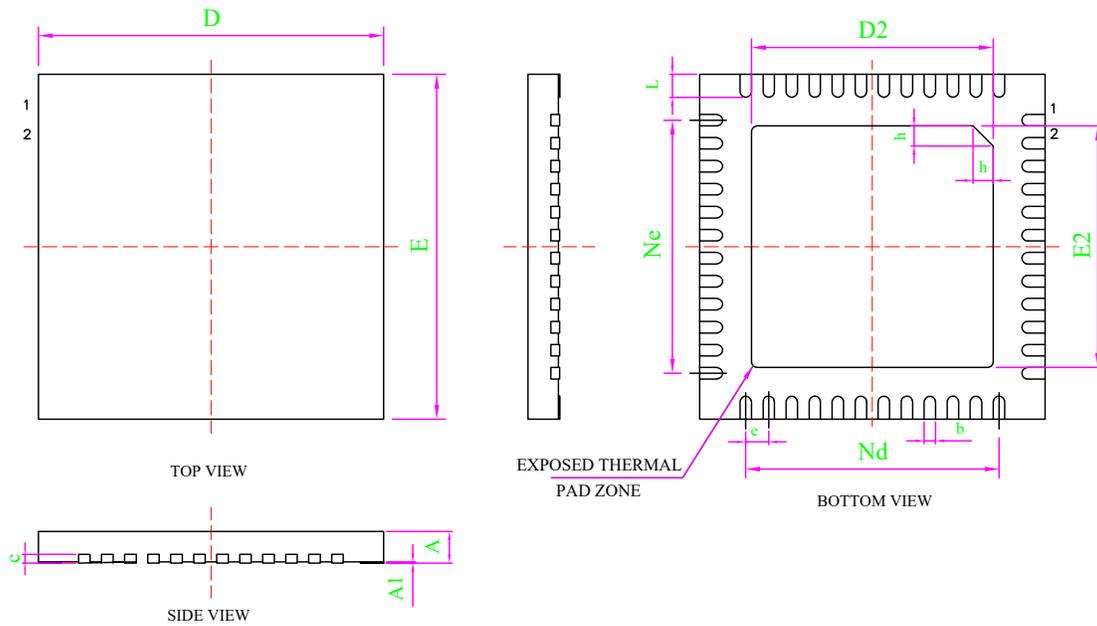
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	2.4	—	5.2	V	—	—
Operating current	IDD1	—	150	300	μA	3V	No load/LCD ON On-chip RC oscillator
		—	300	600		5V	
Operating current	IDD2	—	60	120	μA	3V	No load/LCD ON Crystal oscillator
		—	100	240		5V	
Operating current	IDD3	—	100	200	μA	3V	No load /LCD turns on the external clock
		—	200	240		5V	
Standby Current	ISTB	—	0.1	5	μA	3V	No load, Power down mode
		—	0.3	10		5V	
Low-level Input	VIL	0	—	0.6	V	3V	DATA, /WR, /CS, /RD
		0	—	1.0		5V	
High-level Input	VIH	2.4	—	3.0	V	3V	DATA, /WR, /CS, /RD
		4.0	—	5.0		5V	
DATA, BZ, /BZ, /IRQ	IOL1	0.5	1.2	—	mA	3V	VOL=0.3V
		1.3	2.6	—		5V	VOL=0.5V
DATA, BZ, /BZ	IOH1	-0.4	-0.8	—	mA	3V	VOH=2.7V
		-0.9	-1.8	—		5V	VOH=4.5V
LCD COM Sink Current	IOL2	80	150	—	μA	3V	VOL=0.3V
		150	250	—		5V	VOL=0.5V
LCD COM Source Current	IOH2	-80	-120	—	μA	3V	VOH=2.7V
		-120	-200	—		5V	VOH=4.5V
LCD SEG Sink Current	IOL3	60	120	—	μA	3V	VOL=0.3V
		-120	200	—		5V	VOL=0.5V
LCD SEG Source Current	IOH3	-40	-70	—	μA	3V	VOH=2.7V
		-70	-100	—		5V	VOH=4.5V
Pull-UP Resistor	RUP	40	80	150	kΩ	3V	DATA, /WR, /CS, /RD
		30	60	100		5V	

10.3 AC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
System Clock	f_{SYS1}	—	256	—	kHz	3V	On-chip RC oscillator
		—	256	—		5V	On-chip RC oscillator
System Clock	f_{SYS2}	—	32.768	—	kHz	3V	Crystal oscillator
		—	32.768	—		5V	
System Clock	f_{SYS3}	—	256	—	kHz	3V	External clock
		—	256	—		5V	
LCD Clock	f_{LCD1}	—	$f_{SYS1}/1024$	—	Hz	—	On-chip RC oscillation
		—	$f_{SYS2}/128$	—			Crystal oscillator
		—	$f_{SYS3}/1024$	—			External clock
LCD Common Period	t_{COM}	—	n/f_{LCD}	—	sec	—	N: Number of COM
Serial Data Clock(/WR)	F_{CLK1}	—	—	150	kHz	3V	Duty cycle 50%
		—	—	300		5V	
Serial Data Clock(/RD)	F_{CLK2}	—	—	75	kHz	3V	Duty cycle 50%
		—	—	150		5V	
Serial Interface Reset PW	t_{CS}	—	250	—	ns	—	/CS
/WR, /RD Input Pulse Width	t_{CLK}	3.34	—	—	μs	3V	Write mode
		6.67	—	—			Read mode
		1.67	—	—	μs	5V	Write mode
		3.34	—	—			Read mode
Rise/Fall Time Serial Data Clock Width	t_r, t_f	—	120	—	ns	3V	—
						5V	
Setup Time for DATA to /WR, /RD Clock Width	t_{su}	—	120	—	ns	3V	—
						5V	
Hold Time for DATA to/ WR, /RD Clock Width	t_h	—	120	—	ns	3V	—
						5V	
Setup Time for /CS to /WR, /RD Clock Width	t_{su1}	—	100	—	ns	3V	—
						5V	
Hold Time for /CS to/ WR, /RD Clock Width	t_{h1}	—	100	—	ns	3V	—
						5V	

11 Package Information

11.1 QFN48L (5.0mm × 5.0mm PP=0.35mm)



MILLIMETER			
SYMBOL	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.13	0.18	0.23
B1	0.12REF		
c	0.10	0.15	0.20
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
e	0.35BSC		
Ne	3.85BSC		
Nd	3.85BSC		
E	4.90	5.00	5.10
E2	3.60	3.70	3.80
L	0.30	0.35	0.40
L1	0.13	0.18	0.23
h	0.25	0.30	0.35
载体尺寸 (mil)	154×154		

12 Disclaimer

Warranty and liability — The information provided in this document is believed to be accurate and reliable. However, Shenzhen Vinka Microelectronics Co., Ltd. (hereinafter “the Company”) makes no warranties, express or implied, as to the completeness or suitability of this information for any specific purpose.

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Right to change — The Company reserves the right to modify any information contained herein without prior notice. The latest version of this document is available at:

<https://www.szvinka.com/>

Applicability — This product is not designed or intended for use in life-critical, medical, or safety systems where failure could result in injury or death. The customer shall assume full responsibility for any such use.

Application — All product application descriptions provided herein are intended for illustrative purposes only. The Company makes no representations or warranties, express or implied, regarding the suitability of any specific application without further testing or modification.

The customer is solely responsible for determining whether the Company’s products are appropriate for their intended applications or end customers.

The customer shall ensure proper design practices, implementation safeguards, and operational validation to minimize risks associated with product use.

The Company shall not be held liable for any defects, losses, costs, or damages arising from weaknesses or failures in the customer’s own products or applications, or from the integration or use of third-party products.

Furthermore, the customer shall conduct all necessary testing and validation for any third-party deployment of the Company’s products to avoid potential misuse or associated damages. The Company assumes no liability in this regard.

Commercial terms of sale — Unless otherwise agreed in writing, sales of this product are subject to the Company’s standard terms and conditions of sale. The Company expressly rejects the applicability of the customer’s general terms and conditions.

Export control — This product may be subject to applicable export control regulations. The customer is solely responsible for compliance with such regulations, including obtaining any necessary export licenses.

13 Revision History

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Initial release	YES
2	1.1	2018-10-11	Add reference circuit	YES
3	1.2	2019-03-21	Alignment correction	YES
4	1.3	2025-05-12	Change Description	YES

[1] Please refer to the latest version of this document before starting or finalizing any design.

[2] Since the release of this document, the status or availability of this product may have changed. For the most up-to-date information, please visit:

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