永嘉微电
Vinka Microelectronics

# VK1088B Datasheet

22×4 LCD DRIVER

Rev.1.3

# 1 General Description

The VK1088B is a dot-matrix memory-mapped LCD driver that supports LCD screens with a maximum of 88 dots (22SEG×4COM), as well as 2COM and 3COM LCD screens. The single-chip microcomputer can be configured with display parameters and send display data through three communication lines, and can also enter power-saving mode through instructions.

# 2 Key Features

- Operating voltage：2.4-5.2V
- Integrated RC oscillator (default)
- Selectable LCD bias:1/2 or 1/3
- Selectable LCD duty:1/2 or 1/3 or 1/4
- Built-in 22×4 bit display RAM
- Power-down mode via software command(LCD OFF, SYS DIS)
- 3 wire serial communication interface
- Software-configurable of LCD parameters
- Dual command formats for configuration and access
- Auto-increment addressing for sequential write
- VLCD adjustable via external pin (≤ VDD)
- Available Packages:
  QFN32L (4.0mm × 4.0mm PP=0.4mm)

# 3 Application field

- Electricity meter/gas meter
- Massage device/beauty device
- Medical instruments
- Vehicle-mounted equipment
- Air conditioner/heater

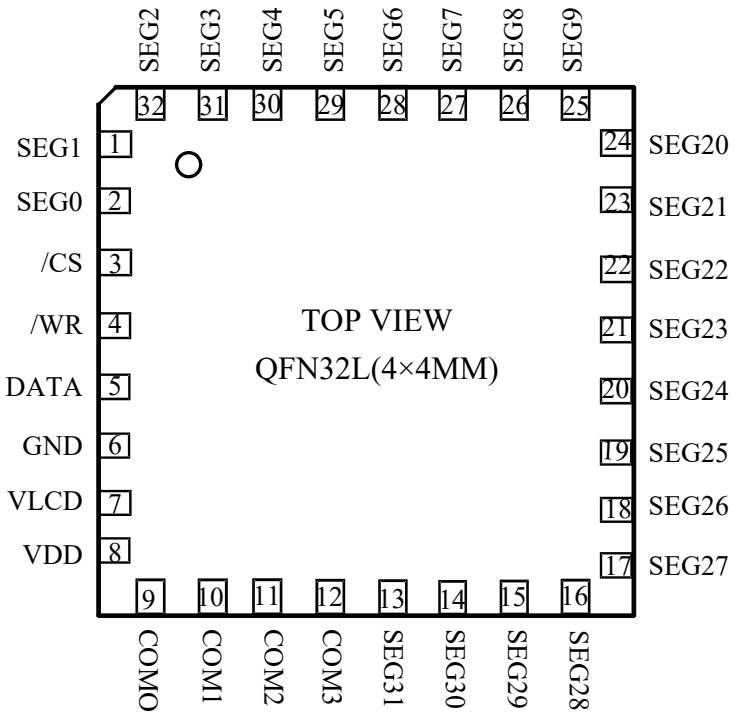
## 4 Product Selection

| Part No. | SEG × COM | BIAS | DUTY | Packaging |
|---|---|---|---|---|
| VK1024B | 6×4,6×3,6×2 | 1/2,1/3 | 1/2,1/3,1/4 | SOP16 |
| VK1056B | 14×4,14×3,14×2 | 1/2,1/3 | 1/2,1/3,1/4 | SOP24 |
| VK1056C | 14×4,14×3,14×2 | 1/2,1/3 | 1/2,1/3,1/4 | SSOP24 |
| VK1056Q | 14×4,14×3,14×2 | 1/2,1/3 | 1/2,1/3,1/4 | QFN24L |
| VK1072B | 18×4,18×3,18×2 | 1/2,1/3 | 1/2,1/3,1/4 | SOP28 |
| VK1072C | 18×4,18×3,18×2 | 1/2,1/3 | 1/2,1/3,1/4 | SOP28 |
| VK1072D | 18×4,18×3,18×2 | 1/2,1/3 | 1/2,1/3,1/4 | SSOP28 |
| VK1088B | 22×4,22×3,22×2 | 1/2,1/3 | 1/2,1/3,1/4 | QFN32L |
| VK1128C | 32×4,32×3,32×2 | 1/2,1/3 | 1/2,1/3,1/4 | QFN48L |

## 5 Ordering Information

| Part No. | Packaging | Tube Qty | Tray Qty | Box Qty | Total Qty | Notes |
|---|---|---|---|---|---|---|
| VK1024B | SOP16 | 50/tube | | 10000/box | 100000 PCS | |
| VK1056B | SOP24 | 30/tube | | 2400/box | 24000 PCS | |
| VK1056C | SSOP24 | 60/tube | | 6000/box | 60000 PCS | |
| VK1056Q | QFN24L | | 490/tray | 4900/box | 29400 PCS | |
| VK1072B | SOP28 | 26/tube | | 2080/box | 20800 PCS | |
| VK1072C | SOP28 | 26/tube | | 2080/box | 20800 PCS | |
| VK1072D | SSOP28 | 50/tube | | 5000/box | 50000 PCS | |
| VK1088B | QFN32L | | | 3000/box | 24000 PCS | |
| VK1128C | QFN48L | | 3000/tray | | 24000 PCS | |

## 6 Package Pinout Information(QFN32L)



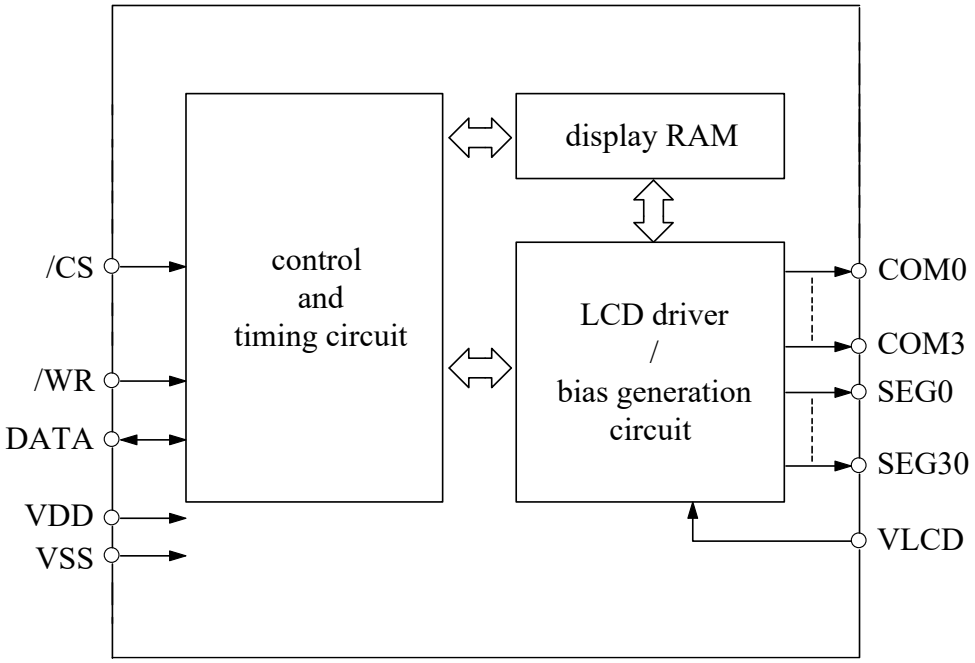

For more information: Page 15

## 6.1 VK1088B/QFN32 Pin Description

| No. | Name | I/O | Function |
|---|---|---|---|
| 1-2<br>13-32 | SEG1-SEG0<br>SEG31-SEG20<br>SEG9-SEG2 | O | LCD SEG drive outputs |
| 3 | /CS | I | Chip select signal with pull-up resistor ,active low. |
| 4 | /WR | I | Serial write signal with pull-up resistor,<br>data latched on the rising edge of the /WR signal. |
| 5 | DATA | I/O | Serial data signal with pull-up resistor,<br>input/output depending on access mode. |
| 6 | GND | GND | Negative power supply |
| 7 | VLCD | I | LCD driving voltage input,must be ≤VDD |
| 8 | VDD | VDD | Positive power supply |
| 9-12 | COM0-COM3 | O | LCD COM drive outputs |

# 7 Functional Description

## 7.1 Block Diagram



## 7.2 Display RAM

The VK1088B integrates 22 × 4-bit RAM for LCD display. directly mapped to SEGx/COMx segments. Data is latched and updated on the LCD according to scan timing set by the system configuration. The display RAM can be accessed using three commands: WRITE, and MODIFY-WRITE. Each RAM address corresponds to a specific combination of SEG and COM lines.

The following is a mapping from the RAM to the LCD pattern:

| | COM3 | COM2 | COM1 | COM0 | | |
|---|---|---|---|---|---|---|
| SEG0 | | | | | 0 | Address 6 bit （A5----A0） |
| SEG1 | | | | | 1 | |
| SEG2 | | | | | 2 | |
| SEG3 | | | | | 3 | |
| ⋮ | | | | | ⋮ | |
| SEG30 | | | | | 30 | |
| | D3 | D2 | D1 | D0 | Data\Addr | |

Note：

1. When the SEG is not continuous, the display RAM address is also not continuous.
2. When writing multiple data continuously，the display data address is automatically incremented by 1.When SEG is not continuous，write 0 to the empty display RAM addressdata，until the address automatically adds 1 to the display RAM address where the next SEG is located.

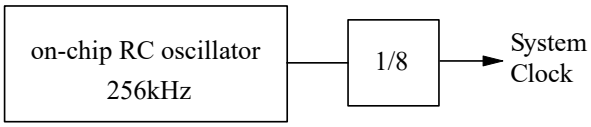
## 7.3 System Oscillator

The VK1088B system clock is used to generate the time base clock frequency, LCD driving clock. The source of the clock from on-chip RC oscillator (256kHz).

After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off, Once the system clock stops，then LCD display become darker and disappears，and the time base lose its function as well.

The LCD OFF command is used to turn the LCD bias generator off. After the LCD OFF command, using the SYS DIS command reduces power consumption, serving as a standby command.

System Oscillator Configuration：




## 7.4 LCD Driver

The VK1088B is a 88-segment LCD driver (22 SEG×4 COM). It supports software-configurable bias settings of 1/2 or 1/3, and COM configurations of 2COM or 3COM or 4COM.

## 7.5 Communication Interfacing

The VK1088B communicates with the host via a 3-wire serial interface.
When used solely for display output, only 3 lines are required (/CS, /WR, and DATA)

- /CS: Chip select input. It enables the serial interface when low and terminates communication when high.
- /WR: Write clock input. On the rising edge, data and commands from DATA are latched into the device.
- DATA: Bidirectional serial data line used to transfer both command and display data.

## 7.6 Command Format

The VK1088B is configured via software commands that support two primary modes: command mode and data mode.

- Command mode is used to configure system-level parameters. It is identified by a command mode ID of 100.
- Data mode supports two types of memory operations: WRITE, and MODIFY-WRITE.

These commands allow the host controller to configure LCD behavior and access display RAM contents.

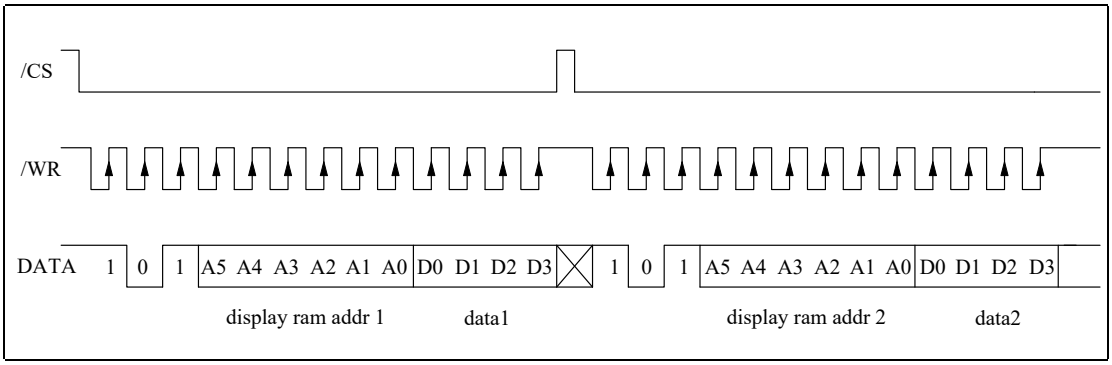
The following are the data mode IDs and the command mode ID:

| Operation | MODE | ID |
|---|---|---|
| WRITE | DATA | 101 |
| COMMAND | COMMAND | 100 |

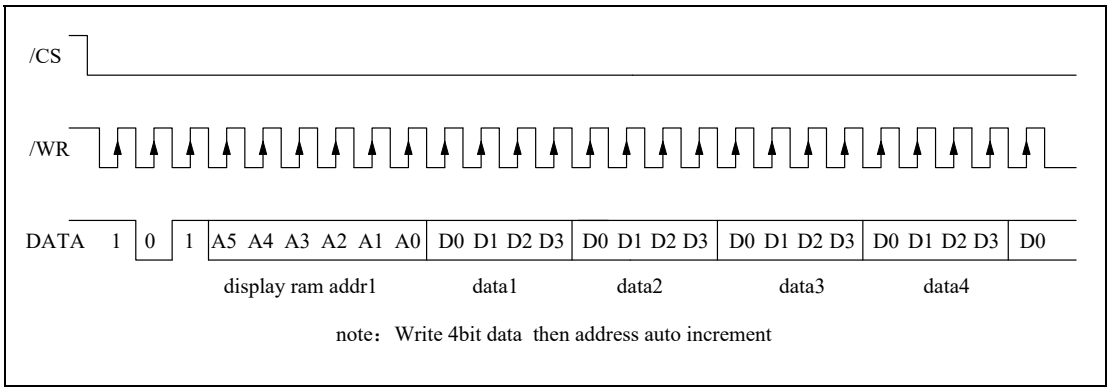
# 8 CMD/Data Timing Diagrams

## 8.1 WRITE Mode

Command Code : 101

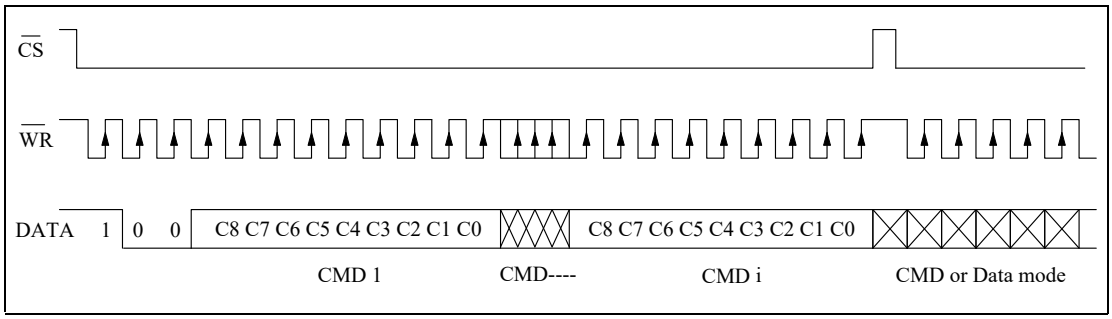



Successive Address Writing



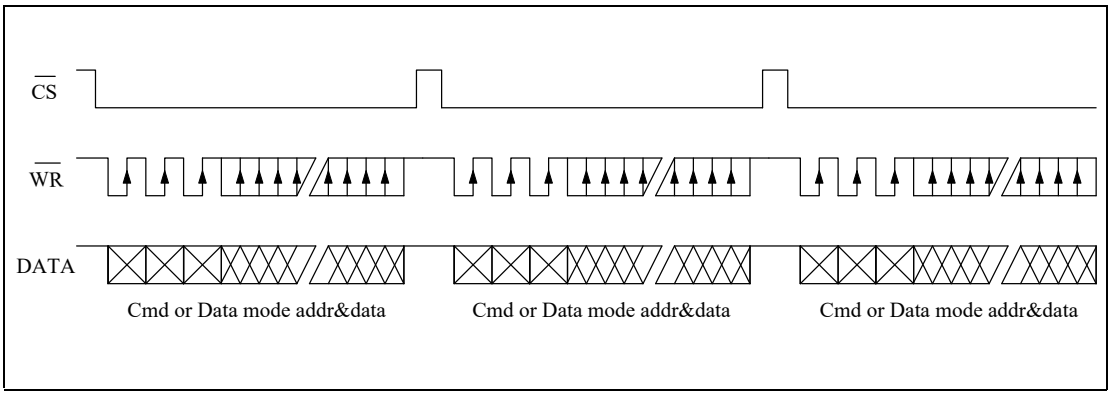
## 8.2 Command Mode

Command Code : 100




## 8.3 Data and Command Mode

Data and Command Mode



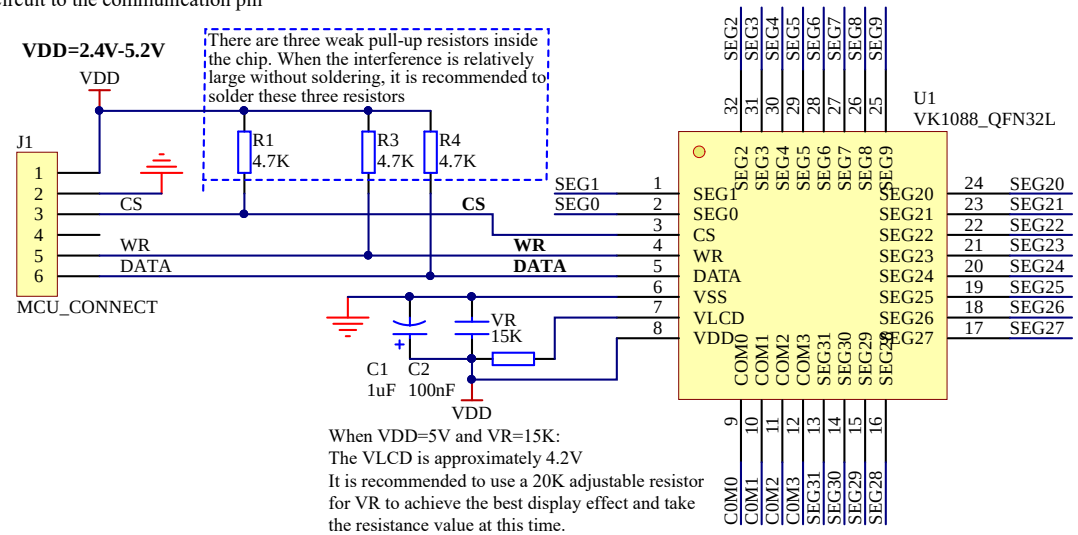
# 9 Command Summary

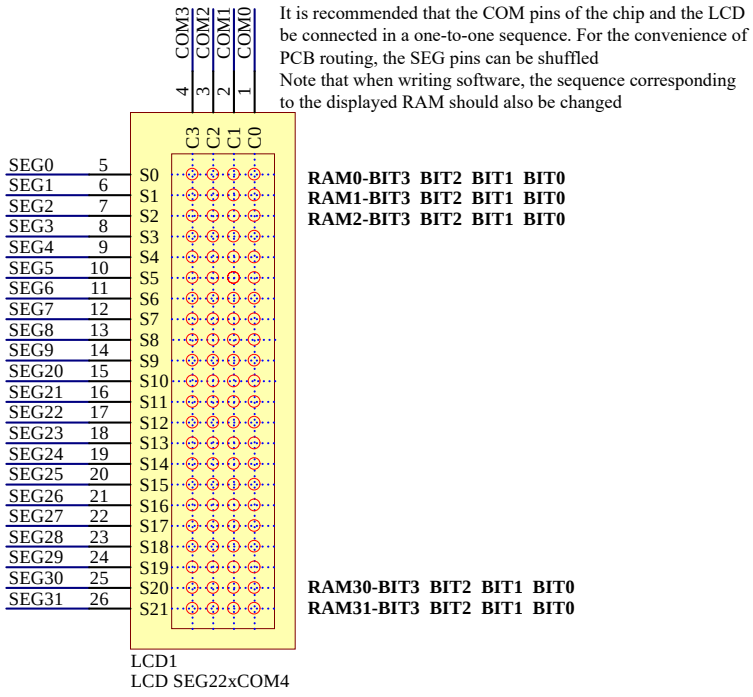
| Name | ID | Command Code | D/C | Function | Def. |
|---|---|---|---|---|---|
| WRITE | 101 | A5A4A3A2A1A0D0D1D2D3 | D | Write data to the RAM | |
| SYS DIS | 100 | 0000-0000-X | C | Turn off system oscillator | YES |
| SYS EN | 100 | 0000-0001-X | C | Turn on the system clock | |
| LCD OFF | 100 | 0000-0010-X | C | Turn off LCD bias generator | YES |
| LCD ON | 100 | 0000-0011-X | C | Turn on LCD bias generator | |
| RC 256k | 100 | 0001-10XX-X | C | on-chip RC oscillator | YES |
| BIAS 1/2 | 100 | 0010-abX0-X | C | LCD 1/2 bias option<br>ab=00：2 COMS<br>ab=01：3 COMS<br>ab=10：4 COMS | |
| BIAS 1/3 | 100 | 0010-abX1-X | C | LCD 1/3 bias option<br>ab=00：2 COMS<br>ab=01：3 COMS<br>ab=10：4 COMS | |
| TEST | 100 | 1110-0000-X | C | Test mode | |
| NORMAL | 100 | 1110-0011-X | C | Normal mode | YES |

Note: X：0 or 1
A5-A0：Display RAM addresses
D3-D0：4bit Display RAM data
D/C： Data/Command mode
Def.：Power on reset default
101 and 100 is command ID

# 10 Application Circuits

When the surrounding interference is relatively large, a 10R to 1k resistor and a PF-level small capacitor to ground can be connected in series on the communication pin
When the power supply of the single-chip microcomputer (3.3V) and the driver chip (5V) is inconsistent, it is recommended to add a level conversion circuit to the communication pin




It is recommended that the COM pins of the chip and the LCD be connected in a one-to-one sequence. For the convenience of PCB routing, the SEG pins can be shuffled
Note that when writing software, the sequence corresponding to the displayed RAM should also be changed

**RAM0-BIT3 BIT2 BIT1 BIT0**
**RAM1-BIT3 BIT2 BIT1 BIT0**
**RAM2-BIT3 BIT2 BIT1 BIT0**

**RAM30-BIT3 BIT2 BIT1 BIT0**
**RAM31-BIT3 BIT2 BIT1 BIT0**

# 11 Electrical Characteristics

## 11.1 Absolute Maximum Ratings

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | VDD | -0.3～5.5 | V |
| Input Voltage | VIN | $V_{SS}$-0.3～$V_{DD}$+0.3 | V |
| Storage Temperature | $T_{STG}$ | -50～+125 | ℃ |
| Operating Temperature | $T_{OTG}$ | -40～+85 | ℃ |

## 11.2 DC Electrical Characteristics

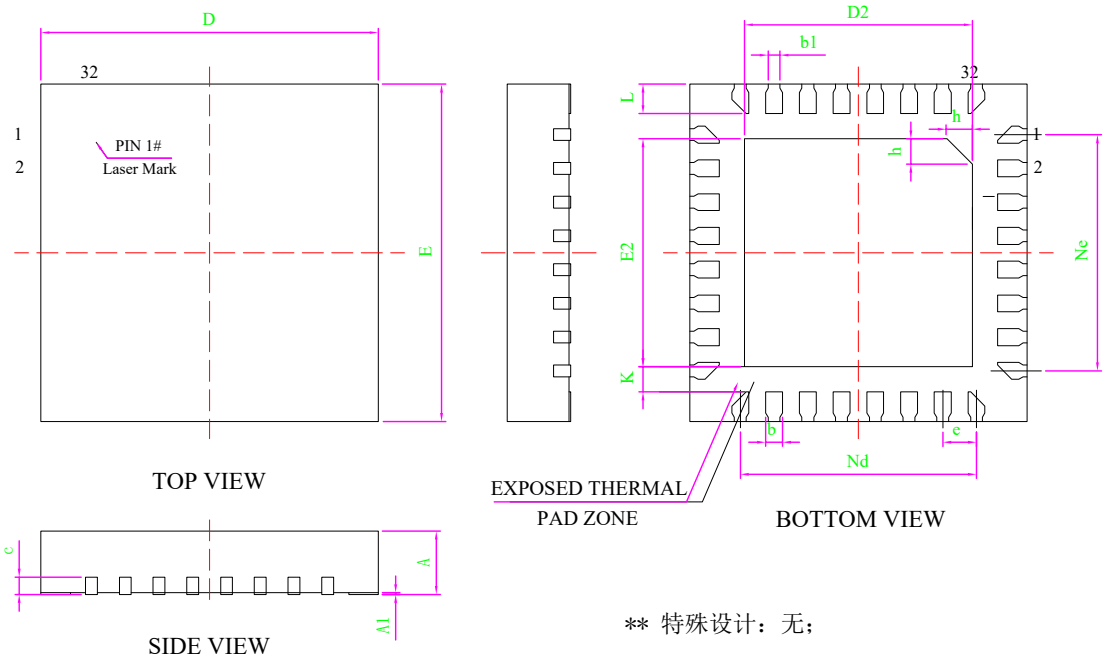
| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | |
|---|---|---|---|---|---|---|---|
| | | | | | | VDD | Conditions |
| Operating voltage | VDD | 2.4 | - | 5.2 | V | - | - |
| Operating current | $I_{DD1}$ | - | 150 | 300 | μA | 3V | No load/LCD ON<br>On-chip RC oscillator |
| | | - | 300 | 600 | | 5V | |
| Standby Current | $I_{STB}$ | - | 0.1 | 5 | μA | 3V | No load,<br>Power down mode |
| | | - | 0.3 | 10 | | 5V | |
| Low-level Input | $V_{IL}$ | 0 | - | 0.6 | V | 3V | DATA, /WR, /CS |
| | | 0 | - | 1.0 | | 5V | |
| High-level Input | $V_{IH}$ | 2.4 | - | 3.0 | V | 3V | DATA, /WR, /CS |
| | | 4.0 | - | 5.0 | | 5V | |
| DATA | $I_{OL1}$ | 0.5 | 1.2 | - | mA | 3V | $V_{OL}$=0.3V |
| | | 1.3 | 2.6 | - | | 5V | $V_{OL}$=0.5V |
| DATA | $I_{OH1}$ | -0.4 | -0.8 | - | mA | 3V | $V_{OH}$=2.7V |
| | | -0.9 | -1.8 | - | | 5V | $V_{OH}$=4.5V |
| LCD COM Sink Current | $I_{OL2}$ | 80 | 150 | - | μA | 3V | $V_{OL}$=0.3V |
| | | 150 | 250 | - | | 5V | $V_{OL}$=0.5V |
| LCD COM Source Current | $I_{OH2}$ | -80 | -120 | - | μA | 3V | $V_{OH}$=2.7V |
| | | -120 | -200 | - | | 5V | $V_{OH}$=4.5V |
| LCD SEG Sink Current | $I_{OL3}$ | 60 | 120 | - | μA | 3V | $V_{OL}$=0.3V |
| | | 120 | 200 | - | | 5V | $V_{OL}$=0.5V |
| LCD SEG Source Current | $I_{OH3}$ | -40 | -70 | - | μA | 3V | $V_{OH}$=2.7V |
| | | -70 | -100 | - | | 5V | $V_{OH}$=4.5V |
| Pull-UP Resistor RUP | $R_{UP}$ | 40 | 80 | 150 | kΩ | 3V | DATA, /WR, /CS |
| | | 30 | 60 | 100 | | 5V | |

## 11.3 AC Electrical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | |
|---|---|---|---|---|---|---|---|
| | | | | | | VDD | Conditions |
| System Clock | $f_{SYS1}$ | - | 256 | - | kHz | 3V | On-chip RC oscillator |
| | | - | 256 | - | | 5V | On-chip RC oscillator |
| LCD Clock | $f_{LCD1}$ | - | $f_{SYS1}$/1024 | - | | | On-chip RC oscillator |
| LCD Common Period | $t_{COM}$ | - | n/ $f_{LCD}$ | - | sec | - | N：Number of COM |
| Serial Data Clock(/WR) | $F_{CLK1}$ | - | - | 150 | kHz | 3V | Duty cycle 50% |
| | | - | - | 300 | | 5V | |
| Serial Interface Reset PW | $t_{CS}$ | - | 250 | - | ns | - | /CS |
| /WR Input Pulse Width | $t_{CLK}$ | 3.34 | - | - | μs | 3V | Write mode |
| | | 1.67 | - | - | μs | 5V | Write mode |
| Rise/Fall Time<br>Serial Data Clock Width | $t_r$，$t_f$ | - | 120 | - | ns | 3V | - |
| | | | | | | 5V | |
| Setup Time for DATA to /WR Clock Width | $t_{su}$ | - | 120 | - | ns | 3V | - |
| | | | | | | 5V | |
| Hold Time for DATA to /WR Clock Width | $t_h$ | - | 120 | - | ns | 3V | - |
| | | | | | | 5V | |
| Setup Time for /CS to /WR Clock Width | $t_{su1}$ | - | 100 | - | ns | 3V | - |
| | | | | | | 5V | |
| Hold Time for /CS to /WR Clock Width | $t_{h1}$ | - | 100 | - | ns | 3V | - |
| | | | | | | 5V | |

# 12 Package Information

## 12.1 QFN32L (4.0mm × 4.0mm PP=0.4mm)




** 特殊设计：无；

| Dimensions | | | |
|---|---|---|---|
| SYMBOL | MIN | NOMINAL | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 |
| b | 0.15 | 0.20 | 0.25 |
| B1 | 0.14REF | | |
| c | 0.203REF | | |
| D | 3.90 | 4.00 | 4.10 |
| D2 | 2.60 | 2.70 | 2.80 |
| e | 0.40BSC | | |
| Nd | 2.80BSC | | |
| E | 3.90 | 4.00 | 4.10 |
| E2 | 2.60 | 2.7 | 2.80 |
| Ne | 2.80BSC | | |
| L | 0.30 | 0.35 | 0.40 |
| h | 0.25 | 0.30 | 0.35 |
| K | 0.30REF | | |

# 13 Disclaimer

**Warranty and liability** —— The information provided in this document is believed to be accurate and reliable. However, Shenzhen Vinka Microelectronics Co., Ltd. (hereinafter "the Company") makes no warranties, express or implied, as to the completeness or suitability of this information for any specific purpose.

In no event shall the Company be liable for any indirect, incidental, or consequential damages, including but not limited to loss of profits, equipment damage, or system failure, arising out of the use of this product or documentation, regardless of the legal theory under which such liability is asserted.

**Right to change** —— The Company reserves the right to modify any information contained herein without prior notice. The latest version of this document is available at: https://www.szvinka.com/

**Applicability** —— This product is not designed or intended for use in life-critical, medical, or safety systems where failure could result in injury or death. The customer shall assume full responsibility for any such use.

**Application** —— All product application descriptions provided herein are intended for illustrative purposes only.
The Company makes no representations or warranties, express or implied, regarding the suitability of any specific application without further testing or modification.

The customer is solely responsible for determining whether the Company's products are appropriate for their intended applications or end customers.

The customer shall ensure proper design practices, implementation safeguards, and operational validation to minimize risks associated with product use.

The Company shall not be held liable for any defects, losses, costs, or damages arising from weaknesses or failures in the customer's own products or applications, or from the integration or use of third-party products.

Furthermore, the customer shall conduct all necessary testing and validation for any third-party deployment of the Company's products to avoid potential misuse or associated damages. The Company assumes no liability in this regard.

**Commercial terms of sale** —— Unless otherwise agreed in writing, sales of this product are subject to the Company's standard terms and conditions of sale. The Company expressly rejects the applicability of the customer's general terms and conditions.

**Export control**—— This product may be subject to applicable export control regulations. The customer is solely responsible for compliance with such regulations, including obtaining any necessary export licenses.

# 14 Revision History

| No. | Version | Date | Modify the content | Check |
|---|---|---|---|---|
| 1 | 1.0 | 2018-08-10 | Initial release | YES |
| 2 | 1.1 | 2018-10-11 | Add reference circuit | YES |
| 3 | 1.2 | 2019-03-21 | Alignment correction | YES |
| 4 | 1.3 | 2025-05-06 | Change Description | YES |

[1] Please refer to the latest version of this document before starting or finalizing any design.

[2] Since the release of this document, the status or availability of this product may have changed. For the most up-to-date information, please visit: https://www.szvinka.com/