



XMB294D 'F cvcuj ggv

'3: 6'NEF 'F T>

Tgx&G

ƆvgngewcnRtqr gtvŀ "Ucvo gpv<

Uj gpl j gp"Xkpnœ"O letqgrgestqpleu"Eq0"Nf0*j gtgkpchgt"tghgttgf "v"cu"öy g"Eqo r cp{ö+"qy pu" rgi cmŀ "tgi kvgtgf "Ɔvgngewcn'r tqr gtvŀ "tki j w"kp"dqy "f qo guke"cpf "Ɔvgtpcvkqpcn'lwtkuf levkpu0' Cp{"wpcwj qtkŀ gf "wug"qh'vj g"Eqo r cp{œ'r tqf weu"qt"r cvgpvgf "vgej pqrqi kgu'd{"Ɔpf kxf wcu"qt" qti cpkŀ cvkpu'ku'wtkewŀ 'r tqj kdkgf 0

Vj g"Eqo r cp{"tugtxgu"vj g"tki j v"vq"vcng"rgi cn'cevkq"ci ckpu'cp{"Ɔphtkpi go gpv"cpf "v"uggnlhwni' eqo r gpuvkq'ht'f co ci gu"qt'vprcy hwni ckpu0

Vj g"Eqo r cp{œ'pco g"cpf "vtf go ctmu"ctg"rgi cmŀ "r tqvgevgf"cpf "o c{"pqv'dg"wugf"qt"ko kcvgf" y kj qw'gZR rlek'y tkwgp"r gto kuukp0'P q"ko r rikf"qt"gzr tguu'rkpgpug"uj cm'dg"i tcpvgf"wpf gt"cp{" ektewo ucpegu0

3. 工作电压

Vj g"XMB294D"ku'c'f qv'o cvtz'o go qt{/o cr r gf "NEF "f tkxgt "y cv' uwr r qt'u"NEF "uetggpu'y kj "c"o czko wo "qh'94"fq'u"3: UGI 6EQO + " cu'y gni'cu"4EQO "cpf "5EQO "NEF "uetggpu"Vj g'ukpi ng/ej kr " o letqeqo r wgt'ecp'dg'eqphki wtgf "y kj "f kur rc{"r ctco gvgtu'cpf "ugpf" f kur rc{"f cvc"y'j tqwi j "y tgg"eqo o wplecvkqp'ikpgu.cpf "ecp'cuq"gpvgt" r qy gt/ucxkpi "o qf g"y'j tqwi j "kputwvklpu0

4. 主要特性

- 工作电压: 2.4-5.2V
- Integrated RC oscillator (default)
- Selectable LCD bias: 1/2 or 1/3
- Selectable LCD duty: 1/2 or 1/3 or 1/4
- Built-in 32×4 bit display RAM
- Power-down mode via software command(LCD OFF, SYS DIS)
- 3 wire serial communication interface
- Software-configurable of LCD parameters
- Dual command formats for configuration and access
- Auto-increment addressing for sequential write
- VLCD adjustable via external pin ($\leq VDD$)
- Available Packages:
SSOP28(150mil) (9.9mm × 3.9mm PP=0.635mm)

5. 引脚功能

- Grgv'lekyl "o gvgt li cu'o gvgt
- O cuuci g'f gxleg'ldgcwyl "f gxleg
- O gf lecn'kputwo gpw
- Xgj kerg/o qwpvgf "gs wkr o gpv
- Ckt "eqpf kklqpgt lj gcvgt

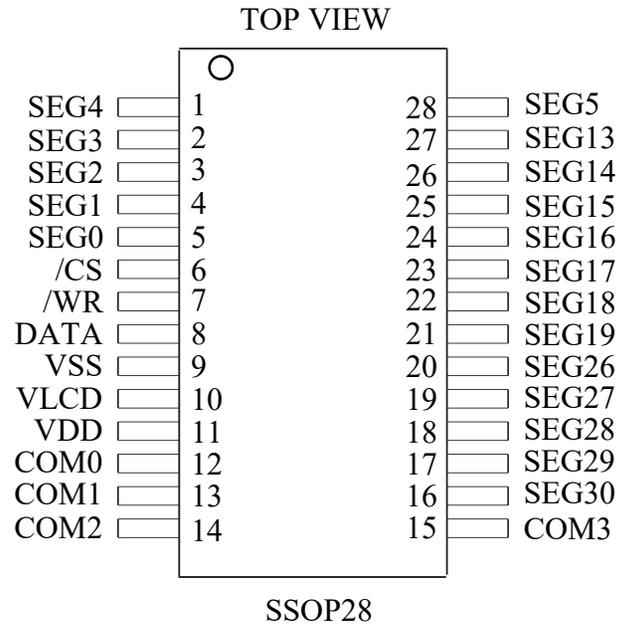
4 Product Selection

Part No.	SEG × COM	BIAS	DUTY	Packaging
VK1024B	6×4,6×3,6×2	1/2,1/3	1/2,1/3,1/4	SOP16
VK1056B	14×4,14×3,14×2	1/2,1/3	1/2,1/3,1/4	SOP24
VK1056C	14×4,14×3,14×2	1/2,1/3	1/2,1/3,1/4	SSOP24
VK1056Q	14×4,14×3,14×2	1/2,1/3	1/2,1/3,1/4	QFN24L
VK1072B	18×4,18×3,18×2	1/2,1/3	1/2,1/3,1/4	SOP28
VK1072C	18×4,18×3,18×2	1/2,1/3	1/2,1/3,1/4	SOP28
VK1072D	18×4,18×3,18×2	1/2,1/3	1/2,1/3,1/4	SSOP28
VK1088B	22×4,22×3,22×2	1/2,1/3	1/2,1/3,1/4	QFN32L
VK1128C	32×4,32×3,32×2	1/2,1/3	1/2,1/3,1/4	QFN48L

5 Ordering Information

Part No.	Packaging	Tube Qty	Tray Qty	Box Qty	Total Qty	Notes
VK1024B	SOP16	50/tube		10000/box	100000 PCS	
VK1056B	SOP24	30/tube		2400/box	24000 PCS	
VK1056C	SSOP24	60/tube		6000/box	60000 PCS	
VK1056Q	QFN24L		490/tray	4900/box	29400 PCS	
VK1072B	SOP28	26/tube		2080/box	20800 PCS	
VK1072C	SOP28	26/tube		2080/box	20800 PCS	
VK1072D	SSOP28	50/tube		5000/box	50000 PCS	
VK1088B	QFN32L			3000/box	24000 PCS	
VK1128C	QFN48L		3000/tray		24000 PCS	

6 Package Pinout Information(SSOP28)



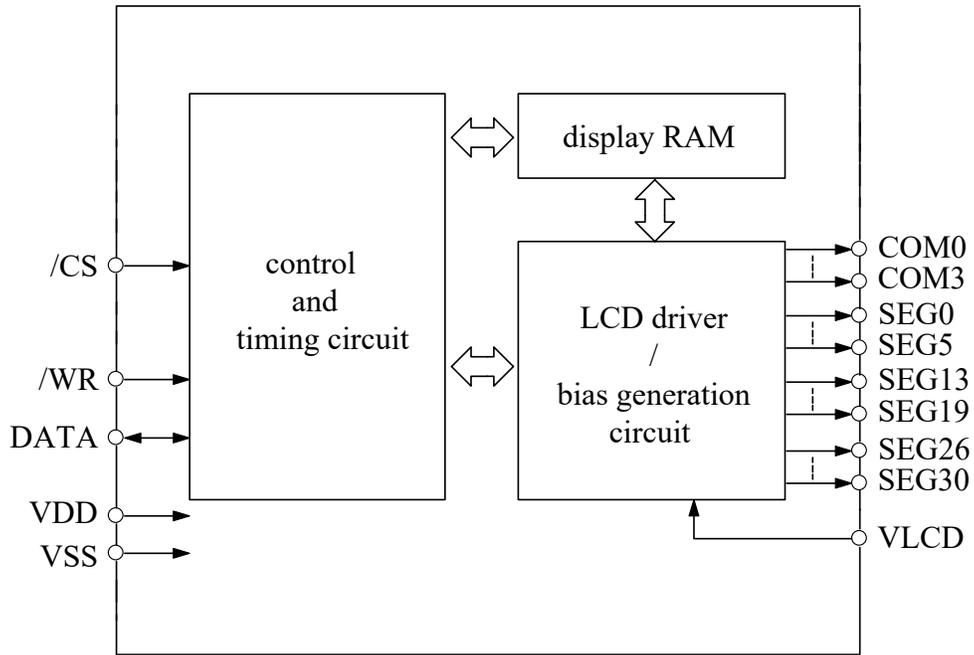
For more information: [Page 15](#)

6.1 VK1072D/SSOP28 Pin Description

No.	Name	I/O	Function
1-5 16-28	SEG4-SEG0 SEG30-SEG13 SEG5	O	LCD SEG drive outputs
6	CS	I	Chip select signal with pull-up resistor ,active low.
7	WR	I	Serial write signal with pull-up resistor, data latched on the rising edge of the /WR signal.
8	DATA	I/O	Serial data signal with pull-up resistor, input/output depending on access mode.
9	VSS	VSS	Negative power supply
10	VLCD	I	LCD driving voltage input,must be \leq VDD
11	VDD	VDD	Positive power supply
12-15	COM0-COM3	O	LCD COM drive outputs

7 Functional Description

7.1 Block Diagram



7.2 Display RAM

The VK1072D integrates 32×4 -bit RAM for LCD display, directly mapped to SEGx/COMx segments. Data is latched and updated on the LCD according to scan timing set by the system configuration. The display RAM can be accessed using three commands: WRITE, and MODIFY-WRITE. Each RAM address corresponds to a specific combination of SEG and COM lines.

The following is a mapping from the RAM to the LCD pattern:

	COM3	COM2	COM1	COM0		
SEG 0					0	Address 6 bit (A5---A0)
SEG 1					1	
⋮					⋮	
SEG5					5	
---	---	---	---	---	---	
SEG13					13	
⋮	⋮	⋮	⋮	⋮	⋮	
SEG19					19	
---	---	---	---	---	---	
SEG26					26	
⋮	⋮	⋮	⋮	⋮	⋮	
SEG30					30	
---	---	---	---	---	31	
	D3	D2	D1	D0	Data\Addr	

Note:

1. When the SEG is not continuous, the display RAM address is also not continuous.
2. When writing multiple data continuously, the display data address is automatically incremented by 1. When SEG is not continuous, write 0 to the empty display RAM address data, until the address automatically adds 1 to the display RAM address where the next SEG is located.

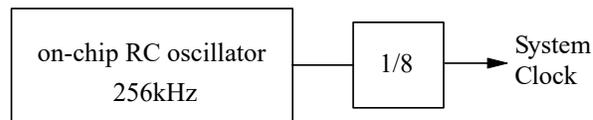
7.3 System Oscillator

The VK1072D system clock is used to generate the time base clock frequency, LCD driving clock. The source of the clock from on-chip RC oscillator (256kHz).

After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off, Once the system clock stops , then LCD display become darker and disappears , and the time base lose its function as well.

The LCD OFF command is used to turn the LCD bias generator off. After the LCD OFF command, using the SYS DIS command reduces power consumption, serving as a standby command.

System Oscillator Configuration :



7.4 LCD Driver

The VK1072D is a 72-segment LCD driver (18 SEG×4 COM). It supports software-configurable bias settings of 1/2 or 1/3, and COM configurations of 2COM or 3COM or 4COM.

7.5 Communication Interfacing

The VK1072D communicates with the host via a 3-wire serial interface.

When used solely for display output, only 3 lines are required (/CS, /WR, and DATA)

- /CS: Chip select input. It enables the serial interface when low and terminates communication when high.
- /WR: Write clock input. On the rising edge, data and commands from DATA are latched into the device.
- DATA: Bidirectional serial data line used to transfer both command and display data.

7.6 Command Format

The VK1072D is configured via software commands that support two primary modes: command mode and data mode.

- Command mode is used to configure system-level parameters. It is identified by a command mode ID of 100.
- Data mode supports two types of memory operations: WRITE, and MODIFY-WRITE.

These commands allow the host controller to configure LCD behavior and access display RAM contents.

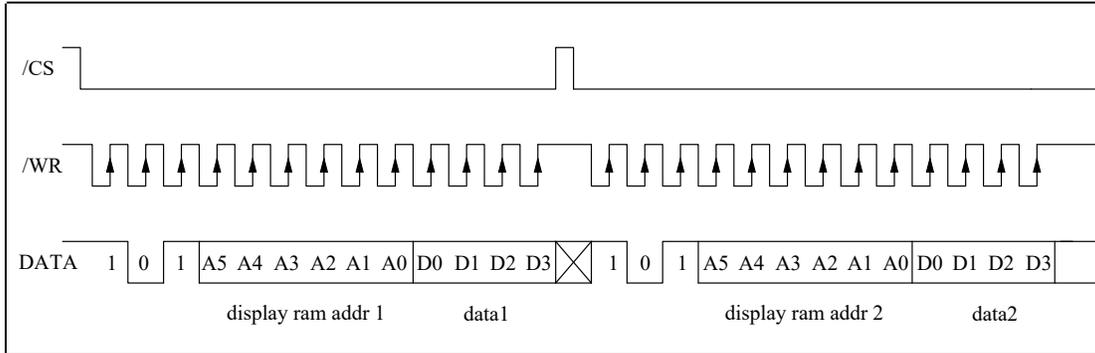
The following are the data mode IDs and the command mode ID:

Operation	MODE	ID
WRITE	DATA	101
COMMAND	COMMAND	100

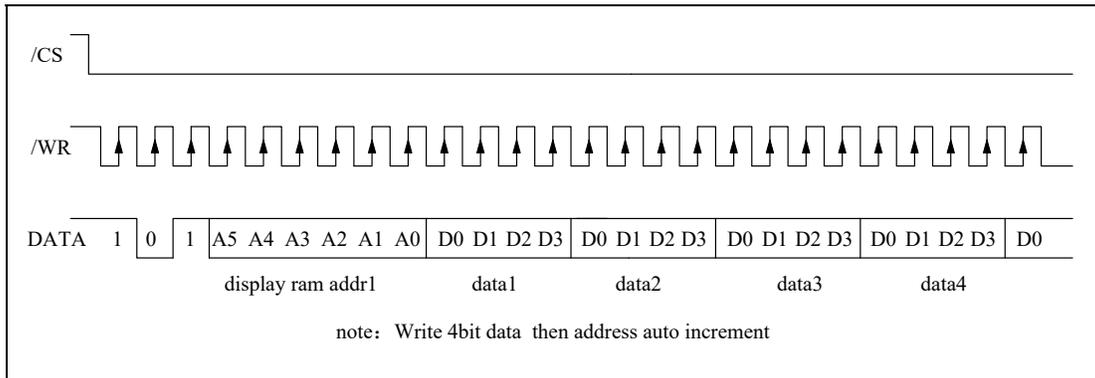
8 CMD/Data Timing Diagrams

8.1 WRITE Mode

Command Code : 101

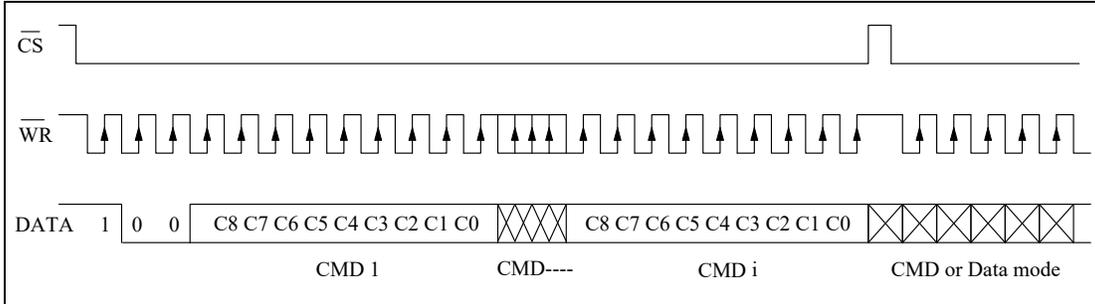


Successive Address Writing



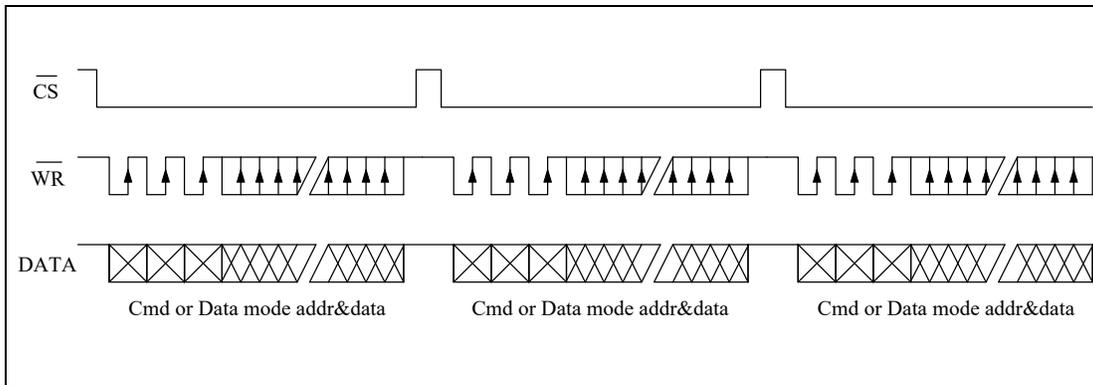
8.2 Command Mode

Command Code : 100



8.3 Data and Command Mode

Data and Command Mode



9 Command Summary

Name	ID	Command Code	D/C	Function	Def.
WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
SYS DIS	100	0000-0000-X	C	Turn off system oscillator	YES
SYS EN	100	0000-0001-X	C	Turn on the system clock	
LCD OFF	100	0000-0010-X	C	Turn off LCD bias generator	YES
LCD ON	100	0000-0011-X	C	Turn on LCD bias generator	
RC 256k	100	0001-10XX-X	C	on-chip RC oscillator	YES
BIAS 1/2	100	0010-abX0-X	C	LCD 1/2 bias option ab=00: 2 COMS ab=01: 3 COMS ab=10: 4 COMS	
BIAS 1/3	100	0010-abX1-X	C	LCD 1/3 bias option ab=00: 2 COMS ab=01: 3 COMS ab=10: 4 COMS	
TEST	100	1110-0000-X	C	Test mode	
NORMAL	100	1110-0011-X	C	Normal mode	YES

Note: X: 0 or 1

A5-A0: Display RAM addresses

D3-D0: 4bit Display RAM data

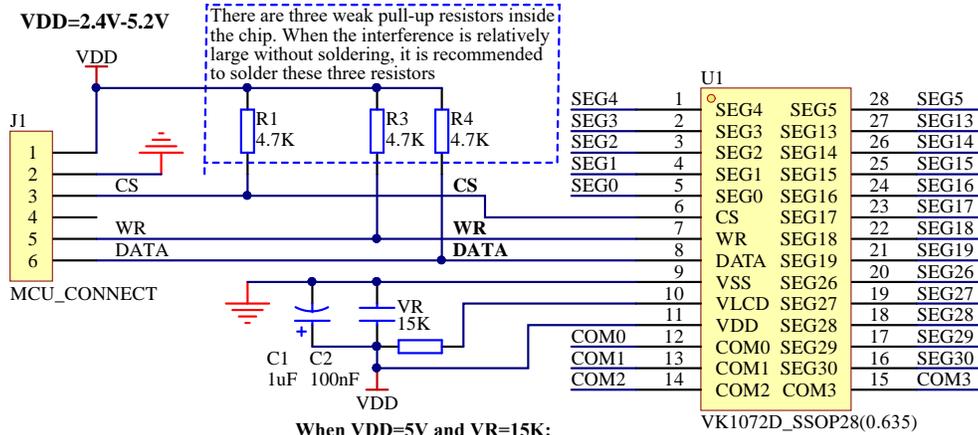
D/C: Data/Command mode

Def.: Power on reset default

101 and 100 is command ID

10 Application Circuits

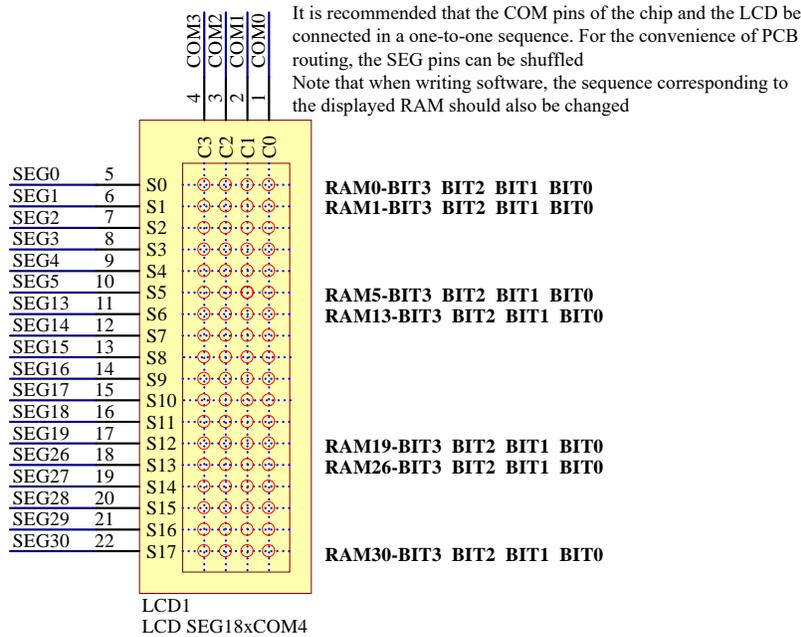
When the surrounding interference is relatively large, a 10R to 1k resistor and a PF-level small capacitor to ground can be connected in series on the communication pin. When the power supply of the single-chip microcomputer (3.3V) and the driver chip (5V) is inconsistent, it is recommended to add a level conversion circuit on the communication pin



When VDD=5V and VR=15K:

The VLCD is approximately 4.2V

It is recommended to use a 20K adjustable resistor for VR to achieve the best display effect and take the resistance value at this time.



11 Electrical characteristics

11.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3~5.5	V
Input Voltage	VIN	$V_{SS}-0.3\sim V_{DD}+0.3$	V
Storage Temperature	T _{STG}	-50~+125	°C
Operating Temperature	T _{OTG}	-40~+85	°C

11.2 DC Electrical Characteristics

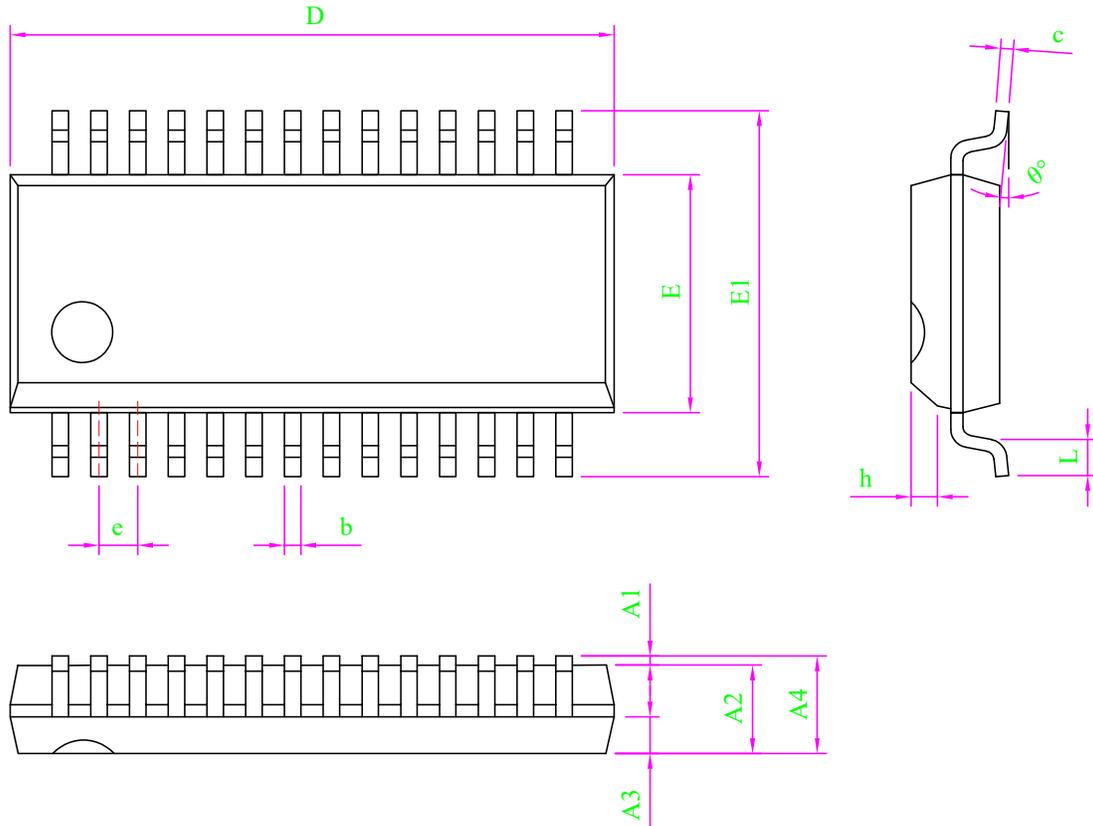
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	2.4	-	5.2	V	-	-
Operating current	I _{DD1}	-	150	300	μA	3V	No load/LCD ON On-chip RC oscillator
		-	300	600		5V	
Standby Current	I _{STB}	-	0.1	5	μA	3V	No load, Power down mode
		-	0.3	10		5V	
Low-level Input	V _{IL}	0	-	0.6	V	3V	DATA, /WR, /CS
		0	-	1.0		5V	
High-level Input	V _{IH}	2.4	-	3.0	V	3V	DATA, /WR, /CS
		4.0	-	5.0		5V	
DATA	I _{OL1}	0.5	1.2	-	mA	3V	V _{OL} =0.3V
		1.3	2.6	-		5V	V _{OL} =0.5V
DATA	I _{OH1}	-0.4	-0.8	-	mA	3V	V _{OH} =2.7V
		-0.9	-1.8	-		5V	V _{OH} =4.5V
LCD COM Sink Current	I _{OL2}	80	150	-	μA	3V	V _{OL} =0.3V
		150	250	-		5V	V _{OL} =0.5V
LCD COM Source Current	I _{OH2}	-80	-120	-	μA	3V	V _{OH} =2.7V
		-120	-200	-		5V	V _{OH} =4.5V
LCD SEG Sink Current	I _{OL3}	60	120	-	μA	3V	V _{OL} =0.3V
		120	200	-		5V	V _{OL} =0.5V
LCD SEG Source Current	I _{OH3}	-40	-70	-	μA	3V	V _{OH} =2.7V
		-70	-100	-		5V	V _{OH} =4.5V
Pull-UP Resistor RUP	R _{UP}	40	80	150	kΩ	3V	DATA, /WR, /CS
		30	60	100		5V	

11.3 AC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
System Clock	f_{SYS1}	-	256	-	kHz	3V	On-chip RC oscillator
		-	256	-		5V	On-chip RC oscillator
LCD Clock	f_{LCD1}	-	$f_{SYS1}/1024$	-			On-chip RC oscillator
LCD Common Period	t_{COM}	-	n/f_{LCD}	-	sec	-	N: Number of COM
Serial Data Clock(/WR)	F_{CLK1}	-	-	150	kHz	3V	Duty cycle 50%
		-	-	300		5V	
Serial Interface Reset PW	t_{CS}	-	250	-	ns	-	/CS
/WR Input Pulse Width	t_{CLK}	3.34	-	-	μ s	3V	Write mode
		1.67	-	-	μ s	5V	Write mode
Rise/Fall Time Serial Data Clock Width	t_r, t_f	-	120	-	ns	3V	-
		-	120	-		5V	
Setup Time for DATA to /WR Clock Width	t_{su}	-	120	-	ns	3V	-
		-	120	-		5V	
Hold Time for DATA to /WR Clock Width	t_h	-	120	-	ns	3V	-
		-	120	-		5V	
Setup Time for /CS to /WR Clock Width	t_{su1}	-	100	-	ns	3V	-
		-	100	-		5V	
Hold Time for /CS to /WR Clock Width	t_{h1}	-	100	-	ns	3V	-
		-	100	-		5V	

12 Package Information

12.1 SSOP28(150mil) (9.9mm × 3.9mm PP=0.635mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.05	-	0.23
A2	1.35	1.45	1.55
A3	0.60	0.65	0.70
b	0.23	-	0.31
c	0.19	-	0.25
D	9.80	9.90	10.00
E	3.90	3.90	4.00
E1	5.80	6.00	6.20
e	0.635 BSC		
h	0.30	-	0.50
L	0.60	-	0.80
θ	0	-	8°

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14 Revision History

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Initial release	YES
2	1.1	2018-10-11	Add reference circuit	YES
3	1.2	2019-03-21	Alignment correction	YES
4	1.3	2025-05-06	Change Description	YES

[1] Please refer to the latest version of this document before starting or finalizing any design.

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