永嘉微电
Vinka Microelectronics

VK1072B Datasheet

18×4 LCD DRIVER

Rev.1.3

Intellectual Property Statement:

Shenzhen Vinka Microelectronics Co., Ltd. (hereinafter referred to as "the Company") owns legally registered intellectual property rights in both domestic and international jurisdictions. Any unauthorized use of the Company's products or patented technologies by individuals or organizations is strictly prohibited.

The Company reserves the right to take legal action against any infringement, and to seek full compensation for damages or unlawful gains.

The Company's name and trademarks are legally protected and may not be used or imitated without explicit written permission. No implied or express license shall be granted under any circumstances.

1 General Description

The VK1072B is a dot-matrix memory-mapped LCD driver that supports LCD screens with a maximum of 72 dots (18SEG×4COM), as well as 2COM and 3COM LCD screens. The single-chip microcomputer can be configured with display parameters and send display data through three communication lines, and can also enter power-saving mode through instructions.

2 Key Features

- Operating voltage：2.4-5.2V
- Integrated RC oscillator (default)
- Selectable LCD bias: 1/2 or 1/3
- Selectable LCD duty: 1/2 or 1/3 or 1/4
- Built-in 32×4 bit display RAM
- Power-down mode via software command(LCD OFF, SYS DIS)
- 3 wire serial communication interface
- Software-configurable of LCD parameters
- Dual command formats for configuration and access
- Auto-increment addressing for sequential write
- VLCD adjustable via external pin ($\leq$ VDD)
- Available Packages:
  SOP28 (300mil) (18mm × 7.5mm PP=1.27mm)

3 Application field

- Electricity meter/gas meter
- Massage device/beauty device
- Medical instruments
- Vehicle-mounted equipment
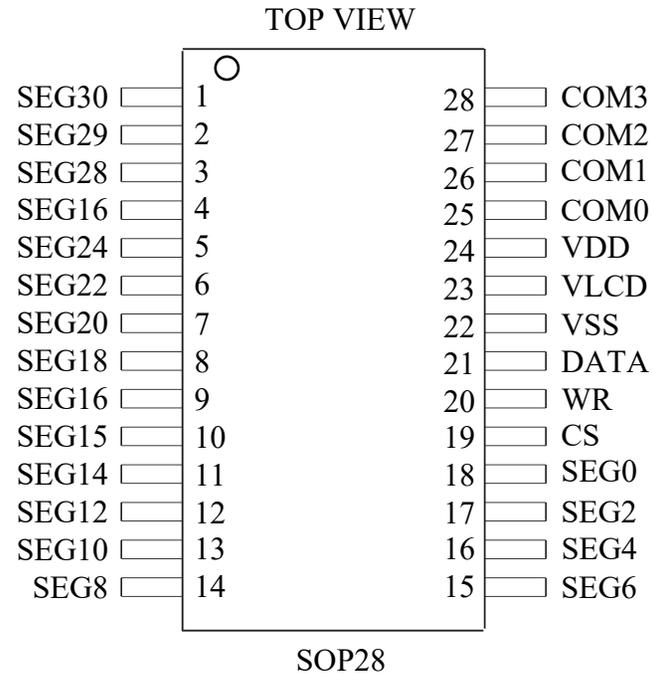- Air conditioner/heater

4 Product Selection

Part No.	SEG × COM	BIAS	DUTY	Packaging
VK1024B	6×4,6×3,6×2	1/2,1/3	1/2,1/3,1/4	SOP16
VK1056B	14×4,14×3,14×2	1/2,1/3	1/2,1/3,1/4	SOP24
VK1056C	14×4,14×3,14×2	1/2,1/3	1/2,1/3,1/4	SSOP24
VK1056Q	14×4,14×3,14×2	1/2,1/3	1/2,1/3,1/4	QFN24L
VK1072B	18×4,18×3,18×2	1/2,1/3	1/2,1/3,1/4	SOP28
VK1072C	18×4,18×3,18×2	1/2,1/3	1/2,1/3,1/4	SOP28
VK1072D	18×4,18×3,18×2	1/2,1/3	1/2,1/3,1/4	SSOP28
VK1088B	22×4,22×3,22×2	1/2,1/3	1/2,1/3,1/4	QFN32L
VK1128C	32×4,32×3,32×2	1/2,1/3	1/2,1/3,1/4	QFN48L

5 Ordering Information

Part No.	Packaging	Tube Qty	Tray Qty	Box Qty	Total Qty	Notes
VK1024B	SOP16	50/tube		10000/box	100000 PCS	
VK1056B	SOP24	30/tube		2400/box	24000 PCS	
VK1056C	SSOP24	60/tube		6000/box	60000 PCS	
VK1056Q	QFN24L		490/tray	4900/box	29400 PCS	
VK1072B	SOP28	26/tube		2080/box	20800 PCS	
VK1072C	SOP28	26/tube		2080/box	20800 PCS	
VK1072D	SSOP28	50/tube		5000/box	50000 PCS	
VK1088B	QFN32L			3000/box	24000 PCS	
VK1128C	QFN48L		3000/tray		24000 PCS	

6 Package Pinout Information(SOP28)

TOP VIEW

```
SEG30 ⊏ 1          28 ⊐ COM3
SEG29 ⊏ 2          27 ⊐ COM2
SEG28 ⊏ 3          26 ⊐ COM1
SEG16 ⊏ 4          25 ⊐ COM0
SEG24 ⊏ 5          24 ⊐ VDD
SEG22 ⊏ 6          23 ⊐ VLCD
SEG20 ⊏ 7          22 ⊐ VSS
SEG18 ⊏ 8          21 ⊐ DATA
SEG16 ⊏ 9          20 ⊐ WR
SEG15 ⊏ 10         19 ⊐ CS
SEG14 ⊏ 11         18 ⊐ SEG0
SEG12 ⊏ 12         17 ⊐ SEG2
SEG10 ⊏ 13         16 ⊐ SEG4
SEG8 ⊏ 14          15 ⊐ SEG6
```

SOP28

For more information:

6.1   VK1072B/SOP28 Pin Description

No.	Name	I/O	Function
1-18	SEG30-SEG0	O	LCD SEG drive outputs
19	CS	I	Chip select signal with pull-up resistor ,active low.
20	WR	I	Serial write signal with pull-up resistor, data latched on the rising edge of the /WR signal.
21	DATA	I/O	Serial data signal with pull-up resistor, input/output depending on access mode.
22	VSS	VSS	Negative power supply
23	VLCD	I	LCD driving voltage input,must be ≤VDD
24	VDD	VDD	Positive power supply
25-28	COM0-COM3	O	LCD COM drive outputs

7　Functional Description

7.1　Block Diagram
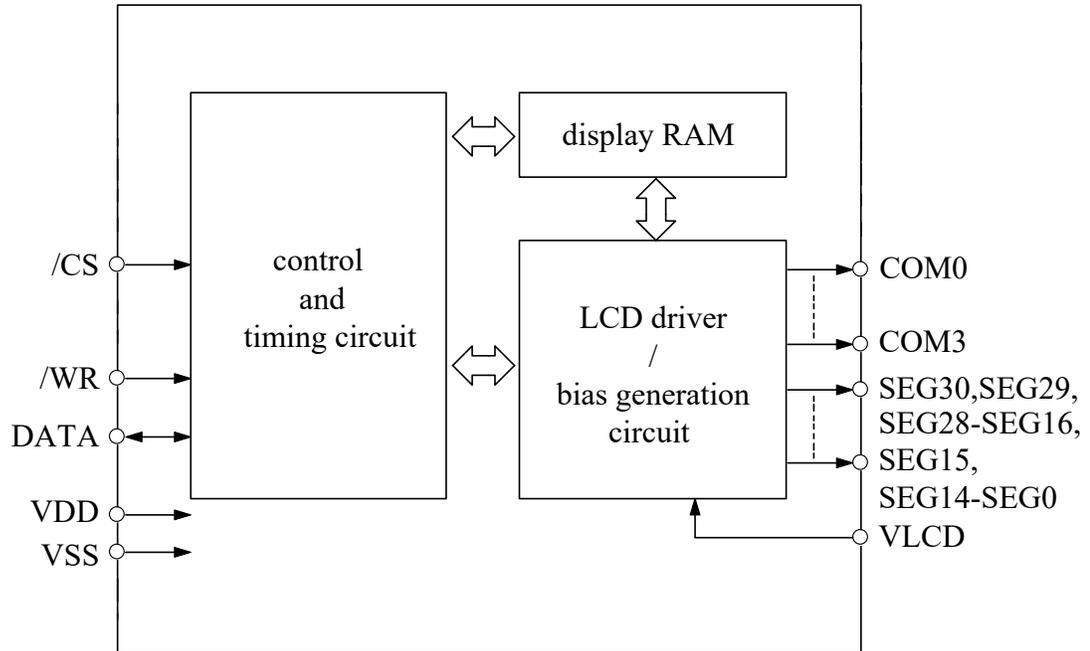
7.2 Display RAM

The VK1072B integrates 32 × 4-bit RAM for LCD display. directly mapped to SEGx/ COMx segments. Data is latched and updated on the LCD according to scan timing set by the system configuration. The display RAM can be accessed using three commands: WRITE, and MODIFY-WRITE. Each RAM address corresponds to a specific combination of SEG and COM lines.

The following is a mapping from the RAM to the LCD pattern:

	COM3	COM2	COM1	COM0		
SEG0					0	
SEG2					2	Address 6 bit
SEG4					4	（A5----A0）
SEG6					6	
⋮					⋮	
SEG30					30	
					31	
	D3	D2	D1	D0	Data\Addr	

Note：
1. When the SEG is not continuous, the display RAM address is also not continuous.
2. When writing multiple data continuously，the display data address is automatically incremented by 1.When SEG is not continuous，write 0 to the empty display RAM addressdata，until the address automatically adds 1 to the display RAM address where the next SEG is located.

7.3 System Oscillator

The VK1072B system clock is used to generate the time base clock frequency, LCD driving clock. The source of the clock from on-chip RC oscillator (256kHz).

After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off, Once the system clock stops，then LCD display become darker and disappears，and the time base lose its function as well.

The LCD OFF command is used to turn the LCD bias generator off. After the LCD OFF command, using the SYS DIS command reduces power consumption, serving as a standby command.

System Oscillator Configuration：
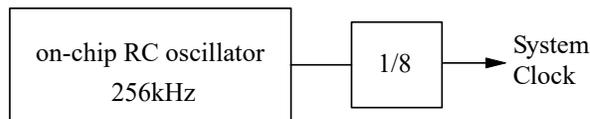
7.4   LCD Driver

The VK1072B is a 72-segment LCD driver (18 SEG×4 COM). It supports software-configurable bias settings of 1/2 or 1/3, and COM configurations of 2COM or 3COM or 4COM.

7.5   Communication Interfacing

The VK1072B communicates with the host via a 3-wire serial interface.

When used solely for display output, only 3 lines are required (/CS, /WR, and DATA)

- /CS: Chip select input. It enables the serial interface when low and terminates communication when high.

- /WR: Write clock input. On the rising edge, data and commands from DATA are latched into the device.

- DATA: Bidirectional serial data line used to transfer both command and display data.

7.6   Command Format

The VK1072B is configured via software commands that support two primary modes: command mode and data mode.

- Command mode is used to configure system-level parameters. It is identified by a command mode ID of 100.

- Data mode supports two types of memory operations: WRITE, and MODIFY-WRITE.

These commands allow the host controller to configure LCD behavior and access display RAM contents.

The following are the data mode IDs and the command mode ID:

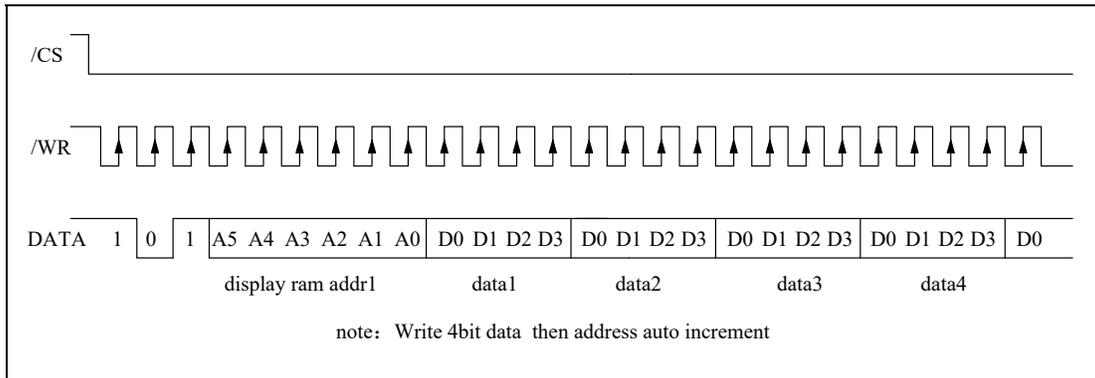| Operation	MODE	ID
WRITE	DATA	101
COMMAND	COMMAND	100

8 CMD/Data Timing Diagrams

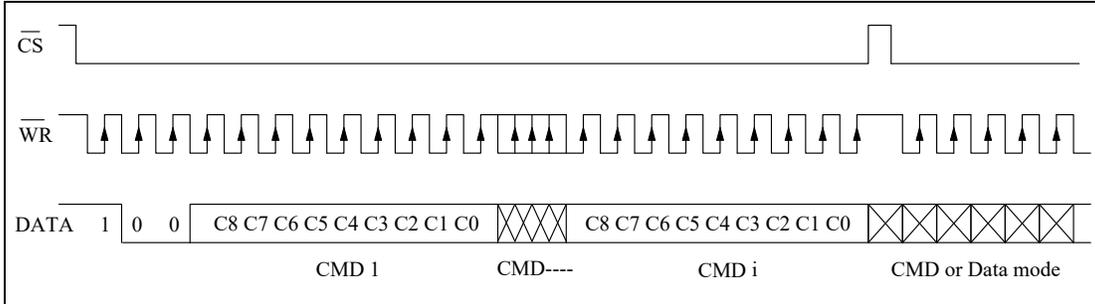## 8.1 WRITE Mode

Command Code : 101
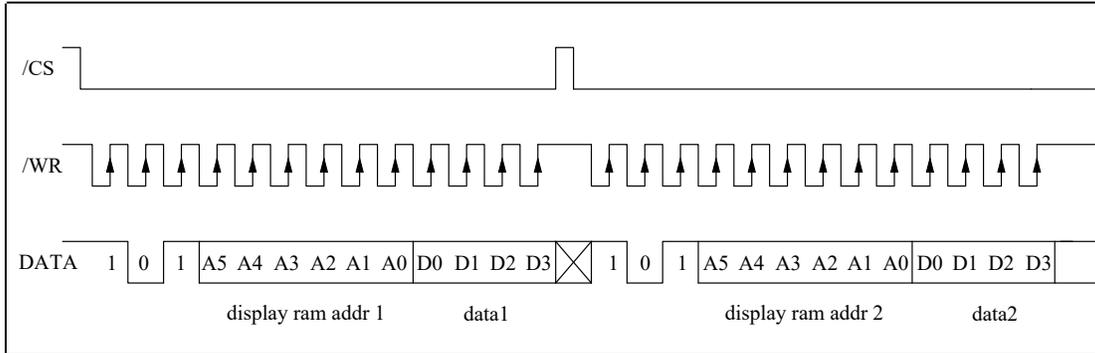
Successive Address Writing

8.2 Command Mode

Command Code : 100

8.3 Data and Command Mode

Data and Command Mode
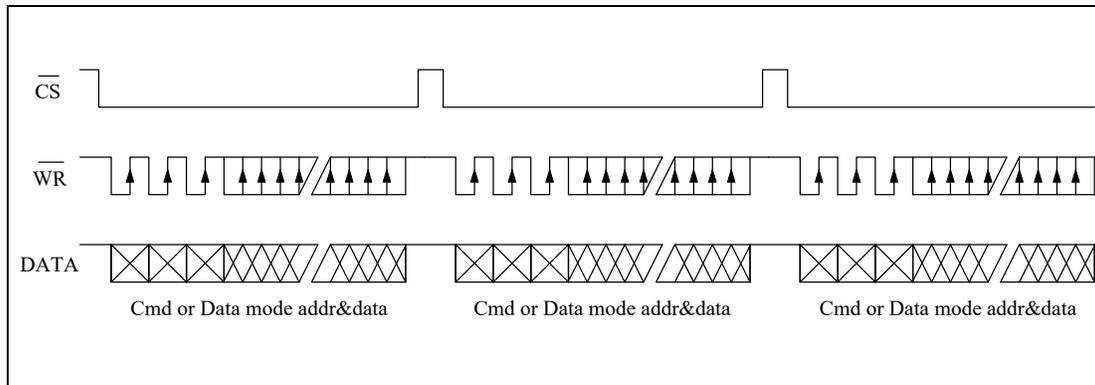
9 Command Summary

Name	ID	Command Code	D/C	Function	Def.
WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
SYS DIS	100	0000-0000-X	C	Turn off system oscillator	YES
SYS EN	100	0000-0001-X	C	Turn on the system clock	
LCD OFF	100	0000-0010-X	C	Turn off LCD bias generator	YES
LCD ON	100	0000-0011-X	C	Turn on LCD bias generator	
RC 256k	100	0001-10XX-X	C	on-chip RC oscillator	YES
BIAS 1/2	100	0010-abX0-X	C	LCD 1/2 bias option ab=00：2 COMS ab=01：3 COMS ab=10：4 COMS	
BIAS 1/3	100	0010-abX1-X	C	LCD 1/3 bias option ab=00：2 COMS ab=01：3 COMS ab=10：4 COMS	
TEST	100	1110-0000-X	C	Test mode	
NORMAL	100	1110-0011-X	C	Normal mode	YES

Note: X：0 or 1   D/C： Data/Command mode

A5-A0：DIspaly RAM addresses   Def.：Power on reset default

D3-D0：4bit DIspaly RAM data   101 and 100 is command ID

永嘉微电
Vinka Microelectronics

10 Application Circuits

When the surrounding interference is relatively large, a 10R to 1k resistor and a PF-level small capacitor to ground can be connected in series on the communication pin. When the power supply of the single-chip microcomputer (3.3V) and the driver chip (5V) is inconsistent, it is recommended to add a level conversion circuit on the communication pin

VDD=2.4V-5.2V

There are three weak pull-up resistors inside the chip. When the interference is relatively large without soldering, it is recommended to solder these three resistors

R1 4.7K   R3 4.7K   R4 4.7K

J1
1
2
3 CS
4
5 WR
6 DATA
MCU_CONNECT

U1
1	SEG30	COM3	28	COM3
2	SEG29	COM2	27	COM2
3	SEG28	COM1	26	COM1
4	SEG26	COM0	25	COM0
5	SEG24	VDD	24	
6	SEG22	VLCD	23	
7	SEG20	VSS	22	
8	SEG18	DATA	21	DATA
9	SEG16	WR	20	WR
10	SEG15	CS	19	CS
11	SEG14	SEG0	18	SEG0
12	SEG12	SEG2	17	SEG2
13	SEG10	SEG4	16	SEG4
14	SEG8	SEG6	15	SEG6

VK1072B_SOP28(1.27)

VDD
VR 15K
C1 1uF
C2 100nF

When VDD=5V and VR=15K:
The VLCD is approximately 4.2V
It is recommended to use a 20K adjustable resistor for VR to achieve the best display effect and take the resistance value at this time.

COM3 4 COM2 3 COM1 2 COM0 1

It is recommended that the COM pins of the chip and the LCD be connected in a one-to-one sequence
The SEG pins can be shuffled for the convenience of PCB routing
Note that when writing software, the sequence corresponding to the displayed RAM should also be changed

C3 C2 C1 C0

SEG0	5	S0	RAM0-BIT3 BIT2 BIT1 BIT0
SEG2	6	S1	RAM2-BIT3 BIT2 BIT1 BIT0
SEG4	7	S2	
SEG6	8	S3	
SEG8	9	S4	
SEG10	10	S5	
SEG12	11	S6	
SEG14	12	S7	RAM14-BIT3 BIT2 BIT1 BIT0
SEG15	13	S8	RAM15-BIT3 BIT2 BIT1 BIT0
SEG16	14	S9	
SEG18	15	S10	
SEG20	16	S11	
SEG22	17	S12	
SEG24	18	S13	
SEG26	19	S14	RAM26-BIT3 BIT2 BIT1 BIT0
SEG28	20	S15	RAM28-BIT3 BIT2 BIT1 BIT0
SEG29	21	S16	RAM29-BIT3 BIT2 BIT1 BIT0
SEG30	22	S17	RAM30-BIT3 BIT2 BIT1 BIT0

LCD1
LCD SEG18COM4

11 Electrical characteristics

11.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3～5.5	V
Input Voltage	VIN	V_{SS}-0.3～V_{DD}+0.3	V
Storage Temperature	T_{STG}	-50～+125	℃
Operating Temperature	T_{OTG}	-40～+85	℃

11.2 DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	2.4	-	5.2	V	-	-
Operating current	I_{DD1}	-	150	300	μA	3V	No load/LCD ON On-chip RC oscillator
		-	300	600		5V	
Standby Current	I_{STB}	-	0.1	5	μA	3V	No load, Power down mode
		-	0.3	10		5V	
Low-level Input	V_{IL}	0	-	0.6	V	3V	DATA, /WR, /CS
		0	-	1.0		5V	
High-level Input	V_{IH}	2.4	-	3.0	V	3V	DATA, /WR, /CS
		4.0	-	5.0		5V	
DATA	I_{OL1}	0.5	1.2	-	mA	3V	V_{OL}=0.3V
		1.3	2.6	-		5V	V_{OL}=0.5V
DATA	I_{OH1}	-0.4	-0.8	-	mA	3V	V_{OH}=2.7V
		-0.9	-1.8	-		5V	V_{OH}=4.5V
LCD COM Sink Current	I_{OL2}	80	150	-	μA	3V	V_{OL}=0.3V
		150	250	-		5V	V_{OL}=0.5V
LCD COM Source Current	I_{OH2}	-80	-120	-	μA	3V	V_{OH}=2.7V
		-120	-200	-		5V	V_{OH}=4.5V
LCD SEG Sink Current	I_{OL3}	60	120	-	μA	3V	V_{OL}=0.3V
		120	200	-		5V	V_{OL}=0.5V
LCD SEG Source Current	I_{OH3}	-40	-70	-	μA	3V	V_{OH}=2.7V
		-70	-100	-		5V	V_{OH}=4.5V
Pull-UP Resistor RUP	R_{UP}	40	80	150	kΩ	3V	DATA, /WR, /CS
		30	60	100		5V	

11.3 AC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
System Clock	f_{SYS1}	-	256	-	kHz	3V	On-chip RC oscillator
		-	256	-		5V	On-chip RC oscillator
LCD Clock	f_{LCD1}	-	$f_{SYS1}/1024$	-			On-chip RC oscillator
LCD Common Period	t_{COM}	-	n/f_{LCD}	-	sec	-	N：Number of COM
Serial Data Clock(/WR)	F_{CLK1}	-	-	150	kHz	3V	Duty cycle 50%
		-	-	300		5V	
Serial Interface Reset PW	t_{CS}	-	250	-	ns	-	/CS
/WR Input Pulse Width	t_{CLK}	3.34	-	-	μs	3V	Write mode
		1.67	-	-	μs	5V	Write mode
Rise/Fall Time Serial Data Clock Width	t_r，t_f	-	120	-	ns	3V	-
						5V	
Setup Time for DATA to /WR Clock Width	t_{su}	-	120	-	ns	3V	-
						5V	
Hold Time for DATA to /WR Clock Width	t_h	-	120	-	ns	3V	-
						5V	
Setup Time for /CS to /WR Clock Width	t_{su1}	-	100	-	ns	3V	-
						5V	
Hold Time for /CS to /WR Clock Width	t_{h1}	-	100	-	ns	3V	-
						5V	

12   Package Information

12.1   SOP28 (300mil) (18mm x 7.5mm PP=1.27mm)
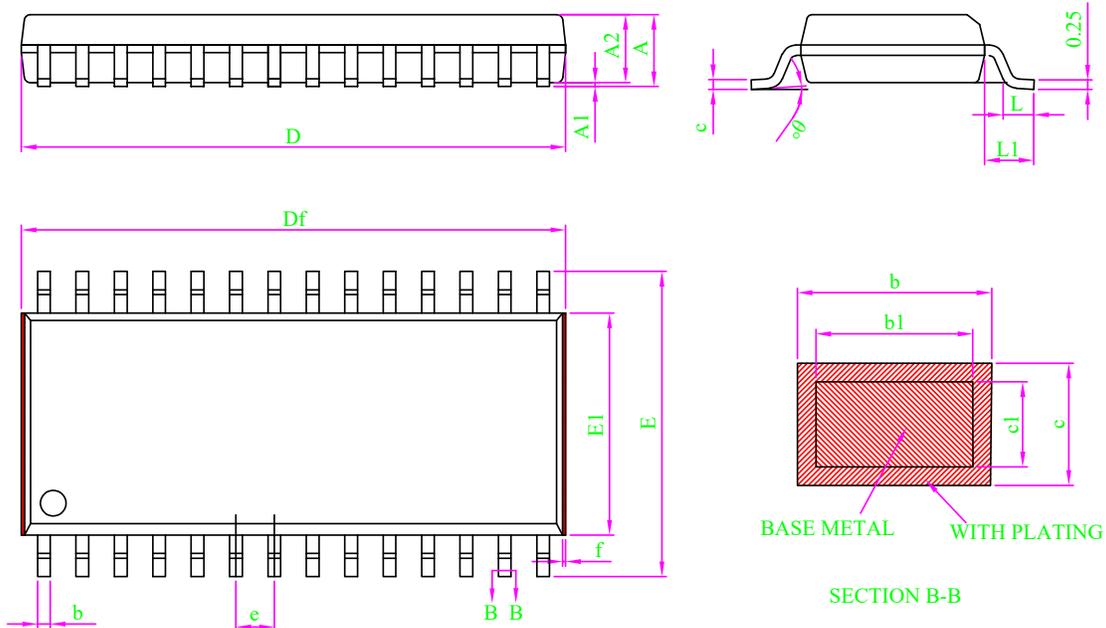
Note:

1. All dimension are in m

2. Dim D& El does not include plast flas；Df includes plastic flash(f);Flash: Plastic residual around body edge after de junk / singulation.

3. Dim b does not include damb protrusion/intrusion.

4.Plating thickness 0.007mm-0.020mm

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	2.64
A1	0.10	0.15	0.20
A2	2.24	2.34	2.44
b	0.39	-	0.47
b1	0.38	0.41	0.43
c	0.25	-	0.30
c1	0.24	0.25	0.26
D	17.90	18.00	18.10
Df	18.00	-	18.50
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
L	0.71	0.86	1.01
L1	1.30	1.40	1.50
θ	0	-	8°
f	0.05	-	0.20

13 Disclaimer

Warranty and liability —— The information provided in this document is believed to be accurate and reliable. However, Shenzhen Vinka Microelectronics Co., Ltd. (hereinafter "the Company") makes no warranties, express or implied, as to the completeness or suitability of this information for any specific purpose.

In no event shall the Company be liable for any indirect, incidental, or consequential damages, including but not limited to loss of profits, equipment damage, or system failure, arising out of the use of this product or documentation, regardless of the legal theory under which such liability is asserted.

Right to change —— The Company reserves the right to modify any information contained herein without prior notice. The latest version of this document is available at: https://www.szvinka.com/

Applicability —— This product is not designed or intended for use in life-critical, medical, or safety systems where failure could result in injury or death. The customer shall assume full responsibility for any such use.

Application —— All product application descriptions provided herein are intended for illustrative purposes only.
The Company makes no representations or warranties, express or implied, regarding the suitability of any specific application without further testing or modification.

The customer is solely responsible for determining whether the Company's products are appropriate for their intended applications or end customers.

The customer shall ensure proper design practices, implementation safeguards, and operational validation to minimize risks associated with product use.

The Company shall not be held liable for any defects, losses, costs, or damages arising from weaknesses or failures in the customer's own products or applications, or from the integration or use of third-party products.

Furthermore, the customer shall conduct all necessary testing and validation for any third-party deployment of the Company's products to avoid potential misuse or associated damages. The Company assumes no liability in this regard.

Commercial terms of sale —— Unless otherwise agreed in writing, sales of this product are subject to the Company's standard terms and conditions of sale. The Company expressly rejects the applicability of the customer's general terms and conditions.

Export control —— This product may be subject to applicable export control regulations. The customer is solely responsible for compliance with such regulations, including obtaining any necessary export licenses.

14 Revision History

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Initial release	YES
2	1.1	2018-10-11	Add reference circuit	YES
3	1.2	2019-03-21	Alignment correction	YES
4	1.3	2025-05-06	Change Description	YES

[1] Please refer to the latest version of this document before starting or finalizing any design.

[2] Since the release of this document, the status or availability of this product may have changed. For the most up-to-date information, please visit:
https://www.szvinka.com/